A Hardware Track Finder for ATLAS Trigger

G. Volpi on behalf of the FTK group

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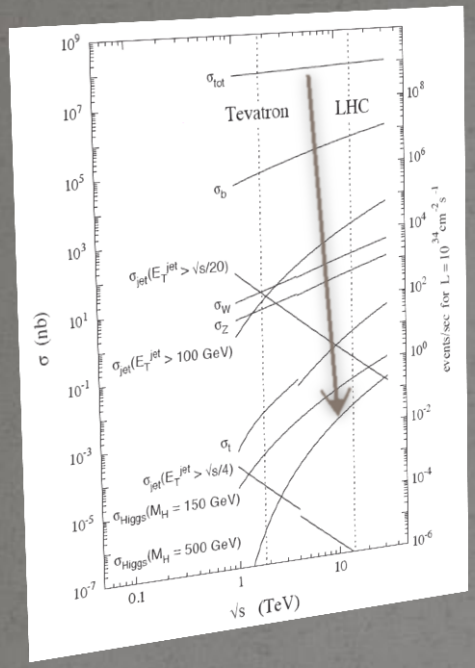
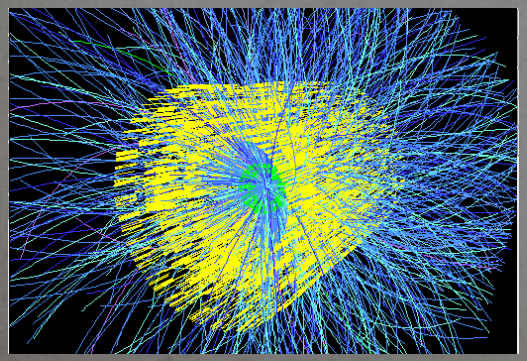
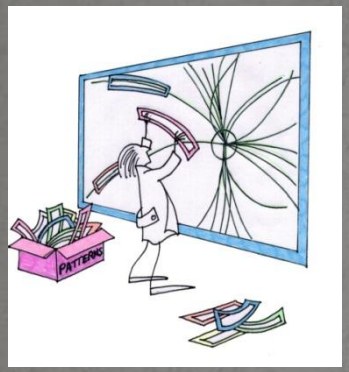
The Motivation and the Challenge

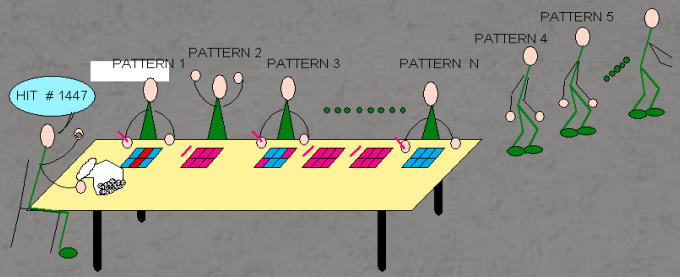


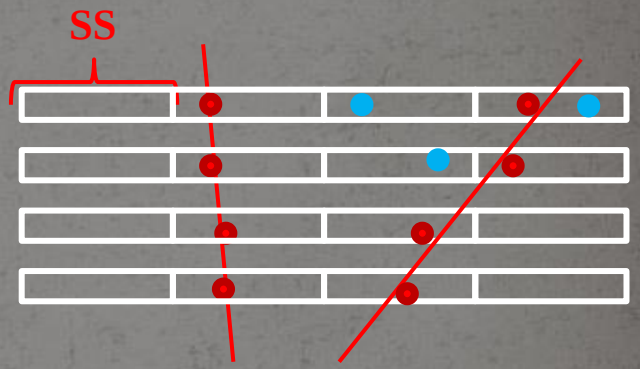


- Testing the standard model at very high precision
- Unexplored regime at 14 TeV
- Need to reject more than 10 orders of magnitude to be sensitive to interesting processes
- Event selection complicated by the presence of a large number of pileup events
  - Full tracking is a powerful tool to limit its effect
- Particles from interesting processes can be buried in a high particle density in the event
- Precision standard model measurements and discovering BSM require ability to:
  - Recognize isolated muons and electrons generated from Z and W bosons
  - Tag b- or tau-jets

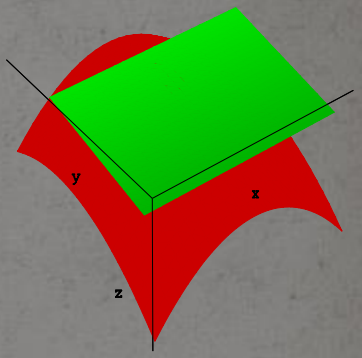
The FTK basic ideas





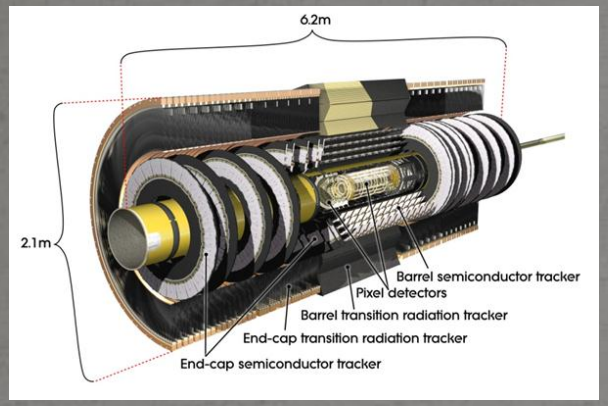


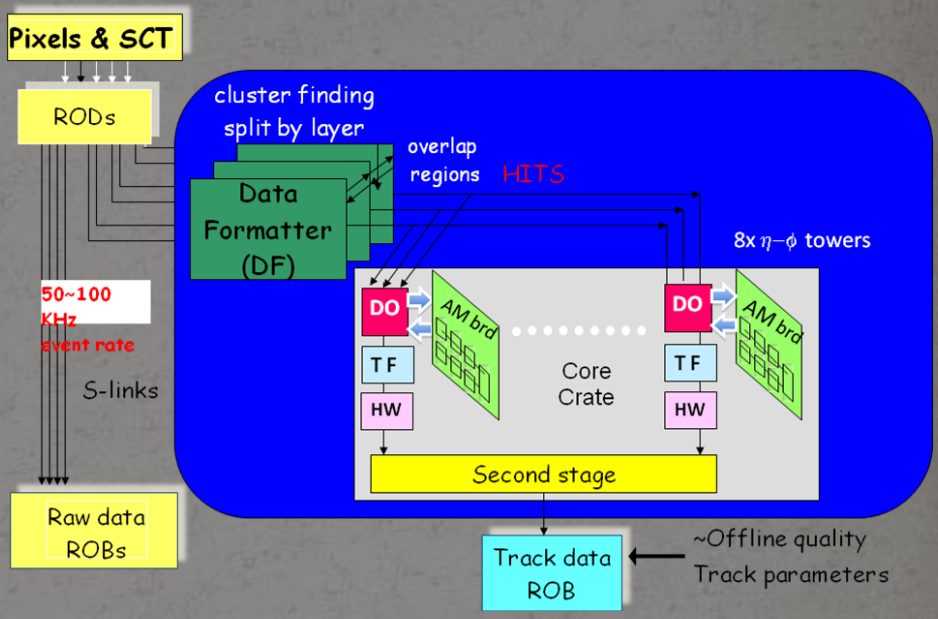
- FTK algorithms designed to be simple and highly parallel
- Tracking divided into two sequential steps
- The pattern matching uses 1 billion patterns and special hardware
  - Hits are grouped in super-strips (SS) with coarse resolution
  - Limited resolution reduces the number of pre-computed patterns
- The track's parameters are evaluated from the full resolution hits using a linear Principal Component Analysis algorithm (j.nima.2003.11.078)



$$p_i = \sum_j C_{ij} \cdot x_j + q_i$$

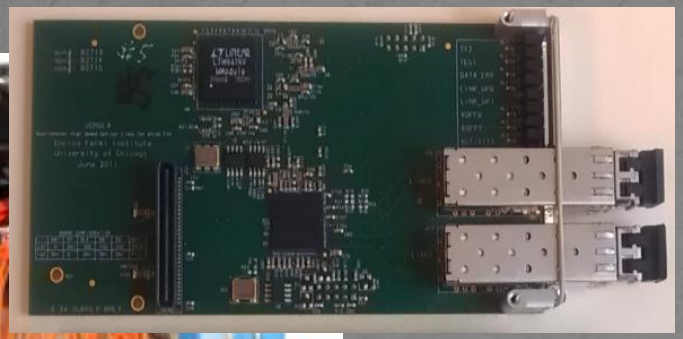
FTK architecture overview





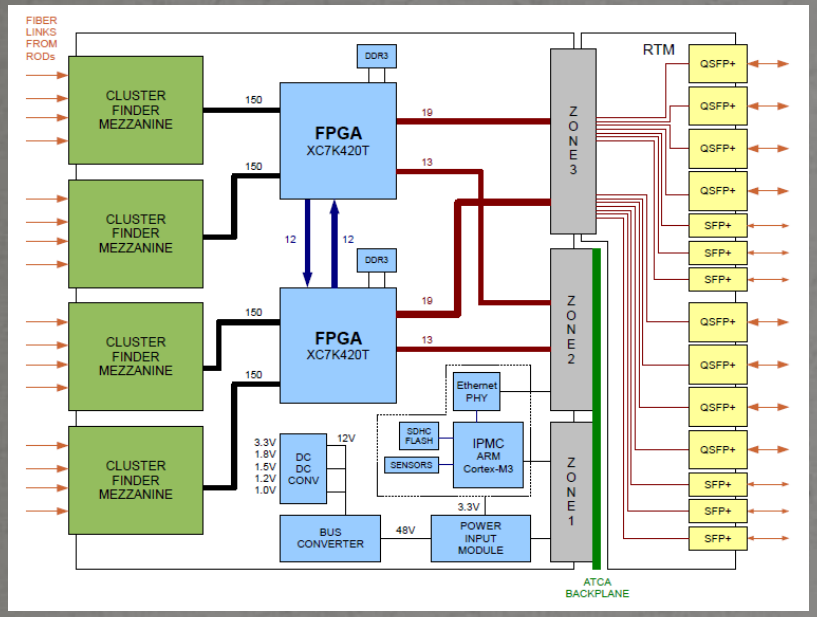
- A copy of all the silicon data is sent to the FTK processing units at each level-1 accept (up to 100 KHz)
- The inner detector modules are organized in 64 overlapping η-φ towers
  - Each tower has 8 parallel processing units to perform the pattern recognition and a preliminary fitting stage

Dual output HOLA board

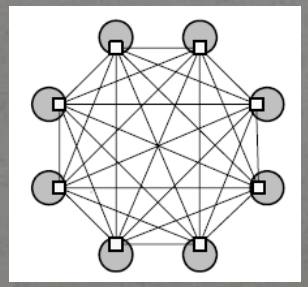


- This is the interface from the ATLAS tracking system
- It is installed on the silicon RODs and sends the same data to two independent streams: DAQ and FTK
- FTK flow control can be disabled during installation and testing, and enabled during normal operation
- 270 boards produced and tested
- 31 were installed in ATLAS during the winter shutdown and will take data in 2012

Data input and formatting

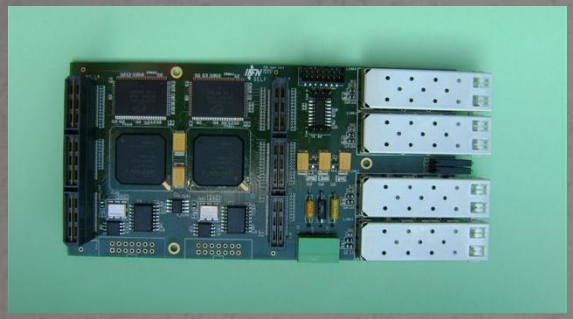


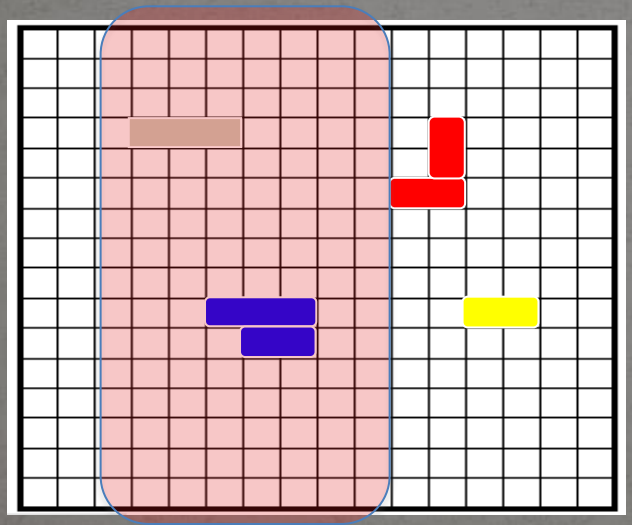
Full mesh backplane data sharing



- 32 Data Formatter boards will collect and organize the clusters
  - Clustering performed in mezzanine cards (next slide)
- The DF has to map the ROD data into the FTK η-φ towers
  - High data sharing between the boards
  - Inter-shelf sharing via an optical link
- ATCA technology was selected

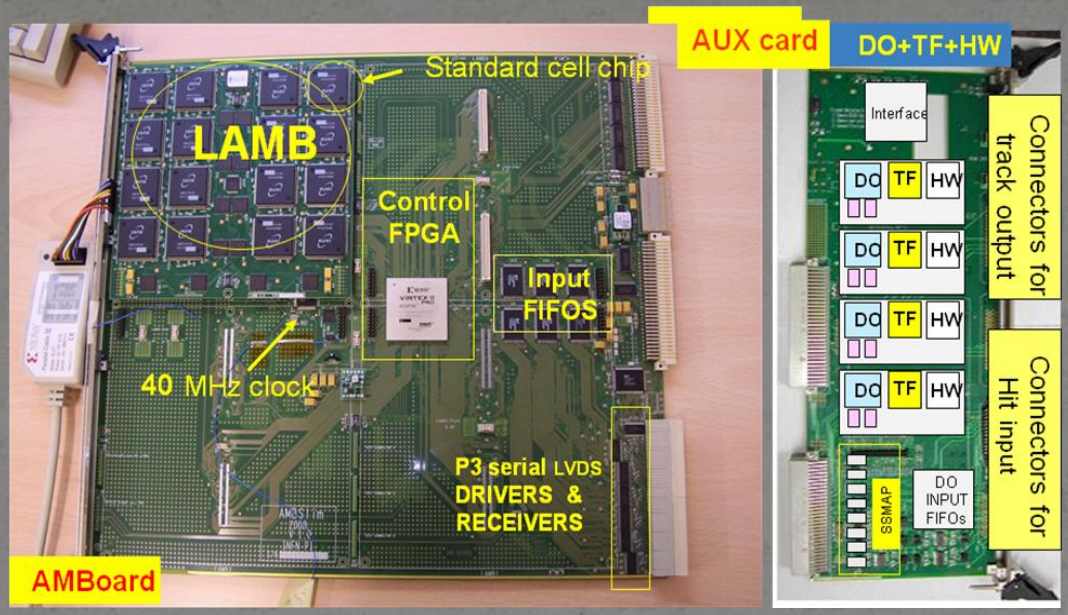
FTK Input mezzanine





- The “FTK input mezzanine” (FTK_IM) receives up to 4 slinks 1.25 Gbps
- It asserts flow control to the HOLAS
- A clustering algorithm is performed to find the hit centroids
  - For the pixels a full 2D identification of the cluster shape is required
  - For the SCT a partial clustering is already done in the FE chip, boundary corrections are however required
- First prototypes prepared
  - Communication with HOLA tested
  - Clustering firmware has to be finalized

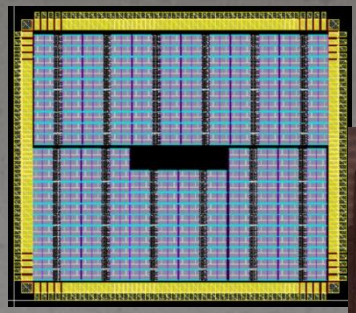
AM board and AUX card

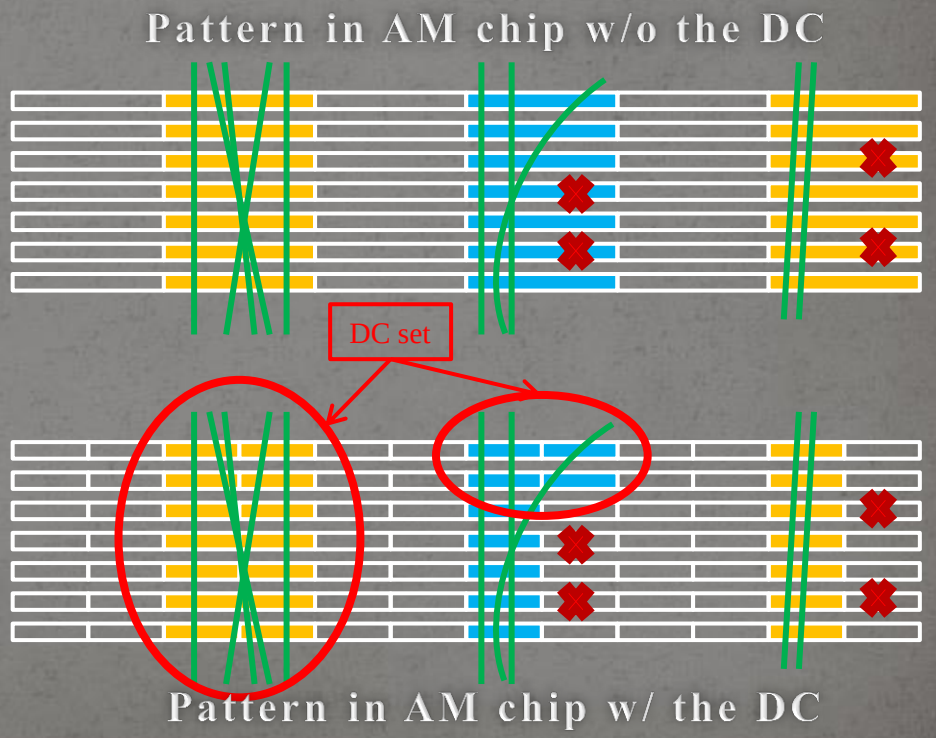


- A processing unit consists of an AM-board and AUX card
- The AUX-card receives the hits from the DF converting the hits into SS and storing the full resolution clusters for the track fitter
- The AM board has 128 AM chips, contained on 4 cards
  - Packed and hot: 100 A at 1.2 V, about 2 kg
- The roads found from the AM are sent back to the AUX and the TF performs fits using the full resolution hits

AM Chip 04

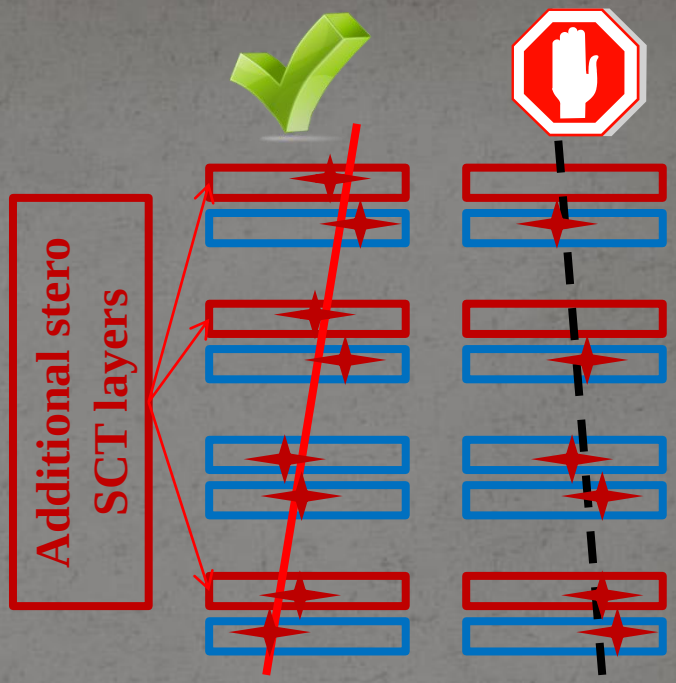
- Many improvements with respect the last version used in CDF
- 65 nm instead of 180 nm
- Up to **80 kpatterns** per chip
- Custom cells to increase the density of patterns
- Selective pre-charge to reduce the power consumption
- Up to 8 detector layers can used
- CAM-like don't care capability to have **variable resolution SS size** to optimize efficiency, pattern density and noise rejection
  (10.1109/ANIMMA.2011.6172856)
- First small area prototypes with 8 kpatterns arrived and ready to be tested

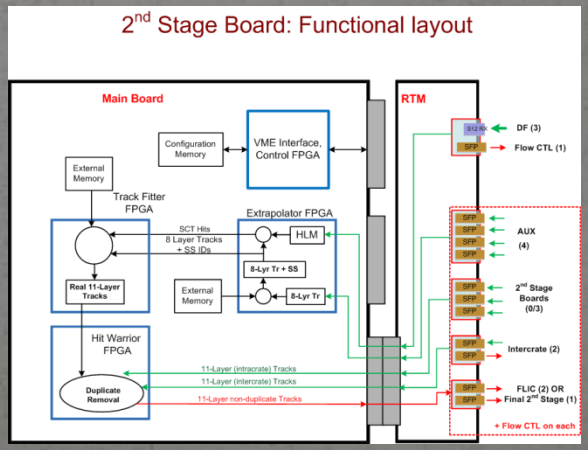




2nd stage board

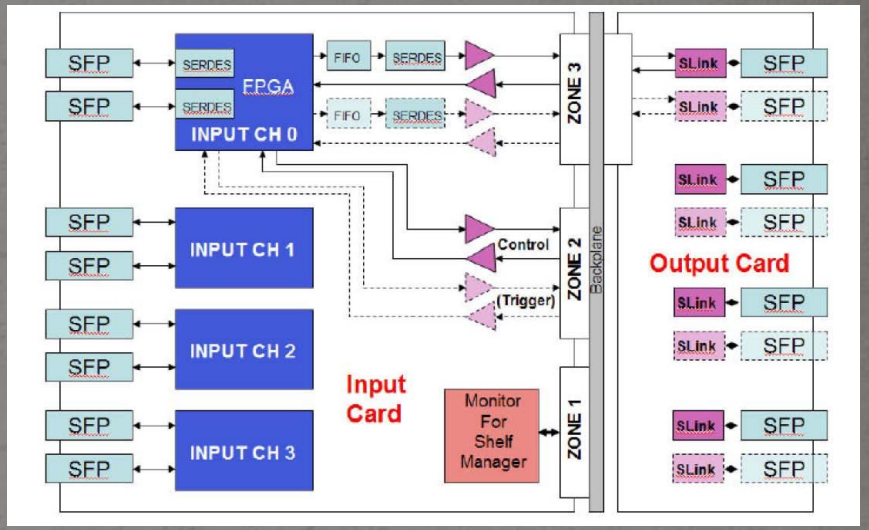
- The AMBoard+AUX card units perform an 8-layer fit
  - This to reduce the pattern bank size
- 2nd stage board attempts to extend the tracks into 3 additional layers
- If additional hits exist they are included
  - Reduces fakes (from 40% to 4%)
  - Improves the fit quality





FTK to Level 2 Interface Crate

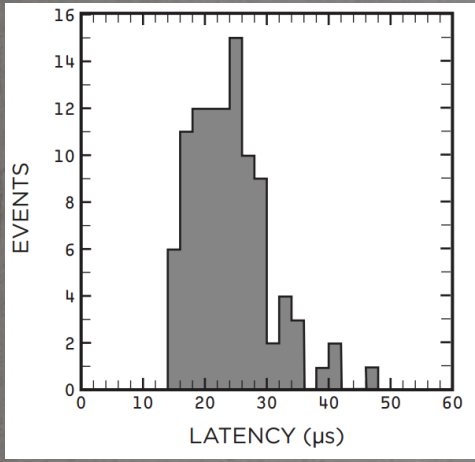
- The FLIC board is responsible for the communication with the ROSes
- Collects the tracks from the 2nd stage boards and changes the format
- Organizes the tracks in a RoI-compatible mode
- Monitoring functionality
- Possibility for local trigger processing under investigation
  - Beam spot, event primary vertex identification, …



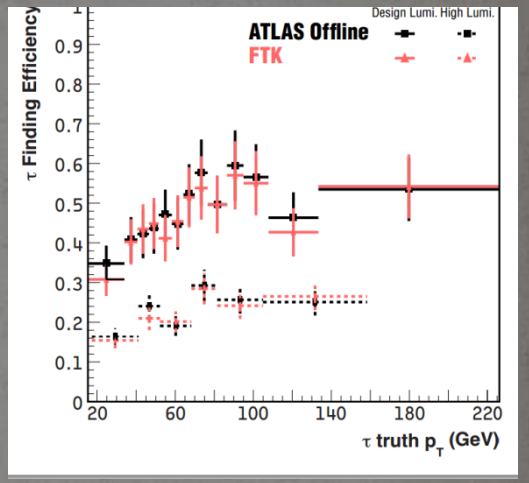
Preliminary dataflow numbers

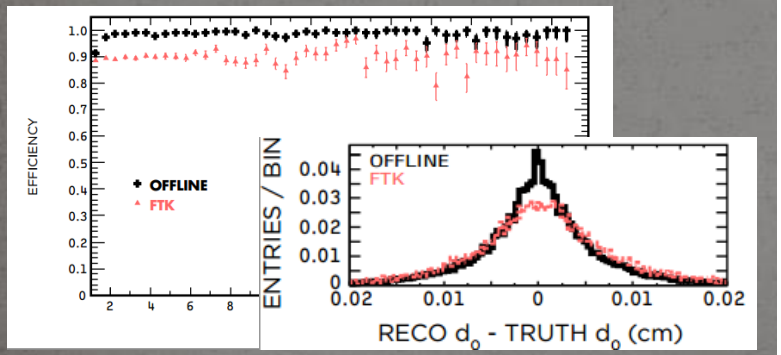
- Detailed emulation of the system used to evaluate the expected dataflow and performance
  - A massive simulation that requires 80 CPU hours for 100 events
  - We put a lot of pressure on grid sites with thousands of slots used
- Typical expected dataflow numbers for 46 pileup events
  - 1000-2000 clusters per tower
  - 1000-2000 roads per AM board
  - 100 kfits per AUX card
  - 100 track segments for the 2nd stage
  - 100-300 output tracks

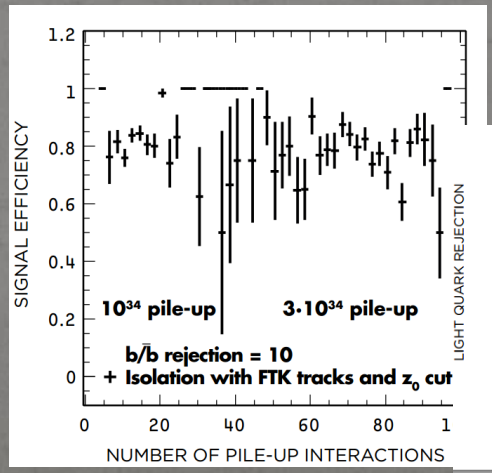
Preliminary results

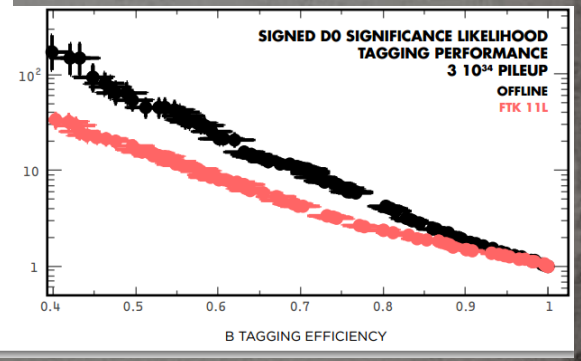


FTK shows a good trade off between execution time (10s of us) and performance.
HLT can spend time on other things.
Quasi-offline results are achieved in many quantities.
Preliminary plots: further refinements can be done at HLT.



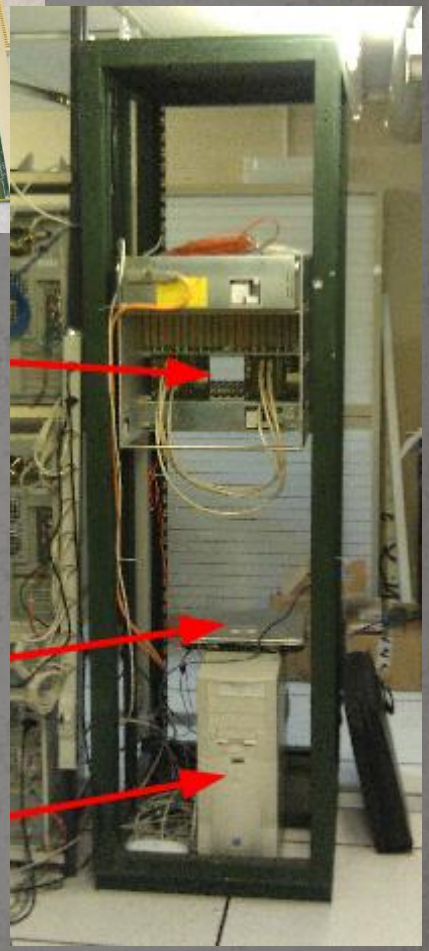






Testing processing units

- A small set of prototype boards will compose the “Vertical Slice”
  - Only 4 towers
  - No data formatter
  - Output consists of roads
    - Fits done offline
- Main goals:
  - Test the integration with the ATLAS DAQ and check the performance with real data
  - Test the high-speed links between AUX and AM board
- Final tests of the boards are on going
  - Installation in an upcoming technical stop

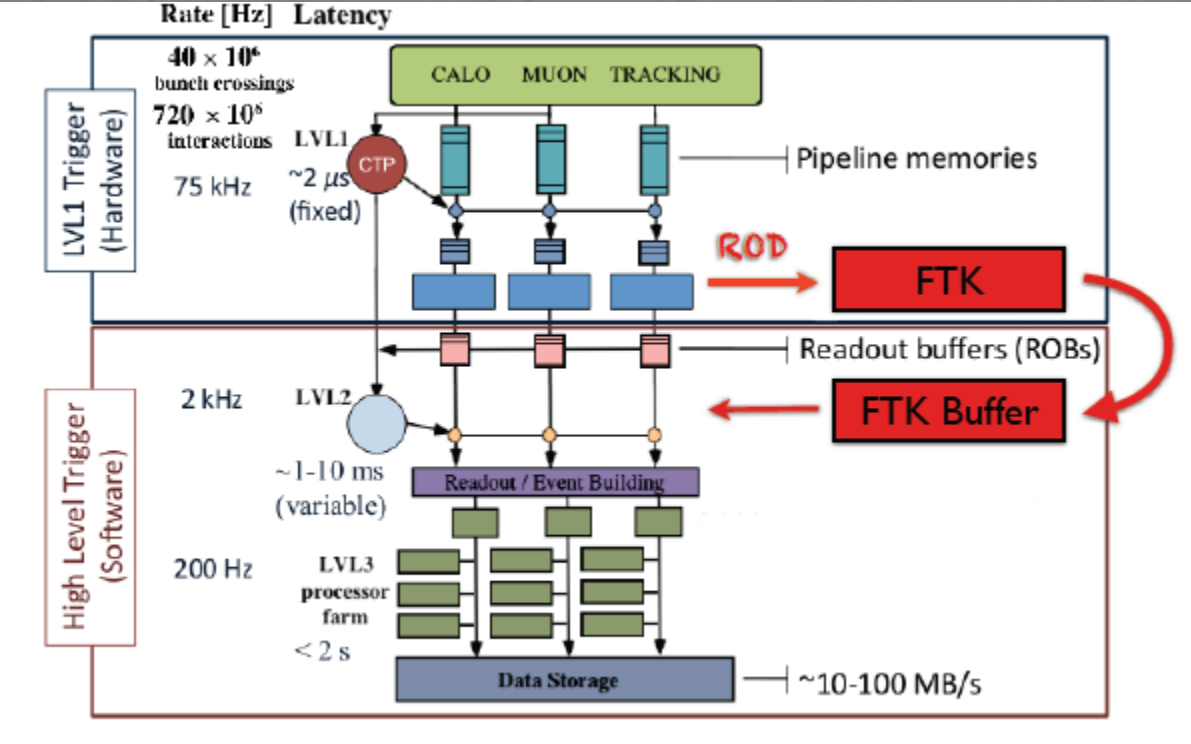


Conclusions

- The logic of the system is mature and well tested using a detailed emulation of the system
- Prototypes at different development stages exist
  - The FTK HOLAs are operating in ATLAS
  - The VS will help to test crucial pieces of the system
- FTK is able to increase the flexibility of the ATLAS trigger
  - A few benchmarks have been identified
  - Improved HLT algorithms using FTK tracks are in progress
- The TDR in spring 2013 and installation in 2014

Backup

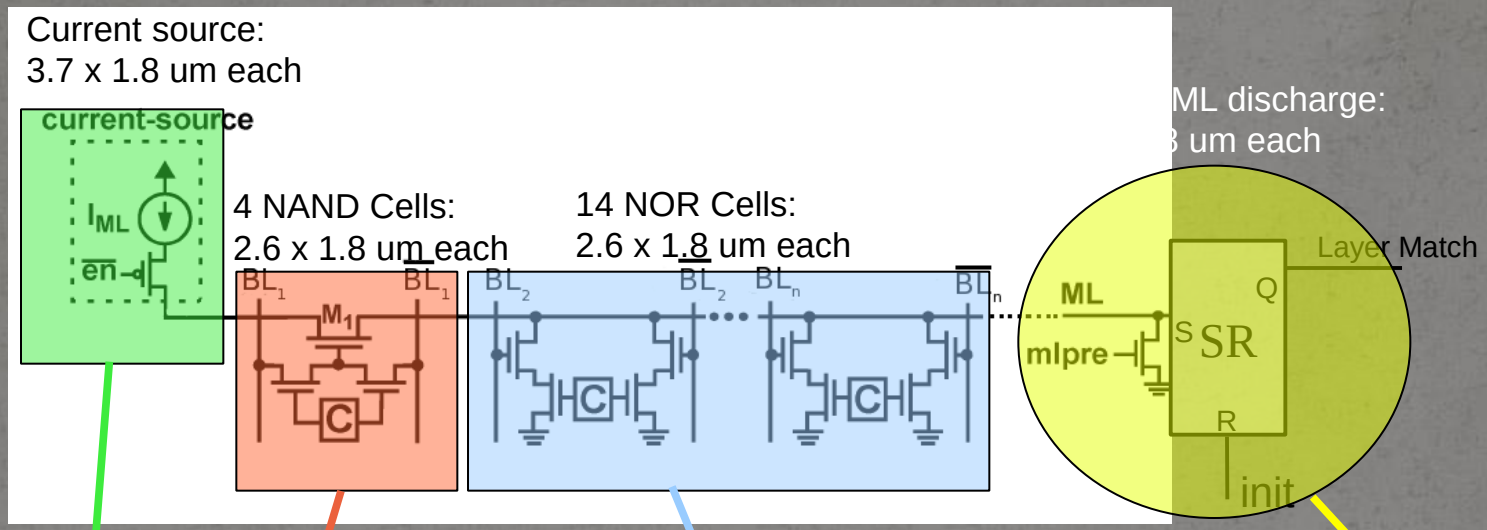
FTK within the ATLAS DAQ



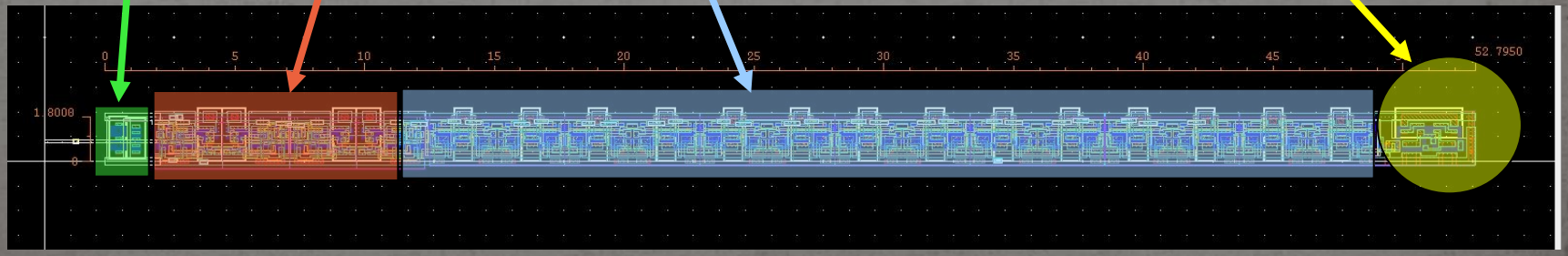
Associative Memory Layer

To save power we have used two different match line driving scheme:

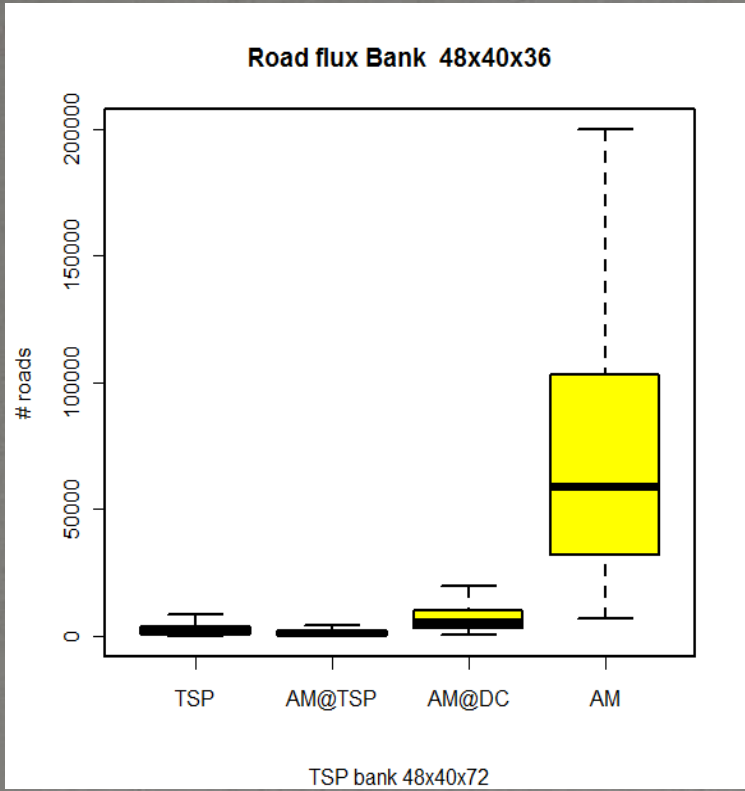
- *Current race scheme (dummy layer timing)*
- *Selective precharge scheme*

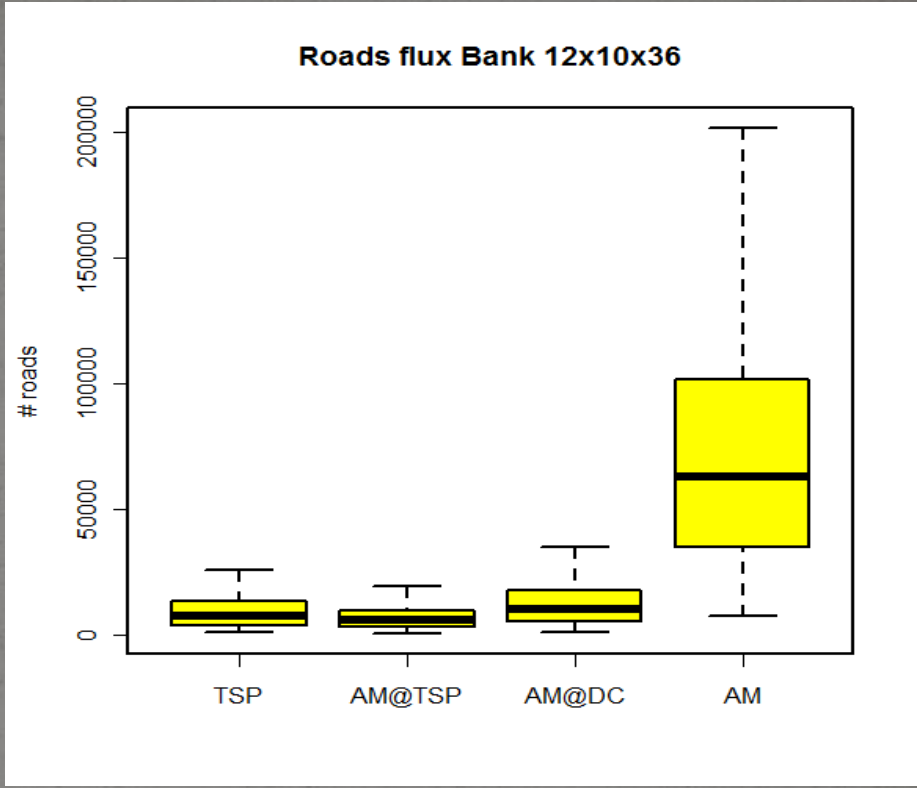


Full Layer layout : w=~53µm X h=1.8 µm



AM performance comparison





- AM size 32 MP
- TSP size 100 MP

- AM size 138 MP
- TSP size 384 MP