Upgraded readout electronics for the ATLAS LAr Calorimeter at the Phase I of LHC

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Abstract

The ATLAS Liquid Argon (LAr) calorimeters produce a total of 182,486 signals which are digitized and processed by the front-end and back-end electronics at every triggered event. In addition, the front-end electronics is summing analog signals to provide coarsely grained energy sums, called trigger towers, to the first-level trigger system, which is optimized for nominal LHC luminosities. However, the pile-up noise expected during the high luminosity phases of LHC will be increased by factors of 3 to 7. An improved spatial granularity of the trigger primitives is therefore proposed in order to improve the identification performance for trigger signatures, like electrons or photons, at high background rejection rates.

The general concept of the upgraded LAr calorimeter readout together with the various electronics components to be developed for such a complex system is presented. The R&D activities and architectural studies undertaken by the ATLAS LAr Calorimeter group are described.

Key words: ATLAS, Liquid Argon Calorimeter, Upgrade, Readout Electronics

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1. Motivation

An upgrade of the LHC to the HL-LHC [1] foresees an increase of the instantaneous luminosities from $10^{34}\text{cm}^{-2}\text{s}^{-1}$ up to $5-7\times10^{34}\text{cm}^{-2}\text{s}^{-1}$ in two phases (I and II) in the years beyond 2018.

A sufficient background rejection demands new readout electronics to provide a finer granularity to the Level-1 trigger system to reduce trigger rates and to improve the resolution for several trigger objects like electrons, photons or jets.

For the first upgrade phase in 2018, new LAr Trigger Digitizer Boards (LTDBs) and LAr Trigger Digitizer and Driver Boards (LTDDBs) are being designed to receive higher granularity signals, digitize them on detector and send them via fast optical links to a new digital processing system (DPS). The DPS applies a digital filtering and identifies significant energy depositions in each trigger channel.

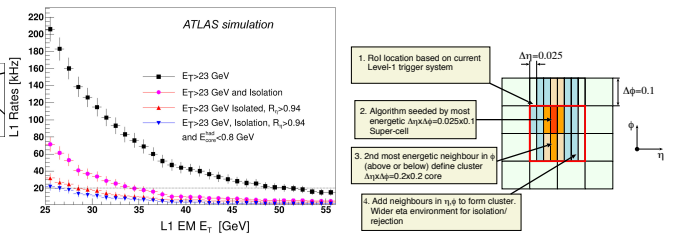

Figure 1: Left: Level-1 trigger rates for different trigger algorithms and energy thresholds; Right: Trigger algorithm based on the most energetic super cell.

The refined trigger primitives are then transmitted to the first level trigger system to extract improved trigger signatures.

Figure 1 shows how an improved readout with higher granularity input to the Level-1 calorimeter triggers allows lower trigger thresholds at a given trigger rate. The main improvement for triggering on electrons and photons is due to a finer lateral resolution of the electromagnetic shower shape.

The study shows that the L1 trigger threshold for single isolated electrons can be reduced from 35 GeV to 28 GeV for a trigger rate fixed at 20 kHz.

2. LAr calorimeter front-end readout

Up to 128 calorimeter channels are mapped to one of 1524 Front End Boards (FEBs). In the electromagnetic calorimeter, each FEB is dedicated to one calorimeter layer (presampler: PS, front: 1, middle: 2, or back: 3) as depicted in figure 2.

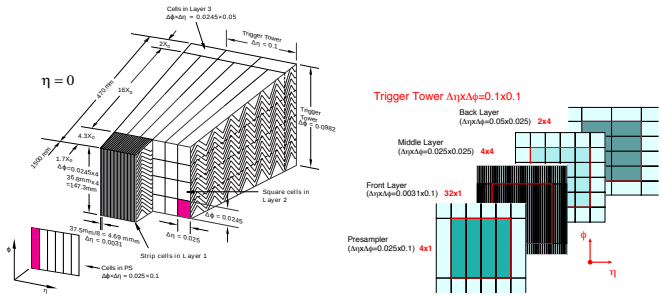

Figure 2: Left: Sketch of a LAr calorimeter barrel module where the different layers and their arrangement in single cells as well as their granularity in η and ϕ; Right: Current Trigger Tower definition: A tower size of $\Delta\eta\times\Delta\phi = 0.1\times0.1$ is chosen for all layers.

Two Layer Sum Boards (LSBs) are mounted onto each FEB, currently providing analog sum signals of a corresponding de-

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tector area of $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ to the Tower Builder Board (TBB) as illustrated in figure 2.

The upgrade foresees an increase of granularity to $\Delta\eta \times \Delta\phi = 0.025 \times 0.1$ in the front and middle layer which requires a replacement of the front and middle layer LSBs. The baseplanes of the Front End Crates will be rebuilt to handle the modified signal routing between LSBs, TBBs and LTDBs.

3. Possible readout architecture for LAr Barrel and Endcap

Figure 3 schematically illustrates the proposal for the Phase I upgrade. The trigger information with increased granularity will be prepared by the FEB and LSB, digitized by the LTDB and LTDDB modules and sent via optical links to the Level-1 calorimeter trigger system. The main data readout by the FEB modules, which is triggered by the Level-1 accept signal of the ATLAS central trigger processor, remains unchanged. Apart from the TBBs all elements to form and process the information for the Level-1 trigger will be re-designed.

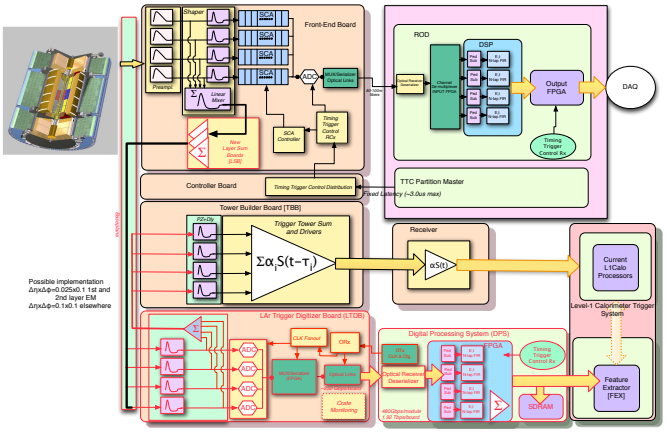

Figure 3: Possible readout architecture for the LAr Barrel and Endcap. Black: current readout modules; Red: new readout modules for Phase I

4. LAr Trigger Digitizer Board

To keep the current architecture of TBBs connected to the existing Level-1 calorimeter trigger receiver, new intermediate LTDBs and LTDDBs are proposed. Their tasks will be to receive fine granularity analog signals from LSBs, to build analog sums as input for the TBBs, to digitize fine granularity analog signals (minimum sampling frequency: 40 MHz) and finally to serialize data and send them off detector using high speed links. Studies on the sampling frequency, dynamic range, effective number of bits, etc. are in progress.

All components are designed to be radiation tolerant. Redundancy of the optical data transmission is foreseen in order to react on unforeseen link failures.

A total bandwidth of 200-300 Gbps is estimated for one LTDB sending off up to 320 signals at 40 MHz.

5. Digital Processing System

Digitized higher granularity data will be received by Digital Processing System boards (DPS). These are planned to be FPGA based processing units which apply digital filtering techniques to convert raw ADC data to fully calibrated energy and transverse energy.

The DPS will mirror the functionality of the existing trigger preprocessor: reception of data using serial optical links, digital signal time alignment, pedestal subtraction and calibration, digital filtering for pile-up suppression to extract E_T contributions, noise thresholding and the immediate serial transmission to the following trigger stage (feature extraction, FEX) by optical links.

The latency budget is the most stringent constraint for the design of the DPS. The time of about 30 bunch-crossings is needed to process the data, including transmission to the calorimeter trigger system.

Data are also locally buffered awaiting a Level-1 decision. On Level-1 accept, data are transmitted to the DAQ for monitoring of the DPS system and functionality, and to the high-level trigger system as input for fast trigger algorithms.

6. R&D activities and architectural studies

Several hardware developments and studies of available commercial hardware are undertaken by the group. Among them:

- A 12 bit ADC in 0.13 μm CMOS technology. The ADC is designed with a 4-bit pipeline and a 8-bit SAR stage, or alternatively as a low latency 12-bit SAR. Radiation tolerance to 10.7 Mrad and 2×10^{14} protons/cm^2 were measured with the first design. Commercial ADCs were tested successfully to about 2.3 Mrad.
- A two-channel Link-on-Chip Serializer at 5-8 Gbps each in 0.25 μm SoS CMOS technology with 8 ns latency was designed and prototyped.
- Prototype DPS modules in ATCA format were tested and operated in ATCA shelf systems. Modern FPGAs (Xilinx Virtex 5/7 and Altera Stratix IV/V) are studied for data processing and serial link performance.
- ATCA specific hardware components are developed, like an Intelligent Platform Management Interface controller in FMC format with Ethernet, USB and JTAG functionality using ARM cortex M3 and Xilinx Spartan 6.

Acknowledgements

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References

[1] The ATLAS Collaboration: *Letter of Intent Phase I Upgrade*, CERN-LHCC-2011-012