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The NA62 Liquid Krypton calorimeter readout module

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ABSTRACT: The NA62 experiment [1] at CERN SPS (Super Proton Synchrotron) accelerator will be focused on precision tests of the Standard Model via studies of ultra-rare decays of charged kaons. The high resolution Liquid Krypton (LKr) calorimeter of the former NA48 experiment [2], together with other detectors, will provide a photon-veto with hermetic coverage from zero out to large angles from the decay region. The old backend electronics [3] does not satisfy the NA62 specifications and the study of a new readout system began in 2008.

This paper presents the Calorimeter REAdout Module (CREAM), an upgrade project for the backend part of the LKr data acquisition chain [3]. The CREAMs will provide 40 MHz sampling of 13248 calorimeter channels, data buffering during the SPS spill, zero suppression, and programmable trigger sums for the experiment trigger processor.

KEYWORDS: Analogue electronic circuits; Data Processing; Digital electronic circuits; Calorimeters

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1 Introduction

The NA62 experiment at CERN aims at studying ultra-rare kaon decays, in particular $K^+ \to \pi^+ \nu\bar{\nu}$. It will be housed in the CERN North Area on a new dedicated high intensity beam line, where 400 GeV/c protons, extracted from the SPS accelerator, will produce a secondary charged hadron beam by impinging on a beryllium target. Since the small signature of the decay process under study, high resolution of the reconstruction of physical quantities and good veto and particle identification capabilities are keys requirements of the experiment.

1.1 NA62 detectors layout

The experimental subsystems are spread along a 170 m long region starting about 100 m downstream of the beryllium target. It consists of several sub-detector systems for a total channel count of about 100 thousand. The fiducial decay region is located in a $\sim$117 m long and a 2.4 m in diameter (in average) vacuum tube. Around and in front of the decay region many detectors will guarantee the hermeticity for photons up to 50 mrad. A straw tube spectrometer, housed in vacuum to reduce multiple scattering, will be devoted to measure the momentum of the charged particle produced in the kaon decay. The identification of the particle type will be done by dedicated detectors. A schematic layout of the experiment is shown in figure 1, more details can be found in [1].

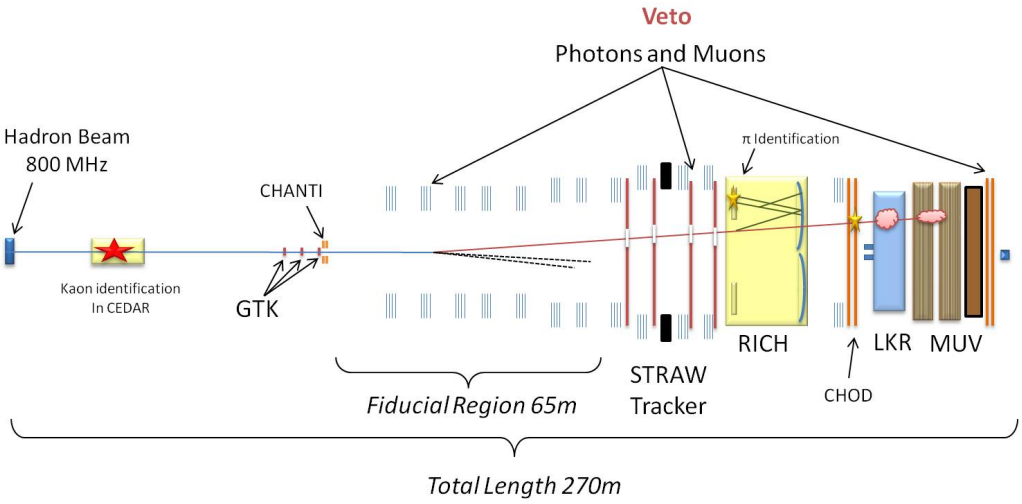

Figure 1. Schematic view of the NA62 experiment sub-detectors.

1.2 NA62 trigger system

The average event rate integrated over the NA62 detectors is about 10 MHz and a very small fraction of these events contains valuable data. A multilevel trigger structure is being implemented in order to reduce this rate to a few kHz.

The first level trigger (called L0) selects events after processing of trigger primitives (prepared on a subsample of data by the few detectors participating in the trigger) on specific hardware. The latency of this processing is fixed, i.e. the L0 accept signal (L0A) occurs a fixed time after the instant of the event seen by the detector, and it can be as high as 10 ms. The L0A signal is distributed to the sub-detector readout electronics via the timing, trigger and control (TTC) links [4].

The next trigger level (called L1) is software based and uses the data kept after L0 of some sub-detectors. The L1 Trigger processor always sends both accept and reject requests to the readout. Subsequent requests are put in Ethernet packets in an asynchronous way. Upon the reception of a L1 request, each sub-detector sends its data to a farm of PCs for subsequent decisions.

The last trigger level (L2) will be based on correlations between different sub-detectors' L1 data. The information, upon which these correlations are determined, will be provided by event-building PC farms. The latency of the L2 trigger is not fixed and can extend into the SPS inter-spill period.

2 LKr calorimeter and its front-end electronics

2.1 Calorimeter

The LKr calorimeter is a quasi-homogeneous electromagnetic calorimeter, which ensures a very good intrinsic energy resolution. It is a key element for vetoing photons from K decays, with the requirement to have a photon detection inefficiency of better than 10^{-5} for energies larger than 35 GeV. In addition, the calorimeter is required to provide trigger signals based on energy deposition to contribute to reducing the L0 trigger rate.

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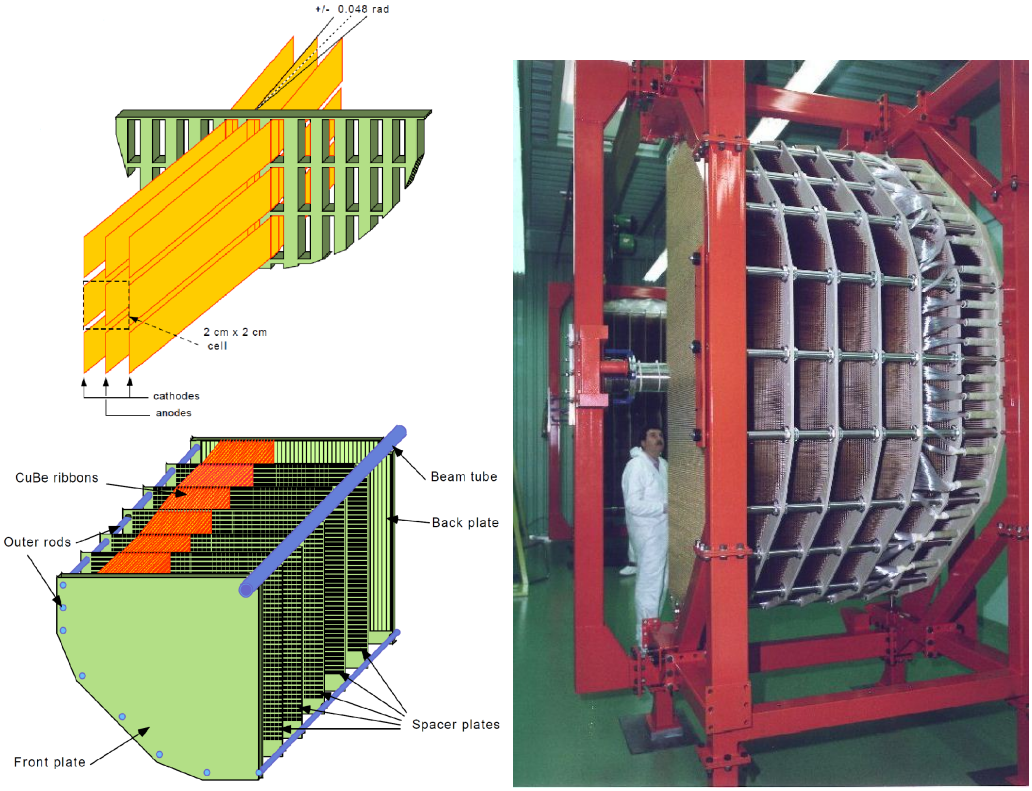

Figure 2. Assembled LKr calorimeter structure and electrode details.

The calorimeter active medium consists of a bath of $\sim 10\,\mathrm{m}^3$ of liquid krypton at 120 K with a total thickness of 125 cm ($\sim$27 radiation lengths) and an octagonally shaped active cross-section of $5.5\,\mathrm{m}^2$. An 8 cm radius vacuum tube goes through the centre of the calorimeter to transport the undecayed beam. Thin copper-beryllium ribbons (of dimensions 40 μm$\times$18 mm$\times$127 cm) stretched between the front and the back of the calorimeter form a tower-structure readout. The 13248 readout cells each have a cross-section of about $2\times2\,\mathrm{cm}^2$ and consist (along the horizontal direction) of a central anode (kept at high voltage) in the middle of two cathodes (kept at the ground). The assembled LKr calorimeter structure and details of the ribbons and spacer plate layout are shown in figure 2.

2.2 Readout electronics

The front-end part of the calorimeter readout was built for the NA48 experiment and comprises two circuits. The initial current is derived from the charge measured by a preamplifier mounted inside the cryostat at liquid Kr temperature and connected to the anode electrode by a blocking capacitor.

The integration time constant of the charge preamplifier is 150 ns. The signal from the preamplifier is transmitted to a combined receiver and differential line driver mounted outside the calorimeter close to the signal feed-through connectors. The receiver amplifies the preamplifier signal and performs a pole-zero cancellation. The signal after pole-zero cancellation has a rise-time of about 20 ns and a fall-time of 2.7 μs. The maximum signal level, 50 GeV, corresponds to $\pm$1 V into 100 Ω at the digitizer electronics input. The required signal to noise ratio is 15000 to 1.

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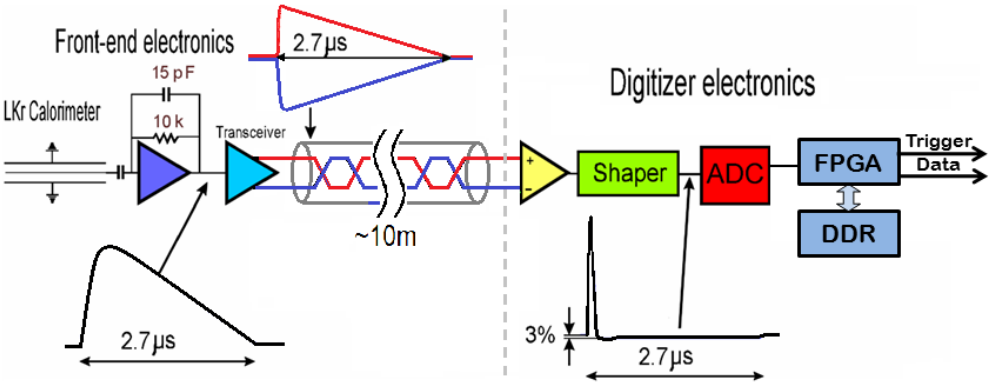

Figure 3. LKr readout chain.

The back-end part of the readout chain, CPD [3], performed final signal shaping and digitization. At the design time in 1995, only a few low cost 10-bit 40 MS/s FADC were available and a custom dynamic range switching ASIC was developed to fulfil the experiment requirements. The maximum event readout rate was 13 kHz.

While two front-end elements remain untouched for NA62, the former back-end digitizer (CPD) performance is not compliant with new requirements and has to be upgraded.

The updated LKr readout chain scheme is sketched in figure 3.

3 CREAM — new back-end digitizer

3.1 Overview

The CREAM is a 1-slot wide VME 6U form-factor module. One module houses 2×16 channels 40 MS/s ADC with at least a 14-bit dynamic range and effective number of bits (ENOB) greater than or equal to 10. The module can run with external and internal clock sources, and the sampling frequency is 40.08 MHz (hereinafter called the 40 MHz clock). The external reference sampling clock will be provided by the TTC links.

The module data processing flow with multiple levels of triggering is illustrated in figure 4 and can be summarised as follows:

- analog inputs, after proper shaping, are continuously digitised using the 40 MHz clock;
- trigger sums are continuously formed in digital form and sent to the L0 trigger logic;
- data are continuously written in a circular buffer waiting for the L0 decision;
- upon receipt of a L0A, the related data, stored a fixed latency time before L0A, are extracted from the circular buffer and stored into another buffer called L0 event buffer, waiting for a possible L1A;
- upon receipt of a L1A, the corresponding data are sent to a PC farm through a gigabit Ethernet port.

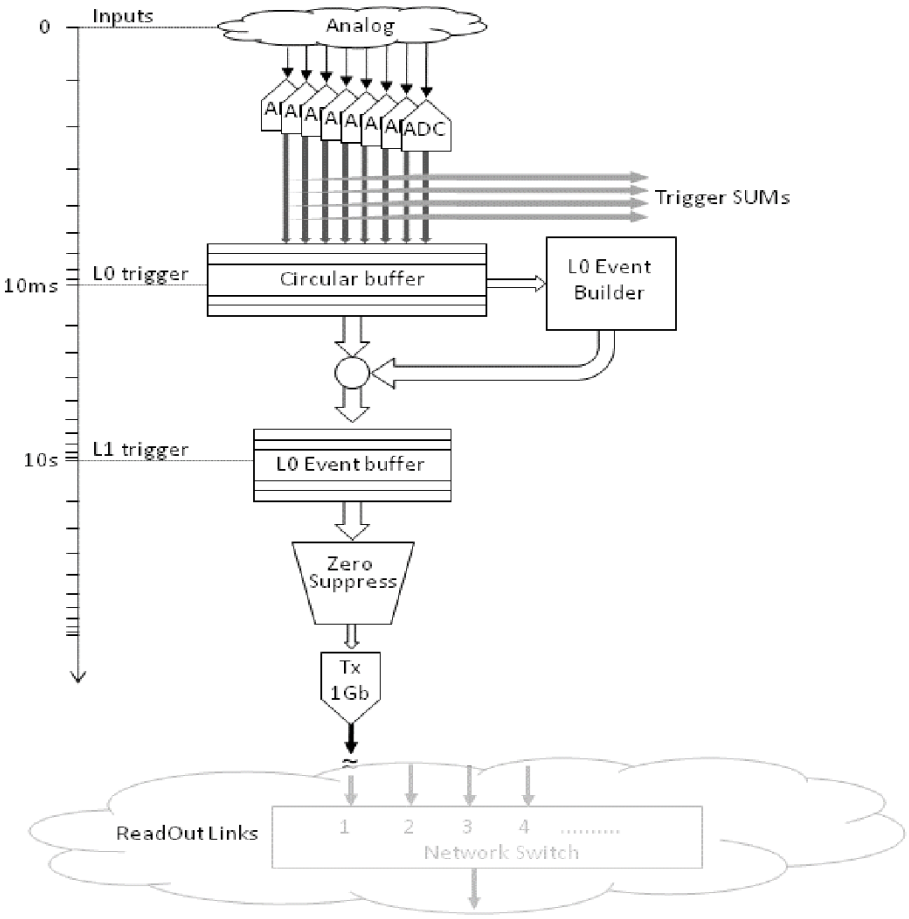

Figure 4. Data processing flow.

The module conforms to the IEEE-1014-1987 and ANSI/VITA 1-1994 [5]. The board hosts the VME P0, P1, and P2 connectors and fits into both VME and VME64 standards. A custom backplane is used to distribute TTC signals via the P0 connectors. Figure 5 shows a block diagram of the module and the following sections detail its different parts.

3.2 Input signal shaping

The signal at the input of the CREAM module has a 20 ns rise-time, a 2.7 μs fall-time and a $\pm$1 V maximum amplitude. Each of the input channels consists of an AC-coupled differential line receiver and a pulse shaper. A 14-bit DAC allows tuning the DC offset of each channel in the range $\pm$1 V in order to correctly adjust the pedestals and to preserve the dynamic range. The signal is shaped before the ADC input into a differential semi-Gaussian signal with a 40 ns rise time and a 70 ns full width at half maximum (FWHM). Thus 8 consecutive, 25 ns spaced samples, cover the entire pulse shape.

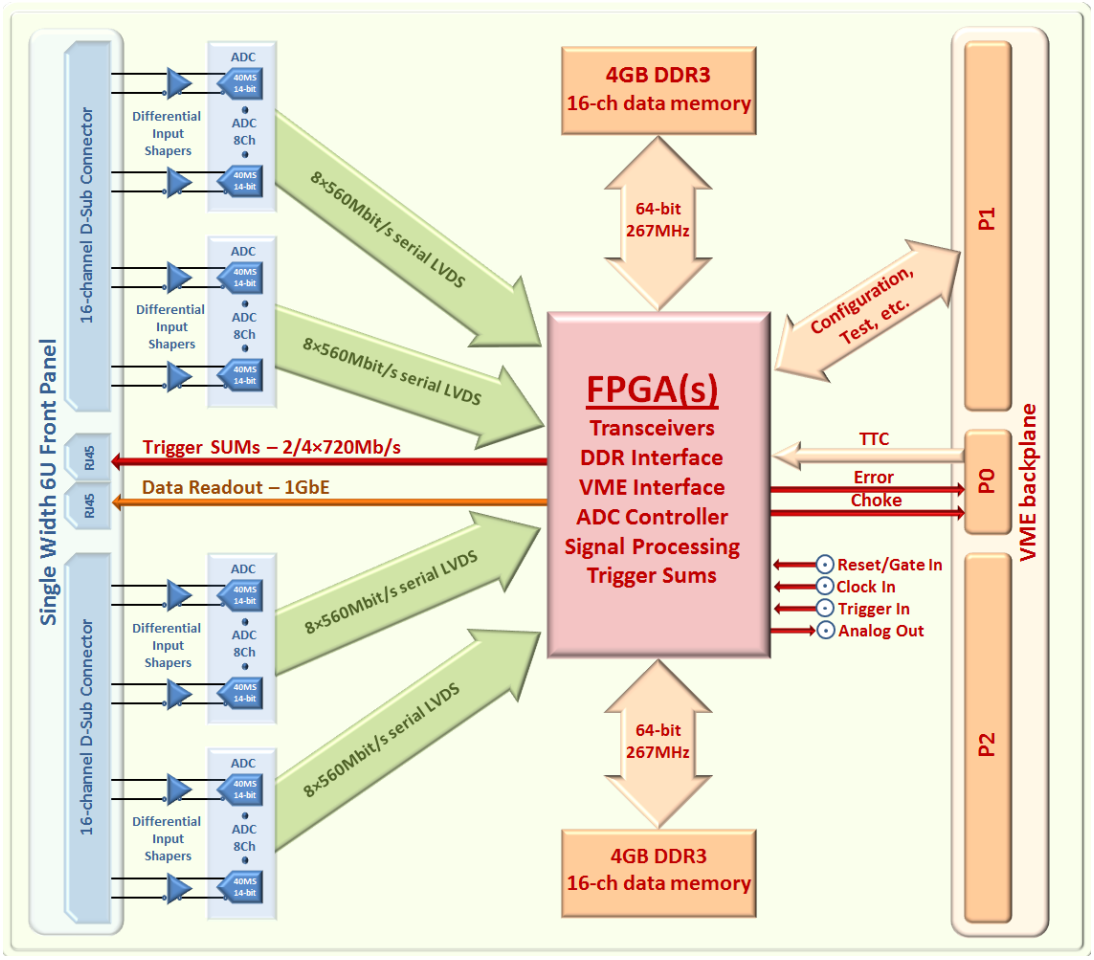

Figure 5. CREAM block diagram.

3.3 ADC

Due to the required performance and total number of channels per board, the AD9252 ADC [6] from Analog Devices is chosen. It is an octal, 14-bit, 50 MSPS ADC with an on-chip sample-and-hold circuit and one serial output data link per channel. The IC has built-in test and control features accessible through a Serial Peripheral Interface (SPI) that includes programmable data pattern generation, along with custom user-defined test patterns. Thus, the test patterns are acquired in the same way as digitised 'analog' inputs, in order to simplify exhaustive analysis of entire acquisition chain. Table 1 gives the main parameters of the analog to digital conversion of the module.

3.4 Data acquisition

The experiment data taking sequence is defined by the SPS accelerator cycle. The accelerator burst time is the data-taking active phase and it can vary in the range of 1–15 s with a period of up to 50 s.

Within the burst, a common time reference is defined by a 31-bit timestamp word, thus covering a maximum time range of about 53.6 s. The burst duration is defined by two commands:

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Table 1. ADC main parameters.

Parameter	**Value**
Resolution	14 bit
Differential Nonlinearity (DNL)	$\leqslant 2$ LSB
Integral Nonlinearity (INL)	$\leqslant 5$ LSB
Crosstalk	$\leqslant -70$ dB
Signal-to-Noise Ratio (SNR), fin=5 MHz	$\geqslant 63$ dB
Effective Number Of Bits (ENOB), fin = 5 MHz	$\geqslant 10$ bit

the start-of-burst and the end-of-burst. The start-of-burst command sets the time stamp to 0. The timestamp associated to each event is defined by the arrival time of the L0A signal. Thus, a unique relationship between the time stamp and the event number is established within each burst.

3.4.1 Digital data processing and trigger modes

The data taking sequence is controlled via the TTC system that drives all timing references. The start-of-burst signal initialises the 31-bit timestamp counter and 32-bit L0ID counter, which are then incremented at each clock cycle and each L0A respectively.

The data streams from all enabled inputs are stored in the circular buffer. The depth of this buffer covers the 10 ms maximum L0 trigger latency, i.e. 800 kB per channel. Upon receipt of the L0A signal, the corresponding data samples (programmable number of samples in the range 4–255 with a default value of 8) are extracted from the circular buffer and stored in the L0 event buffer together with the timestamp counter content at the L0A signal arrival and with a 32-bit L0ID. The L0 event buffer is able to accommodate a 1 MHz L0 average rate during 10 s when 8 samples per L0 event are kept. This requires 2.56 GB memory for 16 channels.

The circular buffers, as well as the L0 event buffers, are implemented in two (one per 16 channels) DDR3 SODIMM modules, with 4 GB storage capacity each.

The events, once written in the L0 event buffer, become available for readout via the Gigabit Ethernet link and/or the VME bus interface, with an optional zero suppression processing. During the memory readout process, the CREAM is still able to store new data in the circular and L0 event buffers. The acquisition process is therefore "dead-time-less", as long as the L0 event buffer is not full.

3.4.2 L0 and L1 readout

The default data taking is initiated by the L1 trigger request. L1 trigger request packets are sent to the module through the Ethernet interface with TCP protocol. One L1 trigger request packet can contain more than one request for data. Events from the same L1 trigger request and with the same Event Builder (EB) destination can be formatted in the same packet to optimize the network bandwidth. The data transmission to the EB is done using TCP or UDP protocol. The readout and the L1 trigger request packets share the same Ethernet link. The "Event data" and "Detector data" formats are presented in figure 6.

For test purposes, it is possible to readout data directly after the L0A signal occurs, but with lower than nominal rate. The data format will be the same as for the L1 readout.

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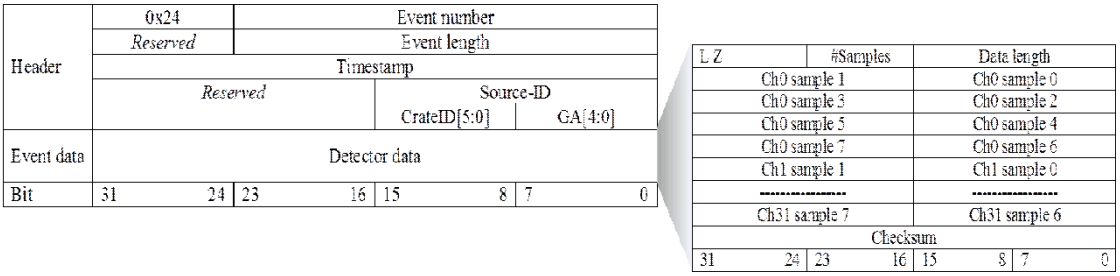

Figure 6. The L1 event and detector data formats.

3.4.3 Data compression

Both the L0 and L1 data copying mechanisms described above will allow reading interesting events without zero suppression, in order to have, at a later stage of the analysis, all the original data available. But, since for each event a large fraction of channels will only contain pedestal counts, a simple zero suppression algorithm to individual channels is foreseen. Channels where the difference between the maximum and the minimum value of the samples is below a predefined value (programmable and possibly different for each channel) will be discarded.

The flexibility of the CREAM architecture could be exploited also for an alternative, triggerless way of readout. In this scheme, continuously digitized data are analyzed by a pipeline process running on the FPGA. This process performs a final calibration and feature extraction with the standard reconstruction algorithms (i.e. digital filters). Precise information on the energy and time of each pulse could be obtained and continuously sent to a cluster of PCs to build complete events.

3.5 Trigger sums outputs

During the data acquisition, digitised signals from the selected channels are summed up to build a Trigger Sum (Super-Cell) to be sent to the LKr L0 trigger system. The sensitive area of the calorimeter forms an octagon, and can be considered a 128×128 cell square grid with the corners missing. The selection of the channels contributing to a particular Super-Cell, as well as the number of Super-Cells formed in a module is programmable.

Before the sums are calculated, all inputs are normalised: each channel pedestal is subtracted from the data and the gain variations are compensated by means of the calibration parameters. The 16-bit sums data are serialised and sent to the L0 trigger processor via standard Ethernet cables. The *embedded clock bit* coding is implemented and high-speed differential cable extender buffers are used.

Up to 4 links are foreseen in order to be able to accommodate up to 4 Super-Cells per CREAM module with effective data rate per link of 720 Mbps.

4 Project status

Due to the huge number of modules ($\sim$450) needed to instrument the LKr readout and the maintenance requirement over the lifetime of the experiment ($\sim$10 years), the decision to sub-contract CREAM development and production to industry has been taken.

A market survey was finished in October 2010 and an invitation to tender was sent out in April 2011. The bids were checked for completeness and compliance with the conditions specified in the invitation to tender documents. CERN management approved the project and the Contract was awarded to CAEN as the lowest bidder conforming to the specification in all respects.

The first prototype delivery is foreseen in July 2012 and these modules will go through rigorous acceptance tests to ensure that design meets the specification and is ready for production. Full production series delivery is planned in July 2013 and entire LKr readout commissioning is foreseen in fall 2013.

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