

## Milestone Report

# Layout of Silicon Micro-Strip Ladders

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# AIDA

Advanced European Infrastructures for Detectors at Accelerators

Seventh Framework Programme, Capacities Specific Programme, Research Infrastructures, Combination of Collaborative Project and Coordination and Support Action

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## MILESTONE 39: LAYOUT OF SILICON MICRO-STRIP LADDERS

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Task 4: Silicon Tracking

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## INTRODUCTION

Within the work package 9 of the EU-funded project Advanced European Infrastructures for Detectors at Accelerators (AIDA), the task 4 (WP9.4) deals with silicon tracking.

Aim of the task is to design and construct “several layers of Silicon micro-strip detectors in front of the calorimeter infrastructure of task 9.5 to provide a precise entry point over a large area”. (as it is formulated in the AIDA contractual documents).

This document specifies the design of the full system, including the silicon sensors with their mechanical support, the possible options of the readout chip and a suitable data acquisition system.

As funding of this task is very limited, almost all hardware components have to be re-used from previous experiments. This is what is called baseline design in the following and fulfils the requirements as specified for the AIDA project fully. However, the involved groups aim for more advanced options and try to develop new silicon detectors, a new readout chip and lightweight carbon-fibre based mechanics. These options are very ambitious and may not be ready within the timescale of the AIDA project. Therefore, they are listed as possible alternative to the baseline design once they have been reached a state to be used for this project instead of the baseline option.

## REQUIREMENTS OF CALORIMETRY

The particle flow paradigm relies on the association of reconstructed charged particle trajectories to energy deposits in the calorimeter. Highly granular calorimeters are being developed to minimize the confusion term that arises from ambiguities due to close-by energy deposits in dense jets. To establish this aspect of the performance of such devices in beam tests a reference entry point must be provided by an independent system. This task provides such an entry point.

The size of the Silicon reference system is chosen in agreement with the beam spot that can be achieved in accelerators at CERN and DESY and by the dimension of showers in the calorimeter prototypes. For electrons (and photons) the lateral development of the shower is governed by the Moliere radius, which is typically of the order of 1 cm. The spot of electron beams can cover the relevant range from several to sub-cm. The performance of electromagnetic calorimeter prototypes can be established with events where multiple particles impinge on the calorimeter in the same event or read-out cycle (relaxing the read-out time to make up for the lack of beam intensity). The lateral development of hadronic showers, on the other hand, depends on the interaction length  $\lambda$ , which is an order of magnitude larger for very dense materials. Simultaneous particles separated by more than approximately 5 cm cannot be achieved in the usual beam infrastructure. For the characterization of hadronic showers one must therefore use overlay techniques, where the response of the calorimeter and Si-based reference system to several particles acquired in different read-out cycles is superposed in software.

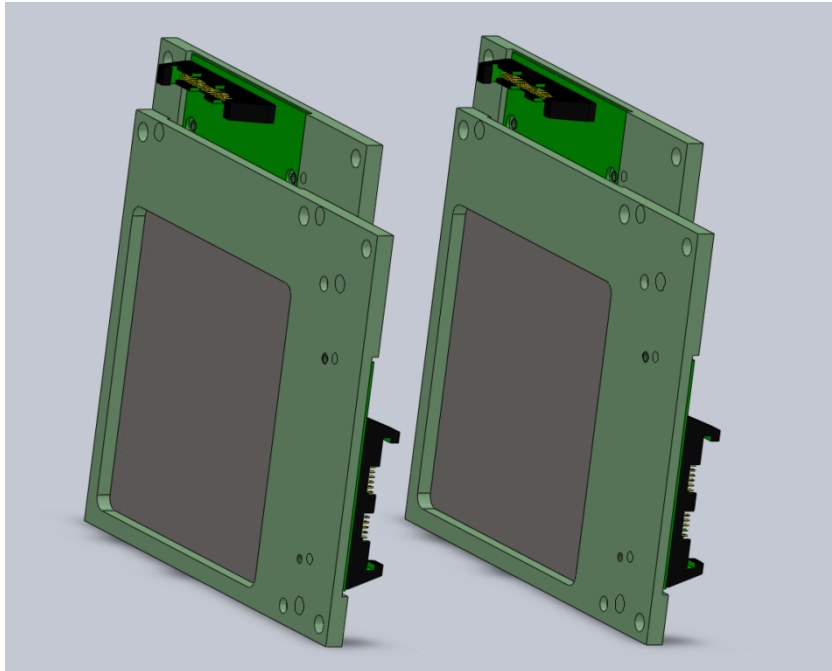
We therefore aim to cover an area of approximately 9 x 9 cm, which can be achieved using a single detector module with silicon strip sensors from a 6-inch wafer production. To facilitate the use of Particle Flow Algorithms (PFA), the calorimeter needs to have a resolution of a few mm. To precisely determine the entry point of the particles into the calorimeter, the silicon sensor resolution of 100  $\mu\text{m}$  is sufficient.

The data acquisition systems of the calorimeter and the silicon sensors must be synchronized to store data from the same event. It has been agreed that the TLU box [1] will be used for this purpose (details see section about DAQ) and that the average trigger rates will be around 1 kHz.

## SYSTEM DESCRIPTION

The baseline system will consist of two planes of (pseudo)-two-dimensional silicon strip sensors with an intrinsic resolution better than 100 microns. Using the impact points on two planes the particle track can be reconstructed giving the required entry point at the calorimeter. This enables the silicon tracking layer to be spatially separated from the calorimeter by a few cm.

To achieve this, four sensors will be used in total, where two of them will be stacked together in a single module.. One sensor in each double-module will be rotated by 90 degrees in respect to the other to get two-dimensional readout with comparable resolution in both dimensions. A 3D rendering of this layout is shown in figure 1.



*Figure 1: Drawing of the two double-module arrangement. Silicon Sensors are shown in gray while the module frame is shown in mid-green. The front-end hybrid housing the readout chips are shown in bright green.*

In the following sections, the different components of the system are described in more detail. The baseline design of each component is described first, followed by possible alternatives for the advanced design.

## ***SILICON SENSORS***

### **Baseline Design**

The baseline option for the silicon sensors is to re-use already existing single sided silicon strip detectors manufactured by Hamamatsu in 2007 for the SiLC collaboration. These sensors have an active area of  $95 \times 95 \text{ mm}^2$  and have 1792 strips with a very narrow pitch of 50 microns. The strips are AC coupled and biased via poly-silicon bias resistors of 20 M $\Omega$ . The full depletion voltage is around 65V (wafer resistivity between 6 and 7 k $\Omega \text{ cm}$ ), so a safe operation voltage at 100V should be foreseen. A picture and schematic drawing of the wafer is shown in figure 2 and figure 3.

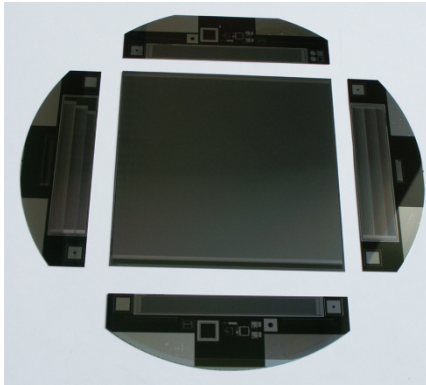


Figure 2: Picture of the wafer developed within the SiLC collaboration in 2007. The large detector in the center will be used for this project.

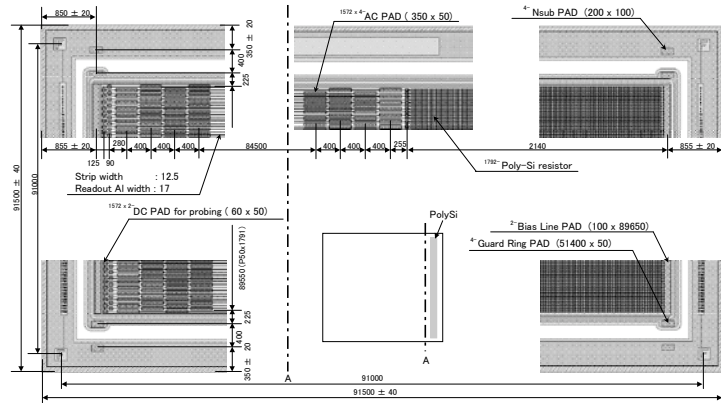


Figure 3: Detailed dimensions of the SiLC sensor

Since the DAQ system cannot handle the large number of strips of a full sensor and because of the relaxed requirements in resolution, only every third strip will be connected to the readout electronics. This results in a configuration with two passive intermediate strips and an effective pitch of  $150\mu\text{m}$ . Previous tests on these sensors [2] have shown that the resolution which can be achieved with this configuration is around 20 microns, although a detailed resolution study has to be done in the future. For this configuration, a pitch adapter from 4 APV chips with a (staggered) pitch of 44 micron to 150 micron strip pitch has to be acquired.

All sensors have been glued onto modules for various applications in the past. Figure 4 and figure 5 show two applications. Before the sensors can be re-used for the AIDA project, they have to be removed from the modules. This is a delicate task with a high risk of damaging the sensors.



Figure 4: LPTPC modules equipped with SiLC sensors.



Figure 5: Telescope test sensors equipped with VAI chip and SiLC sensors.

The disassembly has already been performed on the modules shown in Figure 4 and thanks to the patience and incredible skills of a technician at HEPHY Vienna; six sensors have been successfully recuperated. These sensors have been electrical characterized and five out of the six recuperated sensors show good results and can be used within this task.

## Advanced Design

Several approaches are being pursued to surpass the minimum requirements of the baseline sensors.

One approach is to use strip sensors with resistive strips made of poly-crystalline silicon. The ohmic behaviour acts as voltage divider and enables a position resolution along the strip by taking the charge sharing between the two ends of the strip into account. Different sensors using this technique are currently being developed within this collaboration [3]. Prototype modules as shown in figure 6 have been already tested in a beam test successfully.

Another approach to fabricate new sensors is to qualify a new company as producer for silicon strip detectors. One of the AIDA beneficiary (IPASCR) has a collaboration with a semiconductor company called ON Semi. Within this task, a sample layout has been produced by OEAW (shown in figure 7), which has been evaluated by IPASCR and the company in order to understand the possibility of the fabrication of large reticles on the present production line by the application of stitching technique.

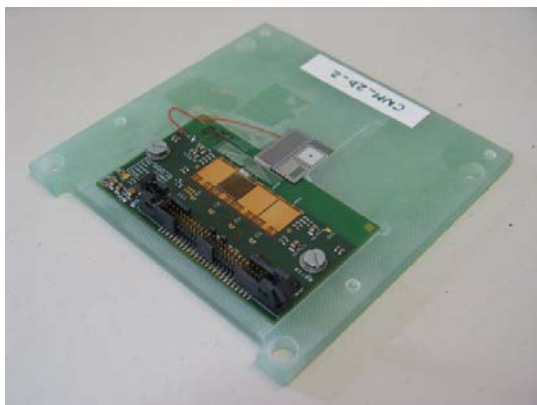


Figure 6: Test-beam module equipped with 2d sensor with resistive strip lines.

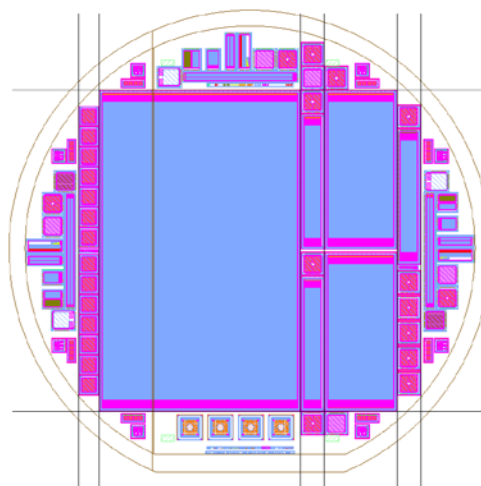


Figure 7: Wafer layout which will be submitted to ON Semi via IPASCR.

## READOUT CHIP

### Baseline Design

For the readout chip, the APV25 chip has been chosen for practical reasons. This chip has been originally developed for the CMS experiment at the LHC. One of the participating institutes (HEPHY) has developed a readout system for the APV25 chip, which will be used for the Belle-II experiment at KEK. It was an obvious choice to make use of this synergy and use the APV25 frontend chip for this project including the Belle-II prototype DAQ system as explained later. Moreover, an existing readout hybrid housing up to four APV25 chips can be used. Only minor modifications are necessary to the hardware in order to be fully compatible with the configuration foreseen within this project.

## Advanced Design

In parallel to the baseline design, one AIDA partner (UB) was evaluating different production technologies for a new readout chip. The TSMC 65nm process has been chosen. Based on this technology, the main characteristics of the preamplifier circuit of the chip have been defined.

## MECHANICS

### Baseline Design

As already shown in figure 1, the modules will consist of a simple plastic frame, onto which the silicon sensor, the hybrid which contains the electronic components and the pitch adapter will be glued. A module with similar dimensions, which has been used for previous beam tests is shown in figure 8. The green frame is made of FR4 (flame redundant 4) and is a fiber-glass reinforced epoxy. This is a stiff material than PVC and allows more precise machining and therefore a better alignment of the components.

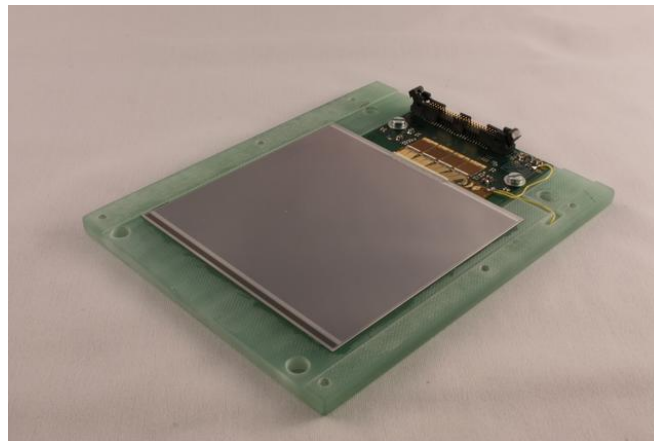


Figure 8: Picture of a beam-test module with FR4 frame.

## Advanced Design

The design of a self-monitoring support structure for the advanced deliverable was performed by IFCA Santander. This structure, made of a Carbon-Fiber-Reinforced Polymer (CFRP) composite, will be equipped with embedded Fiber Bragg Grating (FBG) sensors for temperature and deformation monitoring. Before the production of the first demonstrator, we carried out a FEA mechanical simulation of CFRP support with the goal to determine its expected deformation field. The results from the simulation allowed us to optimise the location of the embedded FBG sensors. Moreover, a collaboration between two partners (ICFA, OEAW) and the Spanish Institute for Aerospace Technology (INTA) in Madrid was defined to manufacture the final CFRP structures.



## DATA ACQUISITION SYSTEM

### Baseline Design

As mentioned in a previous section, the decision to use the APV25 readout chip was strongly influenced by the availability of a suitable data acquisition (DAQ) system. The APVDAQ system, a prototype designed and built in the course of the development of the new Belle-II SVD DAQ system by HEPHY, is readily available within the collaboration. It is able to deliver the requested readout rate of 1 kHz while operating in conjunction with the TLU box to synchronise with DAQ system of the calorimeter. A schematic of the connection of the front-end hybrids housing the readout chips to the backend electronics is shown in figure 9.

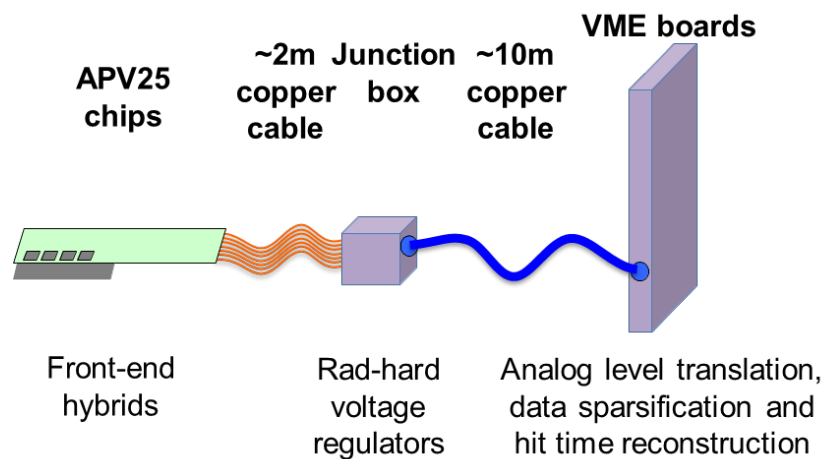


Figure 9: Schematical drawing of the connection between front-end hybrids and electronics.

figure 10 shows the necessary VME boards in more details. It contains a 9U VME crate with a single controller (NECO) and a fan-out unit (SVD3\_Buffer) as well as several FADC modules with built-in processing capabilities. The readout is done via the VME crate to a PC connected via a commercial VME controller. A picture showing these boards in a VME crate can be seen in figure 11.

On the front-end side, which can be located up to 30m away, there are repeater boxes (DOCK) which connect to the front-end hybrids housing the APV readout chips. The system has been adapted to be compatible with the EUDET pixel telescope, which means that the trigger information (including time-stamps) from the TLU is directly included into our VME hardware.

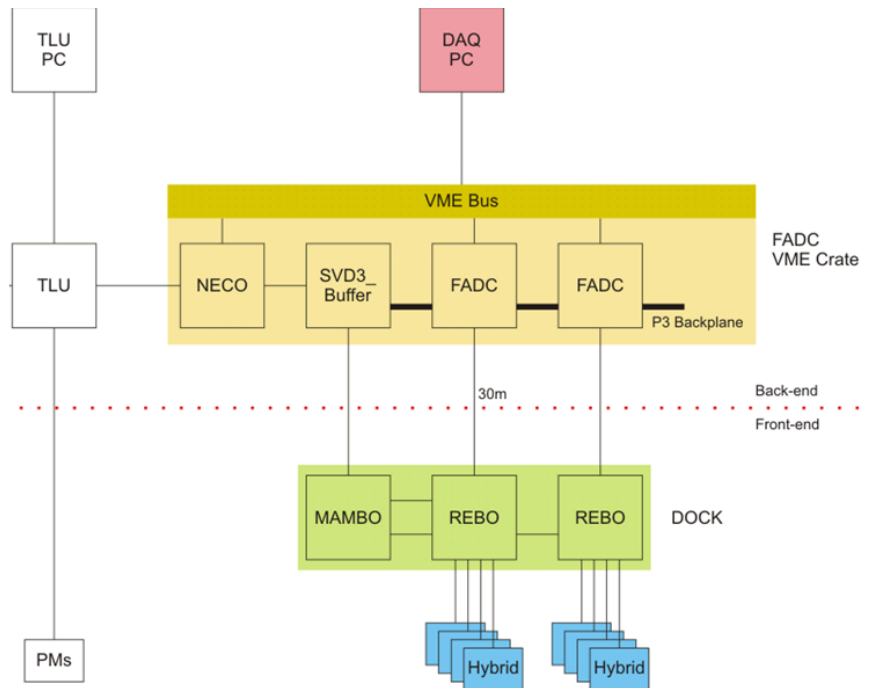


Figure 10: Schematics of the DAQ system.

## Advanced Design

The online DAQ software has been implemented in LabWindows/CVI. This software has already been used for various beam tests in the past and is therefore very stable. The graph shown in figure 12 corresponds to a scope picture (raw data) of six consecutive readout frames of a single APV chip with 128 strip values multiplexed in each frame, where frames are spaced by 25ns. The shaper output waveform (50ns peaking time) of a strip with a particle hit is clearly visible. Multiple samples around the peak have been used to determine the particle timing with an accuracy of a few nanoseconds [4].



Figure 11: Picture of the VME crate housing the DAQ boards: NECO, Buffer and two FADC boards.

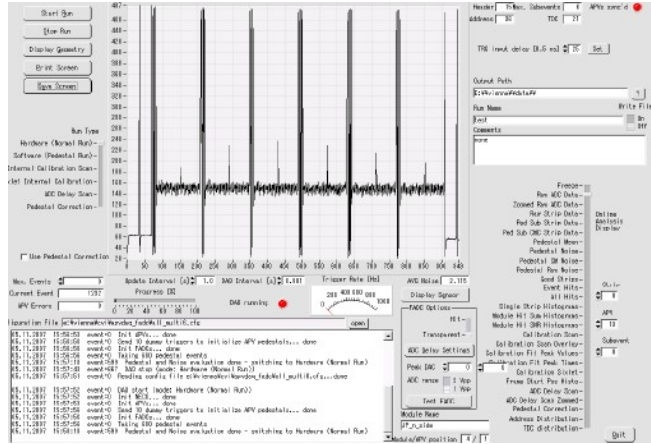


Figure 12: Screenshot of the Windows-based DAQ software. The graph in the center shows the raw APV data of a single chip.

LabWindows/CVI is a Windows-based proprietary software framework by National Instruments. To facilitate the operation, maintenance and extension of the DAQ software, a new portable system called TuxDAQ is currently being developed at HEPHY. It is based on open and free standards like c++/ROOT/Qt and is developed for the Linux operating system [5]. A screenshot of a first alpha version is shown in figure 13.

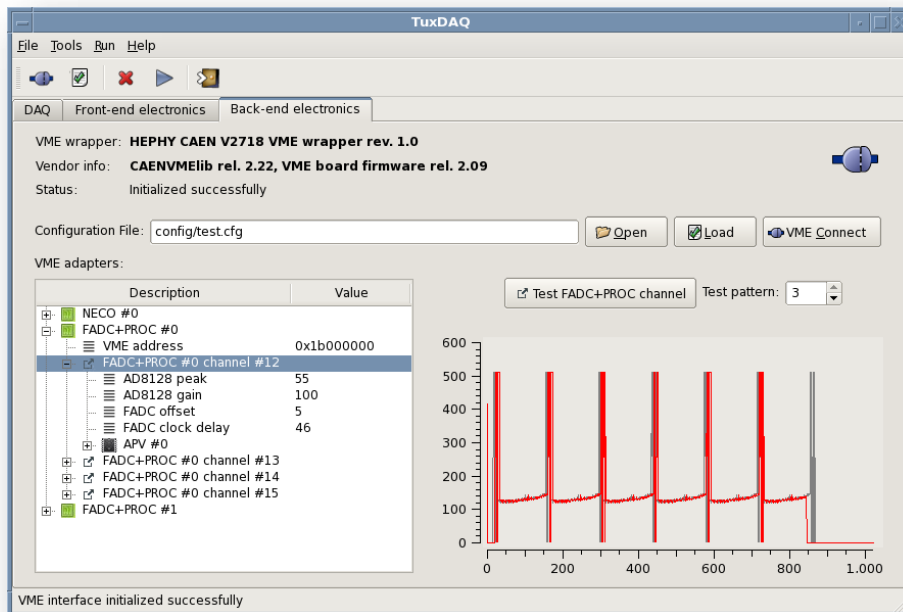


Figure 13: Screenshot of the Linux-based TuxDAQ software.

## **OFFLINE DATA ANALYSIS**

Raw data from the DAQ system is saved to disk in a proprietary binary format. The data can be processed and analyzed using a software framework called HAT provided by HEPHY, which will produce the necessary information for the calorimeter. However, the impact point determined by the silicon tracking infrastructure has to be communicated to the calorimeter DAQ system.

To perform that task an offline conversion of our data to LCIO format is foreseen, which is the same format as used by the DAQ of calorimeter. The final offline data analysis can then access data from both systems and combines the measurements.

## **SCHEDULE FOR BASELINE OPTIONS**

As mentioned earlier, the baseline silicon sensors have been recuperated and are currently being tested. Once this has been completed, the mechanical frames will be built. In parallel, the front-end hybrids will be equipped with APV readout chips and tested afterwards. The design and procurement of the pitch adapters (PAs) connecting the silicon sensors to the chips will happen at the same time as well. After the production of the PAs the modules can be built by mounting all components on the frames and making the electrical connections using wire-bonding.

Barring unexpected delays, the modules should be ready by autumn 2012 in order to be tested in a beam test at CERNs SPS in October/November 2012. There, a first test of the new DAQ software TuxDAQ will be performed. This schedule relies on the availability of pitch adapters which are not yet existing during the time of the writing of this report.

Afterwards, the work is more shifted to software tasks to combine the data with the calorimeter readout using LCIO.

## ACKNOWLEDGEMENTS

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