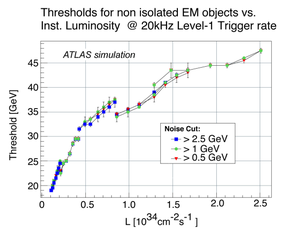
# Upgraded readout electronics for the ATLAS LAr Calorimeter at the Phase I of LHC

TECHNISCHE UNIVERSITÄT DRESDEN

Steffen Stärz,
on behalf of the ATLAS Liquid Argon Calorimeter Group
steffen.staerz@physik.tu-dresden.de

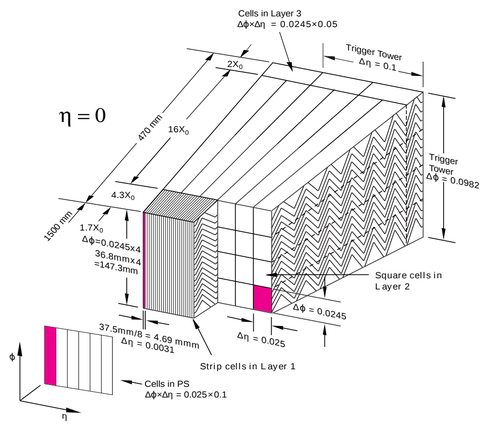
## Motivation




An upgrade of the LHC to the HL-LHC [1] foresees an increase of the instantaneous luminosities from $10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ up to $5-7\times10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ in two phases (I and II) in the years beyond 2020.
A sufficient background rejection demands new readout electronics to provide a finer granularity to the Level-1 trigger system to reduce trigger rates and to improve the resolution for several trigger objects like electrons, photons or jets.

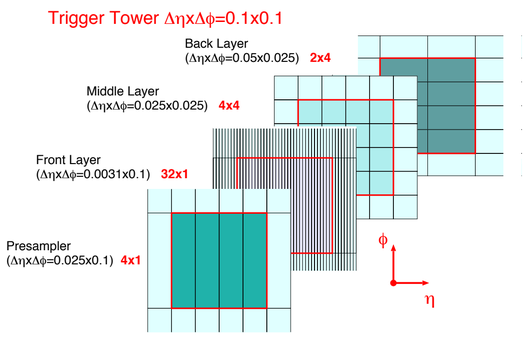
## Front End Boards

Up to 128 calorimeter channels are mapped to one of 1524 Front End Boards (FEBs). Each FEB is dedicated to one calorimeter layer (presampler: PS, front: 1, middle: 2 or back: 3).




## Layer Sum Boards

Two Layer Sum Boards (LSBs) are mounted onto each FEB, currently providing analog sum signals of a corresponding detector area of $\Delta\eta\times\Delta\phi = 0.1\times0.1$ to the Tower Builder Board.



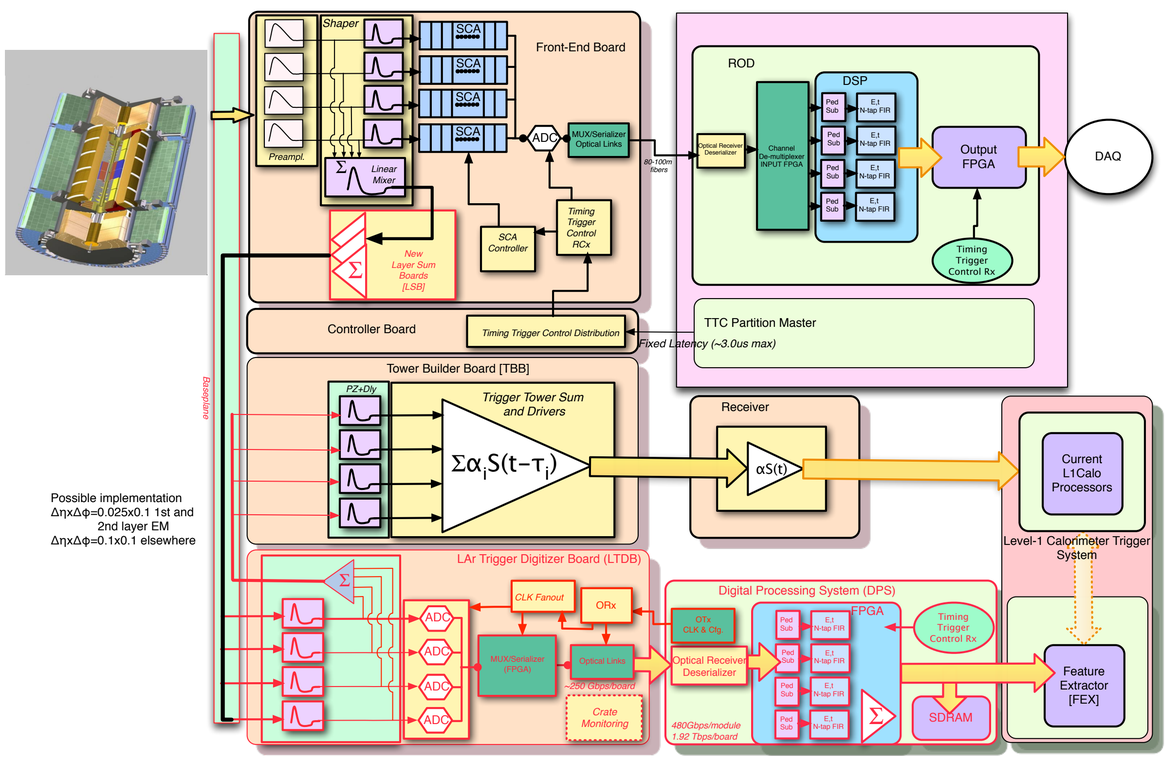

The upgrade foresees an increase of granularity which requires a replacement of the front and middle layer LSBs.

| Layer | Tower sizes $\Delta\eta\times\Delta\phi$ Current | Upgrade |
|---|---|---|
| Presampler | $0.1\times0.1$ | $0.1\times0.1$ |
| Front | $0.1\times0.1$ | $0.025\times0.1$ |
| Middle | $0.1\times0.1$ | $0.025\times0.1$ |
| Back | $0.1\times0.1$ | $0.1\times0.1$ |

The baseplanes of the Front End Crates will be rebuilt to handle the modified signal routing between LSBs, Tower Builder Boards and LAr Trigger Digitizer Boards.

## Possible readout architecture for LAr Barrel and Endcap

The figure schematically illustrates the proposal for the Phase-I upgrade: While the main readout (Front End Boards) is unchanged, apart from the Tower Builder Boards all elements to form and process the information for the Level-1 trigger will be re-designed.




Black: current readout modules; Red: new readout modules for Phase-I

## LAr Trigger Digitizer Board

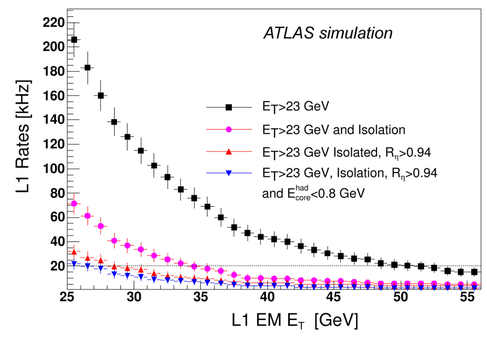
To keep the current architecture of Tower Builder Boards (TBBs), new intermediate LAr Trigger Digitizer Boards (LTDBs) are proposed. Their tasks will be to:

- Receive fine granularity analog signals from LSBs
- Build analog sums as input for the TBBs
- Digitize fine granularity analog signals (minimum sampling frequency: 40 MHz)
- Serialize data and send them off detector using high speed links

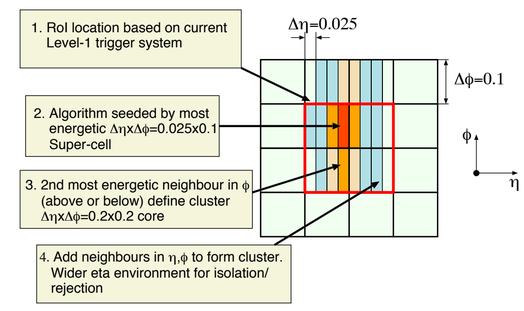
Studies on the sampling frequency, dynamic range, effective number of bits, etc. are in progress.
All components are designed to be radiation tolerant. Redundancy of the optical data transmission is foreseen in order to react on unforeseen link failures.
A total bandwidth of 200-300 Gbps is estimated for one LTDB sending off up to 288 signals at 40 MHz.

## Level-1 calorimeter trigger

The calorimeter trigger selects physics signatures, like high-$p_T$ electrons or photons.




The figure shows how an improved readout with higher granularity input to the Level-1 calorimeter triggers allows lower trigger thresholds at a given trigger rate. The main improvement for triggering on electrons and photons is due to a finer lateral resolution of the electromagnetic shower shape.




The trigger is seeded by the most energetic super-cell and the electromagnetic shower is reconstructed by adding the energy of neighboring cells.

## Digital Processing System

Digitized higher granularity data will be received by Digital Processing System boards (DPS).
FPGA-based processing units apply digital filtering techniques to convert raw ADC data to fully calibrated energy and transverse energy.
The DPS will mirror the functionality of the existing Preprocessor:

- Reception of optical signals,
- Digital signal time alignment,
- Pedestal subtraction and calibration,
- Digital filtering for pile-up suppression to extract $E_T$ contributions,
- Noise thresholding,
- Immediate serial transmission to the following trigger stage (feature extraction, FEX) by optical links.

The latency budget is the most stringent constraint for the design of the DPS.
Data are also locally buffered awaiting a Level-1 decision. On Level-1 accept, data are transmitted to the DAQ and/or the high-level trigger system.

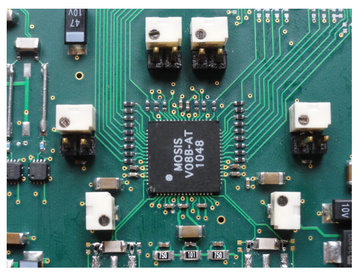
## References

[1] The ATLAS Collaboration: *Letter of Intent Phase I Upgrade*, CERN-LHCC-2011-012

## Acknowledgements

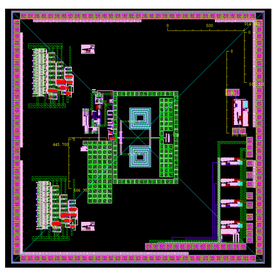
supported by: Bundesministerium für Bildung und Forschung; PHYSICS AT THE TERA SCALE Helmholtz Alliance

## 12 bit ADC



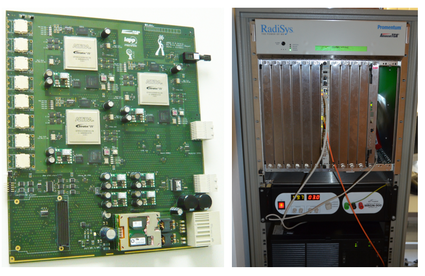

- 4-bit pipeline ADC + 8 bit SAR
- Radiation tolerance: 10.7 MRad, $2\times10^{34}$ protons/cm$^2$
- 0.13 $\mu$m CMOS technology

## Link-on-Chip Serializer



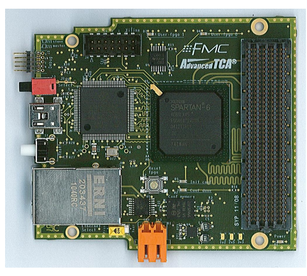
- LOCs2 two-channel prototype, each at 8 Gbps
- 0.25 $\mu$m SoS CMOS technology
- Latency: 8 ns

## DPS ATCA Prototype




- Prototype processing boards with Xilinx Virtex-5/7 and Altera Stratix IV/V
- ATCA shelf system with dual-star backplane and 10-Gb-Ethernet switch

## ATCA IPM Interface




- Intelligent Platform Management Interface (IPMI) in FMC format
- ARM cortex M3, Xilinx Spartan 6
- Ethernet, USB, JTAG functionality