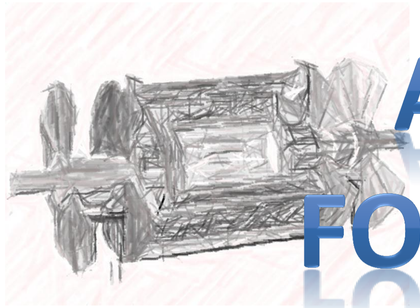

A FAST HARDWARE TRACKER FOR THE ATLAS TRIGGER SYSTEM

Volpi G. [2,4] ; Andreani A.[13,14]; Andreazza A. [13,14]; Citterio M. [13]; Favareto A. [13,14] ; Liberali V. [13,14] ; Meroni C. 13 ; Riva M. [13,14] ; Sabatini F. [13] ; Stabile A. [13, 14] ; Annovi A. [2] ; Beretta M. [2] ; Castegnaro A. [2] ; Bevacqua V. [1,3] ; Crescioli F. [1,3] ; Francesco Cervigni ; Dell'Orso M. [1,3] ; Giannetti P. [1] ; Magalotti D. ; Piendibene M. [1,3] ; Chiara Roda [1,3] ; Sacco I. ; Tripiccione R. [7] ; Fabbri L. [15,16] ; Franchini M. [15,16] ; Giorgi F. [15] ; Giannuzzi F. [15,16] ; Lasagni F. [15,16] ; Sbarra C. [15] ; Valentinetti S. [15,16] ; Villa M. [15,16] ; Zoccoli A. [15,16] ; Lanza A.[11] ; Negri A.[12, 11] ; Vercesi V. [11] ; Bogdan M.[4] ; Boveia A. [4] ; Canelli F. [4,10] ; Cheng Y. [4] ; Dunford M. [4] ; Ho Ling Li [4] ; Kapliy A. [4] ; Kim Y. K. [4,10] ; Melachrinos C. [4] ; Shochet M. [4] ; Tang F. [4] ; Tang Jian [4] ; Tuggle J. [4] ; Tompkins, L. [4] ; Webster J. [4] ; Atkinson, Markus [5] ; Cavaliere, Viviana [5] ; Chang, Philip [5] ; Kasten M. [5] ; McCarn A. [5] ; Neubauer M. [5] ; Hoff J. [10] ; Liu T. [10] ; Jamieson Olsen [10] ; Penning B. [4,10] ; Todri A. [10] ; Wu J. [10] ; Drake G. [6] ; Proudfoot J. [6] ; Zhang J. [6] ; Blair R. [6] ; Anderson J. [6] ; Auerbach B. [6] ; Blazey G. [17] ; Kimura N. [8] ; Yorita K. [8] ; Sakurai Y.[8] ; Mitani T. [8] ; Iizawa T. [8]

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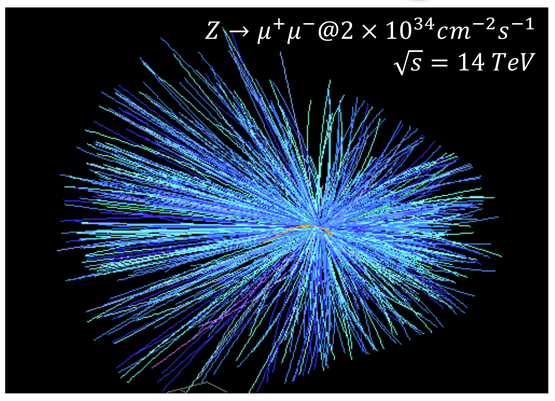
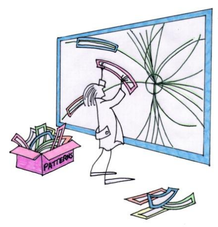
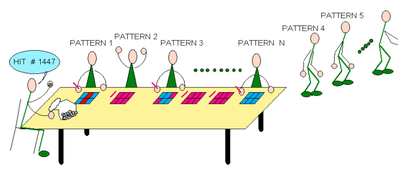
The Challenge



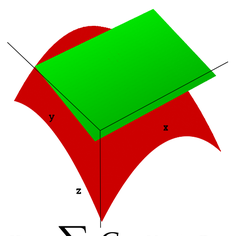
The discovery potential of the ATLAS detector depends on the ability to identify rare events and reject background from pile-up of multiple p-p interactions.
Tracking information is proved as a powerful tool for early rejection of pile-up background but the amount of information can be overwhelming.

The Idea





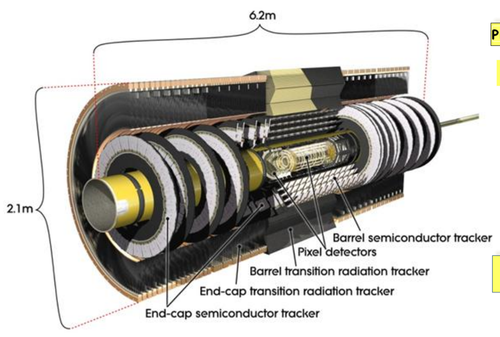
The pattern matching can be parallelized with the use of special CAM-like memories, using parallel match-lines that compare the incoming hits with a list of physical pre-calculated patterns, using a coarser resolution

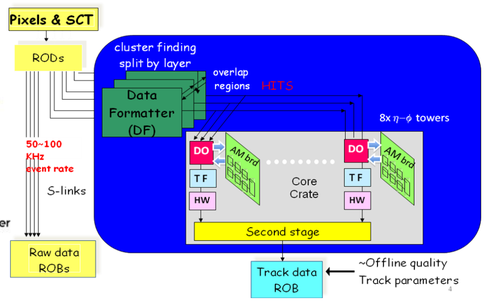


$$p_i = \sum_j C_{ij} \cdot x_j + q_i$$

In each found road the parameters of the track candidates can be calculated exploiting linearized constraints between the hit positions and helix parameters.
Naturally parallel approach, well suited for modern FPGAs

The ATLAS FTK Processor

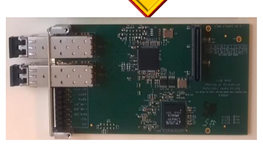




The Fast Tracker processor is designed to read all the silicon layers of the Inner Detector (ID)

- 3 pixel layers, 4 when IBL will be included
- 4 paired SCT layers
- 64 independent η-ϕ towers, 512 parallel processing units

Dual-output HOLA



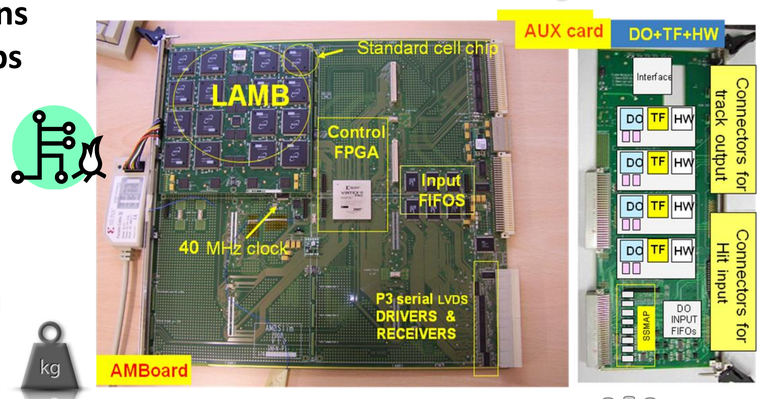
The dual-output HOLA cards provide a copy of the ROD data to 2 channels (DAQ and FTK).
Separated data-flow control for each channel
Production completed:

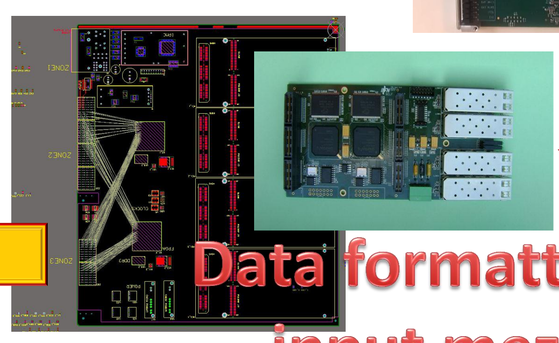
- **All 270 cards produced and tested**
  - **only 2 failures, both fixed**
- **32 already installed within the DAQ system at and ready to test a small scale demonstrator (the Vertical Slice, VS) this summer**

Associative memory Board

The AM board contains 4 LAMB cards, 32 chips each.
Demanding:

- **100 A at 1.2 V**
- **4 48V→1.2V DC-DC converters**
- **About 2 kg for each AM board**

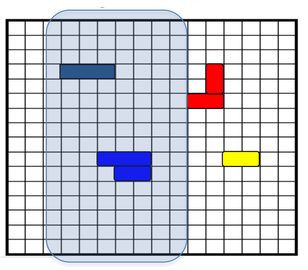




Data formatter and input mezzanine

The data coming from the HOLA cards are clustered by the FTK_IM card.
The Data Formatter (DF) has the responsibility to subdivide the data and send them to the appropriate η-ϕ tower.
Advanced design stage based on ATCA crate with full-mesh backplane

FPGA clustering algorithm



A specific clustering algorithm implemented in FPGA was developed. First prototype ready to be tested in the vertical slice this summer.

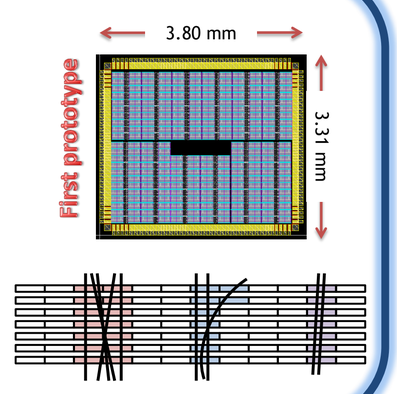
Auxiliary card

The AUX card receives and stores the full resolution clusters from the DF and sends for each cluster a coarser resolution position, the super-strip, to the AM for the pattern matching.
Only 8 out of 11 silicon tracking layers are used at this stage.
The card receives back the matched roads, restores the full resolution, and uses the linear calculation to discard roads without good candidate tracks.

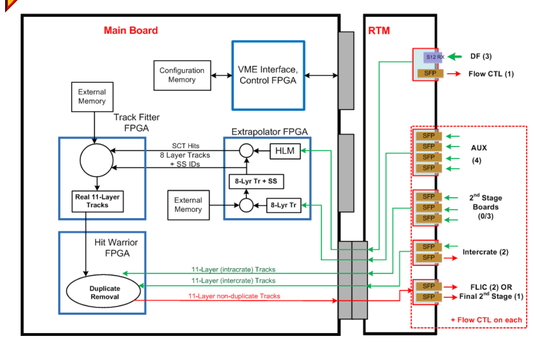
The AMChip04

New custom cell AM chip specifically designed for FTK

- *80K/patterns per chip*
- *65 nm technology*
- *8-layer architecture*
- *Alternate AND and NOR cells to reduce the power*
- *Variable resolution to optimize efficiency and number of patterns*



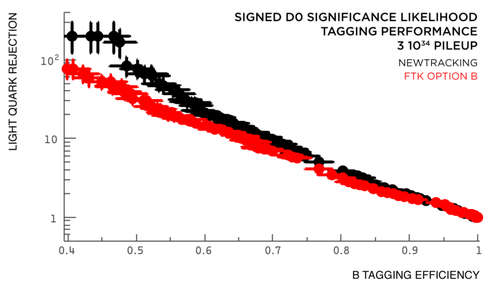
2nd stage board

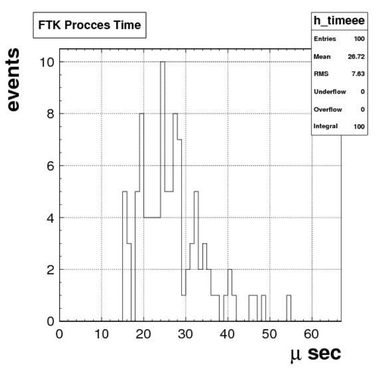


The 2nd stage board combines the track candidates found by the AUX card with the additional 3 SCT layers not used in the pattern matching.
It improves the track quality and rejects a large number of fake tracks: from 40% of the 8 layers to less than 4%.

The FTK performance at high luminosity

- The FTK processor is an hardware system based on an extreme parallelization, composed by 512 processing units
- It performs tracking in the whole detector.
- It is capable of operating after each Level 1 accept, up to 100 KHz, with a latency less than $100\ \mu s$ at luminosity up to $3 \times 10^{34} cm^{-2} s^{-1}$.





- The FTK track quality allows to implementation of complex algorithms such as B- or tau-tagging, with quality comparable to the use of offline tracks.
- Integration with existing algorithms under study.
- Providing a complete list of tracks at the start of the HLT processing can allow use of algorithms that require full event tracking at high rate.
- The FTK frees up HLT resources allowing more complicated algorithms

FTK to Level 2 Interface Crate

The FLIC boards are in a dual-star ATCA crate to allow for additional trigger functionality. Each board is responsible for:

- **Collecting the output from all the 2nd stage boards, both track parameters and hits**
- **ROS communication**
- **Monitoring functions**
- **Possibility to integrate local trigger algorithms or functions**