Online tracking applications of the general purpose EDRO Board

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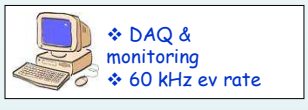
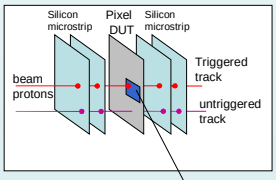
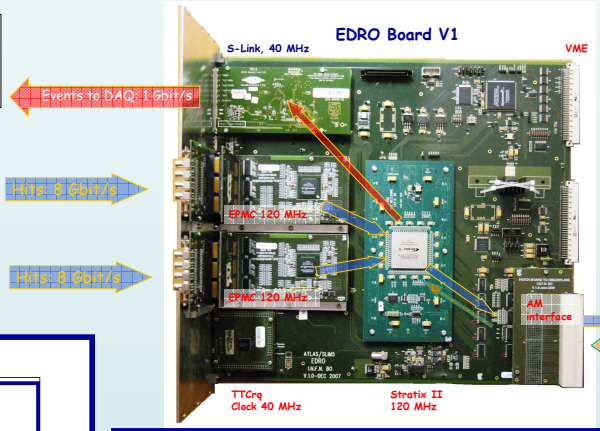
The capability to perform extremely **fast track reconstruction online** is becoming more and more important for the LHC upgrade as well as the next generation of HEP experiments, where the expected instantaneous luminosities (in excess of 10^{34} $cm^{-2}s^{-1}$) and the very low signal/background ratio ask for fast and clean identification of the main characteristics of interesting events. The **Slim5 R&D** project [1] studied different aspects of fast and high-precision tracking in dedicated hardware: data-push silicon sensors, **high bandwidth DAQ systems and Associative Memories** (AM) for fast track identification [1, 2]. The central element of the development system is a **high traffic board, called EDRO** (Event Dispatch and Read Out), capable of collecting and processing digital data with an **input rate of 16 Gbps**. The input hits, suitably formatted or clusterized, are sent to an AM board sending back candidate tracks, which are identified at a rate of **40 MHz**. The EDRO board is then able to deliver triggers and formatted events for further processing. The EDRO-AM system was first exploited on beam tests [1] where it was able to process **events at a maximum rate of 2.5 MHz**, trigger events with identified tracks (maximum latency 1 us) and provide a clean sample of events with well reconstructed tracks. The flexibility of the EDRO-board design allows it to be coupled with completely different hit sources. In the **ATLAS** project called **FTK Vertical Slice**, the **EDRO board** receives level 1 triggered data from a part of the inner detector and, together with an AM board, **identifies tracks for a possible use by the second level trigger processors** [3,4].

EDRO Characteristics

- 1 master board+5 mezzanines
- 4-6 FPGAs: full programmability
- LVDS I/O for high bandwidth
- 8 optical link for I/O on FTK mezzanine
- Main FPGA aggregated I/O: 40 Gbit/s
- 6 Mbit RAM, 120 MHz clock
- Fast Output to DAQ, monitoring via VME



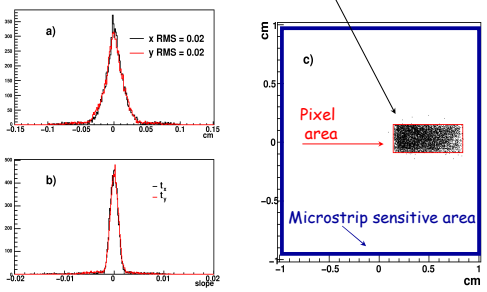




Slim5 testbeam tracks

- 4 double sided microstrip planes used as beam telescope read out with data-push front end chips
- 1 pixel sensor used as DUT
- 12 GeV proton beam at PS
- Input data rate: 4 Gbit/s
- track trigger latency < 780 ns

AM Trigger performances
Fake trigger rate <2x10^{-6} (95% cl)
Up to 95% of triggered events have at least one offline track

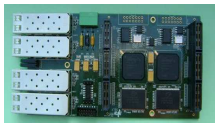


Comparison between offline track parameters and road parameters evaluated at the first microstrip layers.

- difference between coordinates (black: x, red: y);
- difference in track slopes (black: x slope, red: y slope);
- impact point of the tracks having a match with an AM track at the z coordinate of the MAPS chip.

EDRO Version 2 and FTK_IM

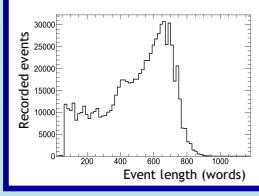
- 512 MB memory on board added
- new Input Mezzanine for FTK applications
- 4 dual 1.3 gbps links
- 2 spartan FPGAs
- 32 MB ram on board

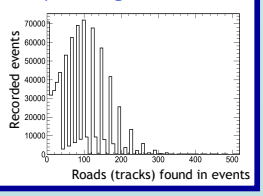


FTK Tests in labs

HW simulation → EDRO → AM → EDRO → DAQ

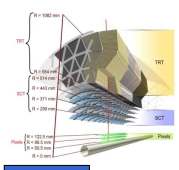
- Mean event: 500 words with 90 roads
- Latency < 3 us, HW efficiency >99%
- DAQ Rate: 30-60 kHz depending on evt size



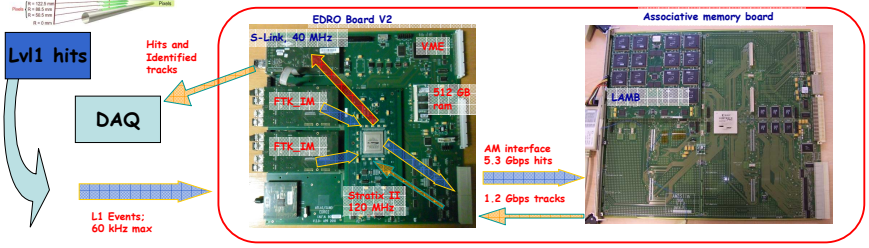


The EDRO board in the Vertical Slice FTK Test

ATLAS Inner detector



- Access to Inner detector data after Lvl 1 trigger
- Clusterization of data in FTK_IM
- Switching of data in EDRO; shipping to AM
- Packaging of HITS and TRACKS for Lvl 2 processing



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