



Control and Operation of the LHCb Readout Boards using Embedded Microcontrollers and the PVSSII SCADA System

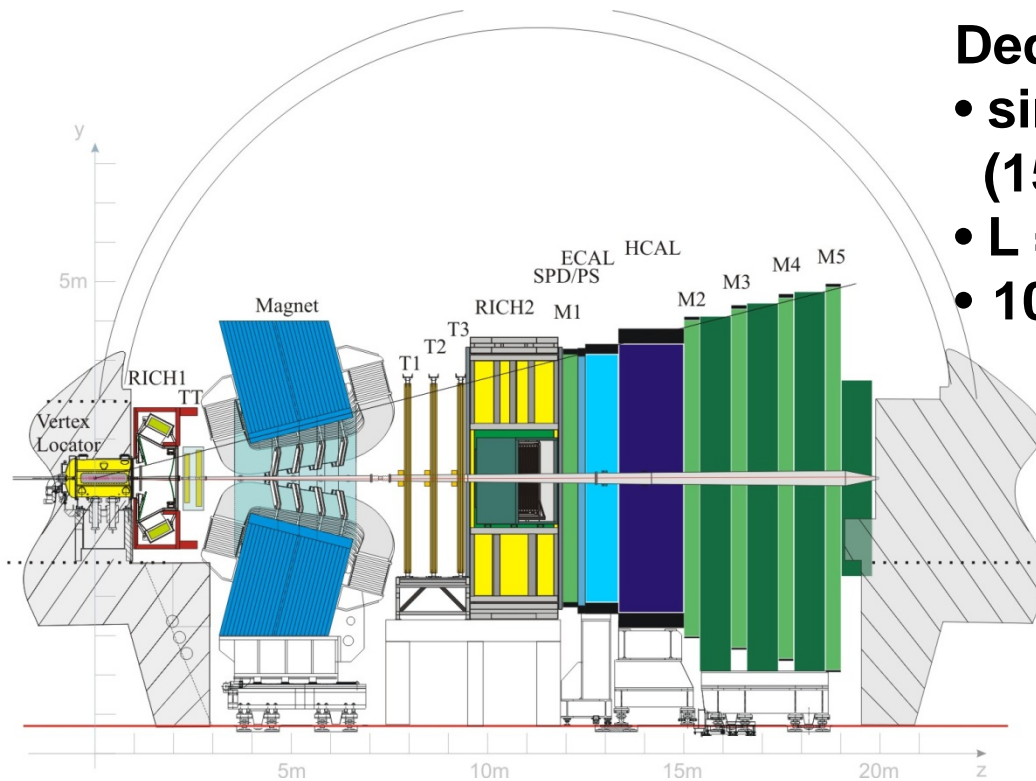
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on behalf of the
LHCb Online Group
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The LHCb experiment



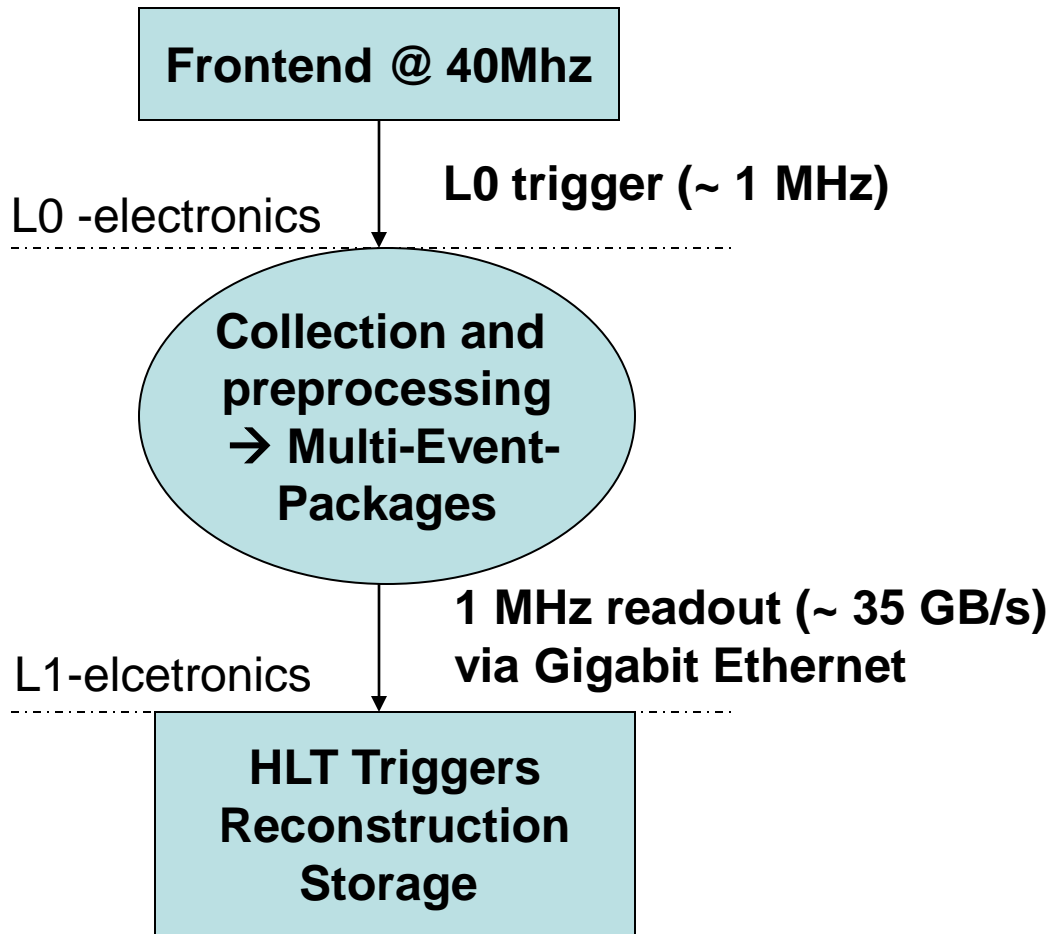
Dedicated to 'B-physics':

- single arm forward spectrometer (15 - 300 mrad)
- $L = 2 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$ ($\sim 1 \text{ evt/bx}$)
- 10^{12} bb-pairs ($\sim 100 \text{ kHz}$)

fraction of interest just 10^{-5}
→ efficient trigger necessary to enrich the data sample!
(implemented in 2 levels)

- Ten sub-detectors with approx. 1.1 million readout channels in total
- average total event size (at average occupancy) is 35 kB (after ZS)

Trigger and DAQ system



L0 trigger:
4 μ s fixed latency
time synchronized to FE-chips
(Calos, Muon & Pile-up Veto)

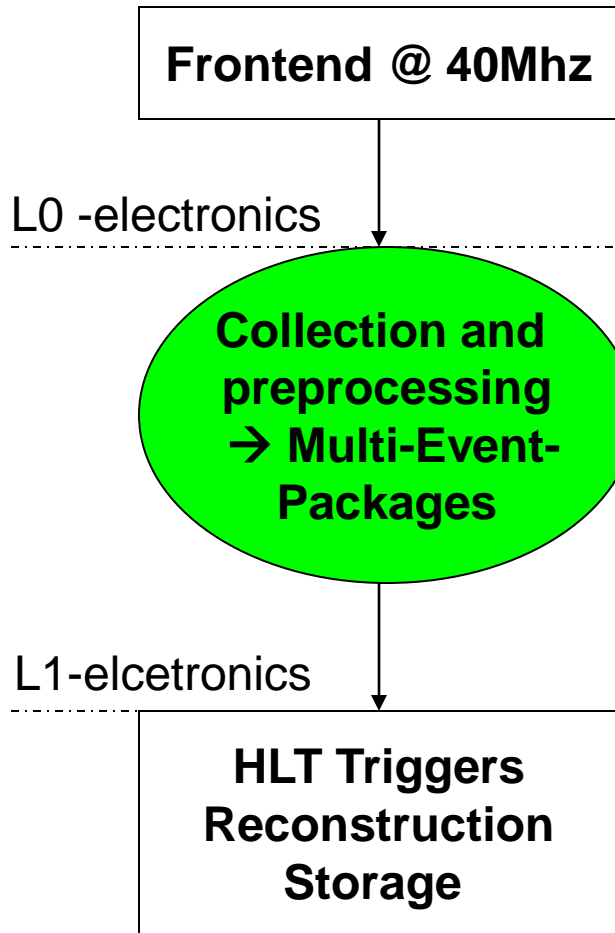
Push-protocol supposing that following stage has enough buffer.
Centralized throttle via TFC-system (synchronous).

HLT trigger:
~2kHz to tape

PC-Farm

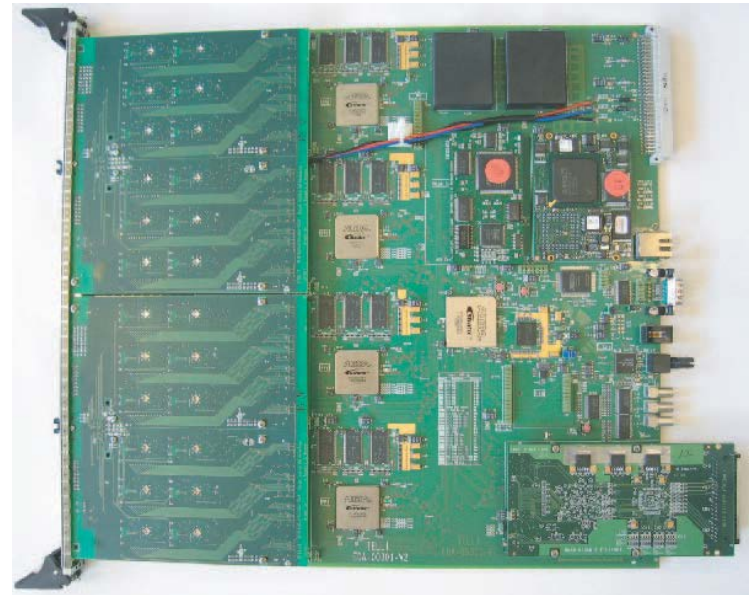
Raw Data: 70 MB/s

TELL1 - board



Trigger Electronics Level 1 board:

- FPGA based
- adopted by almost all subdetectors
- in total ~300 boards
- with ~400 registers & memory blocks

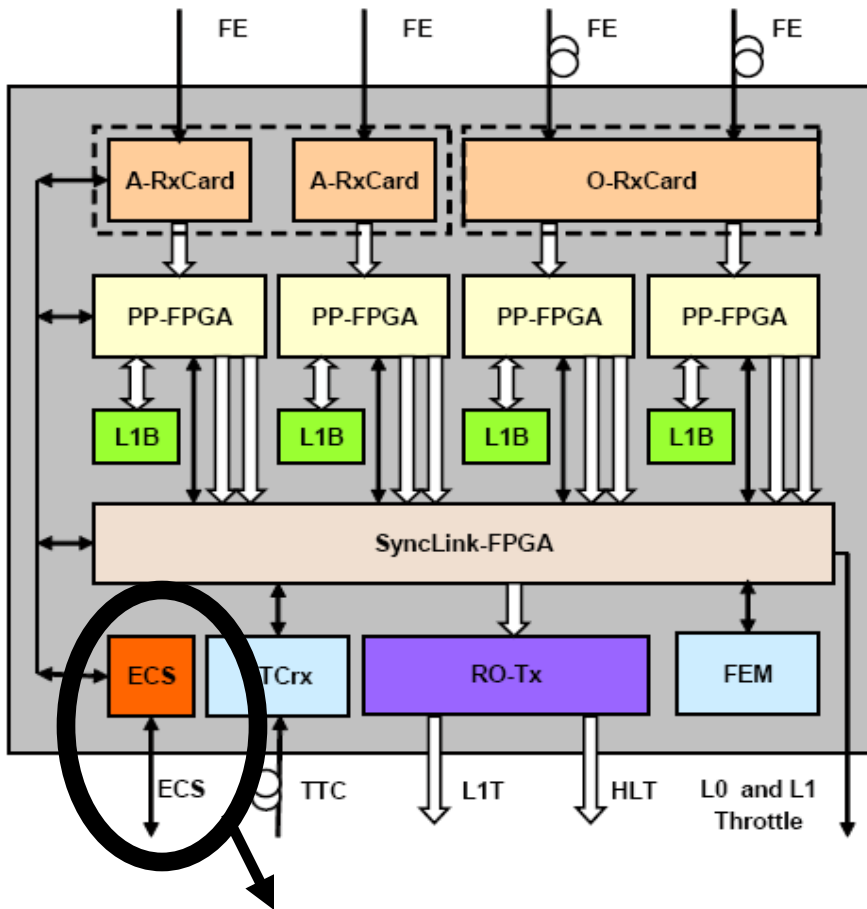


PC-Farm

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IEEE NSS – San Diego 2006

TELL1 - board



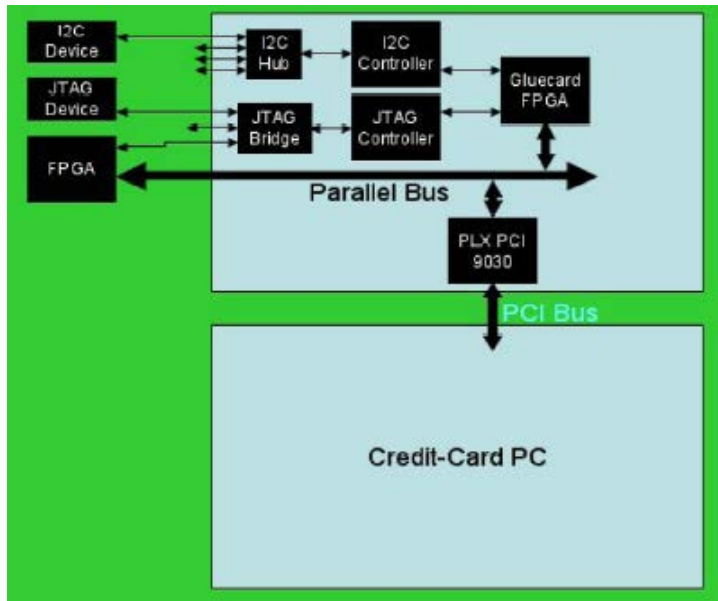
- ADC conversion
- Synchronisation, reordering, pedestal subtraction
- Common mode suppression
- Zero Suppression
- Multi Event Packing
- IP Framing
- Gigabit Ethernet Link

- ECS interface via creditcard sized PC connected to 10/100 Ethernet
- Controls network separated from Data network
- isolated access path → robustness

Credit Card PC

4" - SM520PCX (Digitallogic) CCPC:

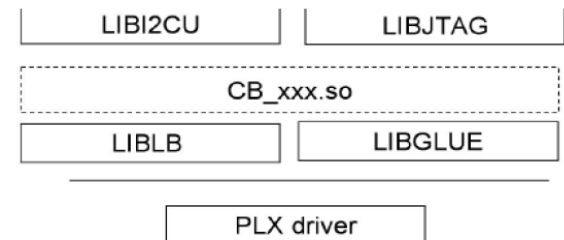
- i486 compatible microcontroller (AMD ELAN 520)
- Linux Kernel at 133 MHz
- reading from local bus 20 MB/s
- filesystem shared over server



Access to board via gluecard over a PLX PCI9030 bridge:

Parallel bus (8/16/32), 3 JTAG chains (2 MHz), 4 I²C lines and 9 GPIO lines

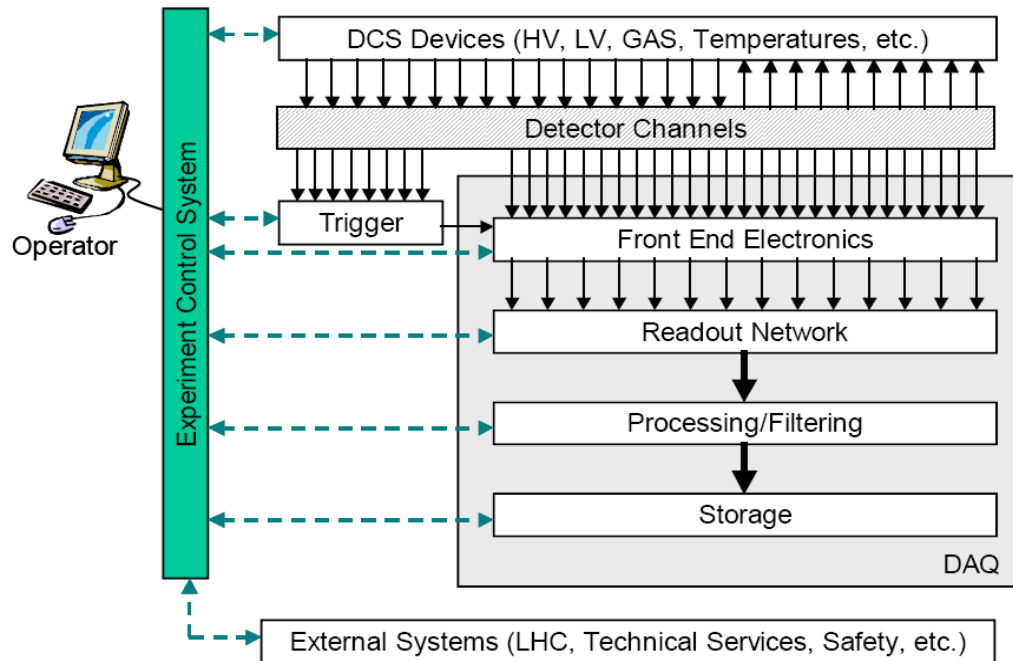
low level libraries under SLC4 (maintenance)



Experiment Control System

A uniform and homogenous control system based on the 'Joint Controls Project' (JCOP) framework - tailored for LHCb needs:

- eases development as well as operation
- distributed and scalable system
- coherent interfaces



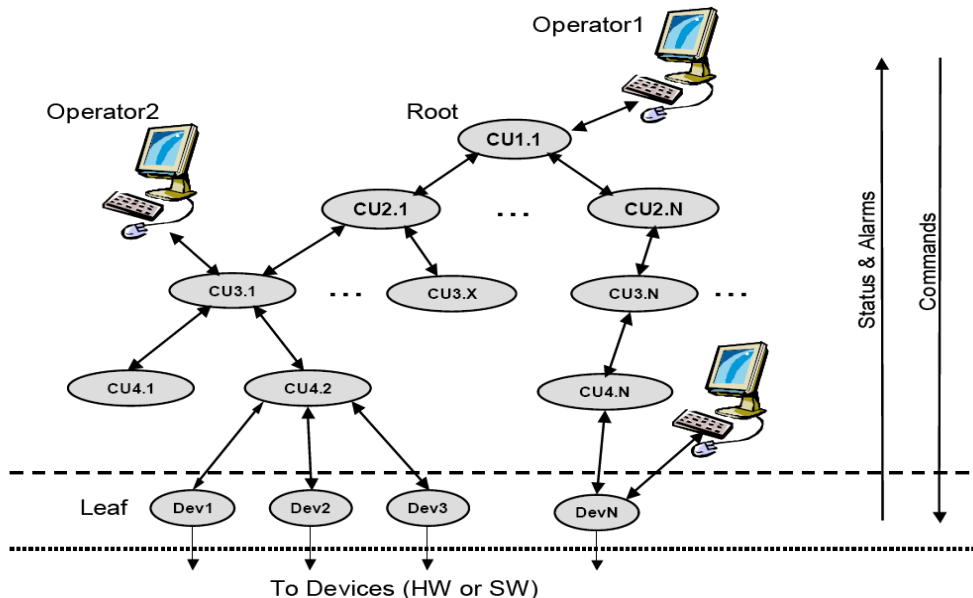
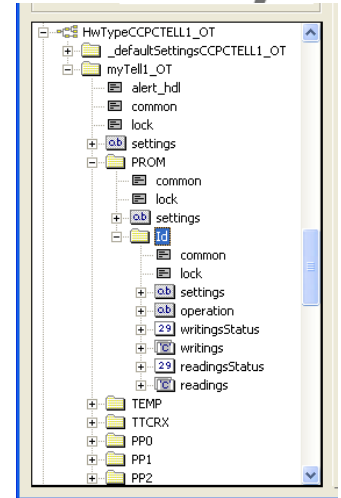
Configuration, monitoring and operation of the 'whole' experiment:

- Data acquisition & trigger
- Detector Operations (DCS)
- Experimental Infrastructure
- Interaction with accelerator & CERN Safety System

Industrial SCADA (PVSSII)

The CERN's common JCOP framework is built upon an industrial SCADA system: PVSSII

- data (registers or probes) is stored in 'data points' (=complex structures) connected to the PVSS internal memory-DB
- Change of these entries triggers a callback function
- Upon certain thresholds alerts can be launched



Extended to allow for finite state modeling & hierarchical control:

- intuitive model of subsystem
- several levels of abstraction
- sub systems can run alone
- auto-recovery from errors

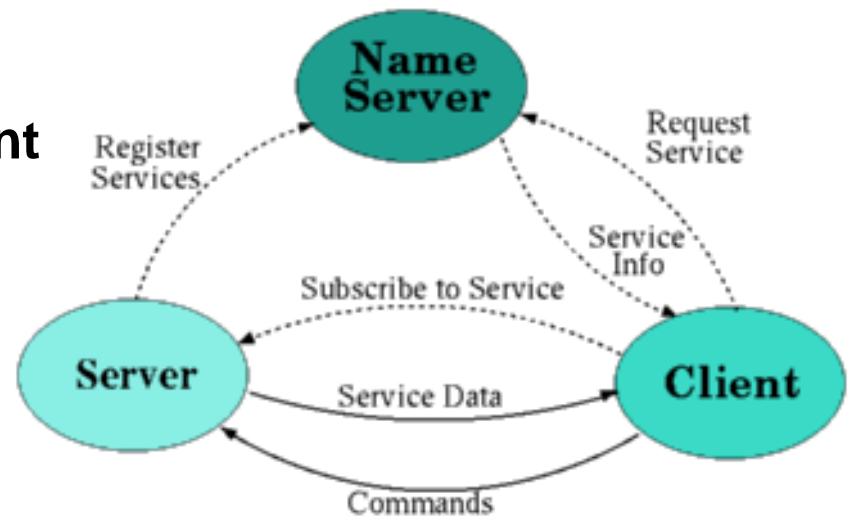
Communication Layer - DIM

Interface from ECS to hardware realized with the 'Distributed Information Management' System (DIM) – a portable lightweight communication layer:

DIM server running on CCPC publishes services to DIM Name Server (DNS) from where the client (ECS) can subscribe to it.

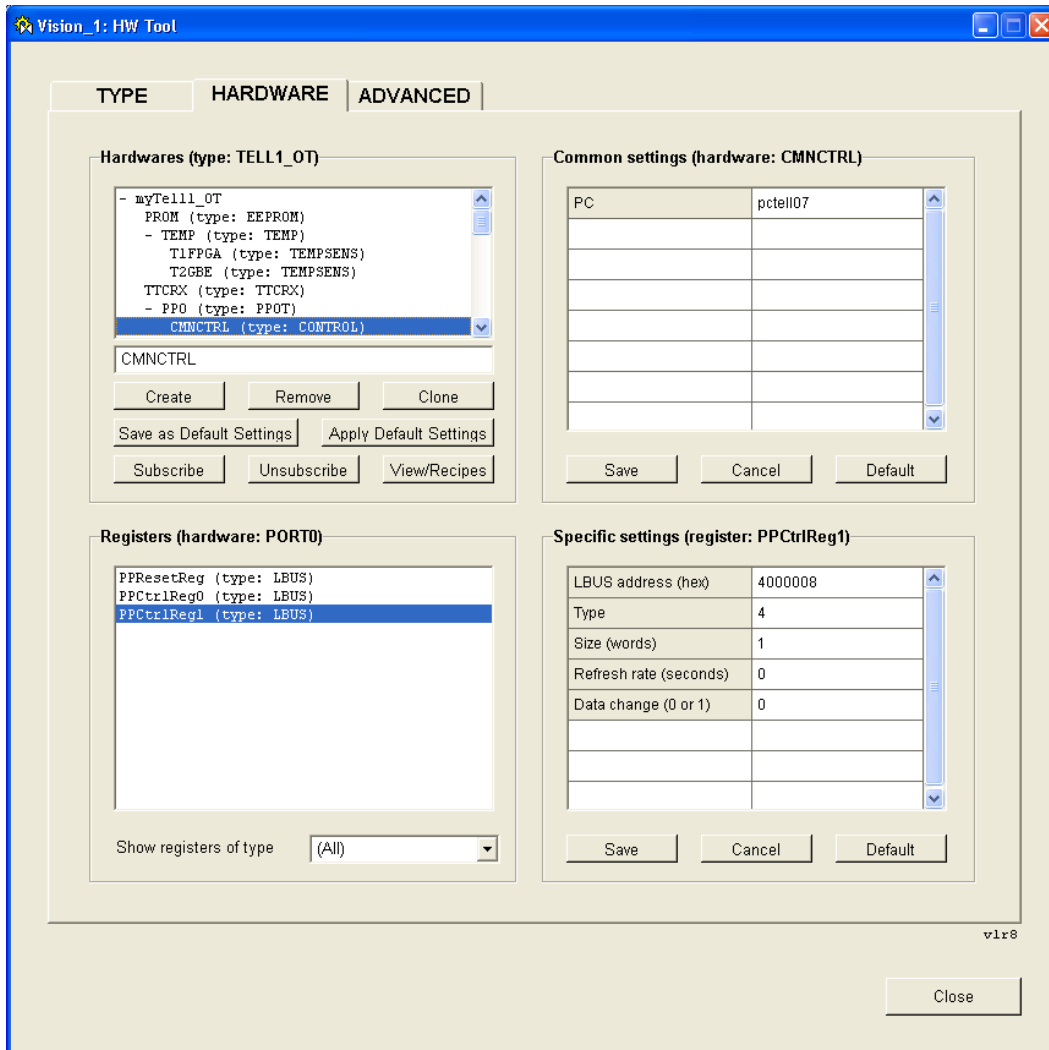
Data exchange peer to peer from server to client.

Client sends commands (write/read) – server updates services (data/status)



- **Portability:** Clients can be installed on any machine just specifying DNS node (no need to take care of connectivity)
- **Robustness:** If server crashes it can easily republish on DNS node

Abstraction Layer - FwHw



Introduced a tool to model hardware as PVSS-datapoints:

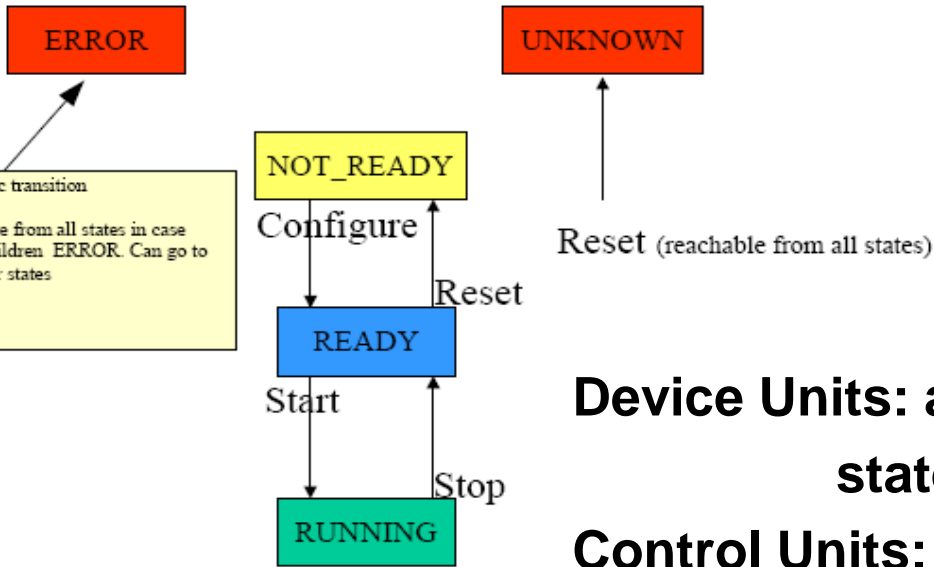
- hides diversity and complexity of the various hardware/bus types
- takes care of the communication with the Tell1 (using DIM)
- framework function calls by register name

Finite State Machines

Further abstraction as finite state machines (SML++):
defined transition from one state of the board into another with possibility to autorecover

Device Units: act on hardware (data points)
state can be triggered by hardware
Control Units: send commands to children (DU)
state transition when children change

- Firmware can be downloaded to board in state NOT_READY
- Configuration of board (mainly writing registers) via 'recipes' downloaded from Configuration Database (different settings for different run conditions)



Tell1 Control Unit

An example for a Tell1 CU panel (under construction)

System	State
Tell1Control	NOT_READY

Sub-System	State
myTell1_OT	CONFIGURING
myTell1_VeLo	NOT_READY
Velo1	READY
Velo2	READY
OT1	READY
OT2	READY
OT3	READY
OT4	READY
OT5	READY

Configuration (Start Up)

Choose Device Unit: myTell1_OT

Assign POF File: D:/tell1_OT_v1.7.pof

Assign CFG File: D:/OT_v17.cfg

Assign CCPC: pctell07

- states of children (DUs) define state of CU
- commands are propagated downwards
- partitioning of the system is a key feature (partitions can have their own trigger)
- clicking on device unit allows to open operator panels for the device (boards)

Tell1 Device Unit

Screenshot of a Tell1 DU panel – operator interface:

The screenshot displays the Tell1 DU operator interface. At the top, the device name is 'myTell1_OT' and its state is 'NOT_READY'. The interface includes a navigation menu with options like 'Overview', 'Status & Diagnostics', 'ORx', 'GBE', 'TTC & FlowControl Mon.', 'Processing Mon.', 'Data Mon.', 'Memory Usage', 'Configuration', and 'Bit Error Test'. The main area shows temperature readings (Temp PP: 27 C, Temp GBE: 21 C) and various status indicators (TTC, ORx, CCPC, CFG, processing, flow control, memory usage, data monitoring) all in green 'OK' states. A 'Counters' section lists various event counters (LD-Events, LD-FE resets, LD-EvCnt resets, BCNCnt resets, MEPs transm., MEP factor) with their values in hexadecimal. A 'Versions' section shows firmware, CFG, and server versions. A 'GBE Tx Status' table provides a detailed view of GBE ports, including Tx_OK, Tx_Error, Link Status, Dest. MAC, and Dest. IP. A 'Tell1 Src IP and MAC' section shows the source IP (11.0.0.15) and source MAC (00:02:B3:D4:FB:XX). The interface also includes a 'Messages' section at the bottom and a 'Close' button.

[MBytes]	Tx_OK	Tx_Error	Link Status	Dest. MAC	Dest. IP
port 0	0 MB	0 MB	Not_OK	00:02:B3:D4:FB:96	11.0.0.14
port 1	0 MB	0 MB	Not_OK	00:02:B3:D4:FB:96	11.0.0.14
port 2	0 MB	0 MB	OK	00:02:B3:D4:FB:96	11.0.0.14
port 3	0 MB	0 MB	OK	00:02:B3:D4:FB:96	11.0.0.14

- identifies board type
- evaluates malfunctioning parts of the board
- quick overview of important counters and registers
- reconfiguration of refresh rate

Tell1 Device Unit

The screenshot displays the 'myTell1_OT: dist_1:Manager4' window. At the top, the device name is 'myTell1_OT' and its state is 'NOT_READY'. The interface includes a navigation menu with options like 'Overview', 'Status & Diagnostics', 'ORx', 'GBE', 'TTC & FlowControl Mon.', 'Processing Mon.', 'Data Mon.', 'Memory Usage', 'Configuration', 'Bit Error Test', and 'User S'. The main area shows a hardware layout with various components and their status:

- ERROR** (orange box)
- IDLE** (green box)
- ERROR** (orange box)
- ERROR** (orange box)

Component status and configuration:

- PP0**: 0 bps
- PP1**: 0 bps
- PP2**: 0 bps
- PP3**: 0 bps
- CCPC**: memory: [input], CPU usage: [input]
- SL**: linker: 0 Hz
- MEP in:** 0 Hz
- MEP out:** 0 Hz
- TTC** (highlighted in red): LD-accept: 0 Hz, throttle: [input]
- GBE**: port0: 0 MB, port1: 0 MB, port2: 0 MB, port3: 0 MB, MEP rate: 0 bps

A 'Messages' section is visible at the bottom left, and a 'Close' button is at the bottom right.

- registers (=data points) can be connected to callback functions which allow to evaluate the functionality of subcomponents (inside Ctrl-script)
- error recovery or alerts can be implemented

Tell1 Device Unit

- many panels to monitor registers – grouped in sub panels
- panels for interaction and reconfiguration of registers

The image displays two screenshots of the Tell1 Device Unit software interface. The left screenshot shows the 'TTC & FlowControl Mon.' panel, which includes a table of TTC counters and flow control information. The right screenshot shows the 'Configuration' panel, which includes GBE Configuration, Processing Configuration, and ECS Configuration sections.

TTC Counters

number of SPIB TX MEP	32 bit	00000000
SPIB TX packet size	16 bit	
number of SPIB TX SOP	32 bit	00000000
number of SPIB TX EOP	32 bit	
number of TTC triggers	32 bit	00000000
number of TTC Trigger types	32 bit	
number of TTC dest IP	32 bit	00000000
number of TTC L0-EVID Error	16 bit	
number of TTC MEP flush signals	8 bit	00
number of TTC L0FE reset signal	8 bit	00
number of TTC BCNT reset signal	8 bit	00
number of TTC EVCNT reset signal	0 bit	00

Flow Control information (only hexadecimal)

Throttle counters	Current	log
PP-FPGA 0	0	0
PP-FPGA 1	0	0
PP-FPGA 2	0	0
PP-FPGA 3	0	0
MEP Buffer	0	0
Trigger info	0	0
Total	00000000	

FlowCtrl info in SL

FRAG_LEN_FIFO_ALMOST_FULL	0	0
FRAG_HEADER_FIFO_ALMOST_FULL	0	0
FRAG_DATA_FIFO_ALMOST_FULL	0	0
SEP_FIFO_ALMOST_FULL	0	0
SL_INFIFO_ALMOST_FULL0	0	0
SL_INFIFO_ALMOST_FULL1	0	0
SL_INFIFO_ALMOST_FULL2	0	0
SL_INFIFO_ALMOST_FULL3	0	0

GBE Configuration

Port	Port 0	Port 1	Port 2	Port 3	Scr
Enable/Disable	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Dest. MAC	00:02:B3:D4:FB:96	00:02:B3:D4:FB:96	00:02:B3:D4:FB:96	00:02:B3:D4:FB:96	00:02:B3:D4:FB:XX
Dest. IP	11.0.0.14	11.0.0.14	11.0.0.14	11.0.0.14	11.0.0.15

Processing Configuration

Info sent by: ECS triggers and all info sent by ECS

Dest IP sent by: ECS triggers and all info sent by ECS

Trigger Type sen by: ECS triggers and all info sent by ECS

Data Gen Enable: disable

Bank Class: err ped nZS ZS

Error bank: enable

ECS Configuration

Trigger number per DAQ loop:

Consecutive trigger number:

Wait cycles between triggers (25ns):

MEP Factor: 0 max 31

Trigger Type: Physics

Conclusions

- **Presented the basic concepts for implementing the LHCb readout boards into the Experiment Control System with a focus on the various layers and frameworks used**
- **The system is currently under test for commissioning of the sub-detectors (refinements still ongoing)**
- **A generic design was of major importance to allow for the usage by different subdetectors and board types**
- **Further wizards to facilitate board implementation by non experts**