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Characterization of a commercial 65 nm CMOS technology for SLHC applications

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ABSTRACT: The radiation characteristics with respect to Total Ionizing Dose (TID) and Single-Event Upsets (SEUs) of a 65 nm CMOS technology have been investigated. Single transistor structures of a variety of dimensions and several basic circuits were designed and fabricated. The circuits include a 64-kbit shift-register, a 56-kbit SRAM and a ring-oscillator. The test chips were irradiated up to 200 Mrad with an X-ray beam and the corresponding transistor threshold shifts and leakage currents were measured. Heavy-ion beam irradiation was performed to assess the SEU sensitivity of the digital parts. Overall, our results give the confidence that the chosen 65 nm CMOS technology can be used in future High Energy Physics (HEP) experiments even without Hardness-By-Design (HBD) solutions, provided that constant monitoring of the TID response is carried out during the full manufacturing phase of the circuits.

KEYWORDS: Radiation damage to electronic components; Front-end electronics for detector readout; Digital electronic circuits; Radiation-hard electronics

2012 JINST 7 P01015

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Contents

1 **Introduction** 1

2 **Experimental details** 2
- 2.1 Test vehicle 2
- 2.2 X-ray irradiation measurement setup 3
  - 2.2.1 Setup for transistor devices 3
  - 2.2.2 Setup for digital circuits 4
- 2.3 Heavy-ion beam SEU measurement setup 4

3 **TID characterization results** 6
- 3.1 Core transistor devices 6
- 3.2 I/O transistor devices 8
- 3.3 Digital blocks 9

4 **SEU sensitivity results** 10
- 4.1 Sensitivity with reduced power supply 11
- 4.2 Technology comparison 11
- 4.3 Multiple bit upsets 11

5 **Conclusions** 11

1 Introduction

Most of the microelectronics components developed for the first generation of LHC have been designed and developed using a commercial 250 nm CMOS technology with special layout techniques (Enclosed Layout Transistors, ELT, and guard-rings), with a considerable improvement over previous technologies in terms of radiation hardness, cost and performance. A second generation of designs for instrumentation for upgraded LHC detectors uses a 130 nm CMOS technology, which offers significant advantages in terms of density and power dissipation over the previous technology, especially as it does not require enclosed transistor layouts. In the vision towards future experiments or upgrades, the demand for ever smaller pixels, faster serializers and lower power in digital circuits justifies a full evaluation of a new, more advanced, low-power technology which is expected to bring further benefits to high volume (at least on the HEP scale) designs. With this aim in mind, work was started to characterize a 65 nm CMOS technology.

A step towards smaller-feature-size technologies is necessary to improve the performances of pixel detectors in terms of size and/or functionality embedded per pixel. In general, any front-end circuit can benefit from a more advanced technology node in terms of density, especially for digital

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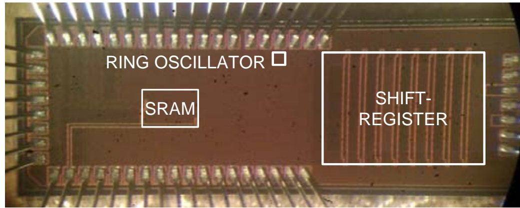

Figure 1. Digital chip with 64-kbit shift-register, 56-kbit SRAM, and 1025-elements ring-oscillator.

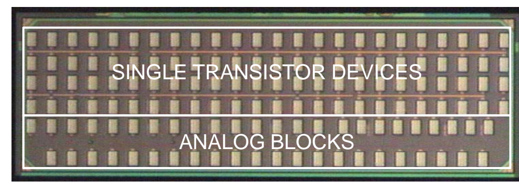

Figure 2. Chip with single transistors devices organized in a array of 24×4 pads. Additional analog blocks are present on this test chip.

2012 JINST 7 P01015

blocks. Analog parts of pixels can also benefit from the reduced capacitances associated with the smaller sizes, resulting in a lower noise equivalent charge.

The chosen 65 nm low-power CMOS technology was developed for logic and mixed-signal/RF circuits, and allows multiple supply voltages for core and I/O. Its nominal supply voltage is 1.2 V and it features a high-resistivity epitaxial substrate process, shallow trench isolation (STI), two gate oxide options (1.2 and 2.5 V), nickel-silicided low-resistance n+ and p+ polysilicon and diffusion areas. Its device options contain nMOS and pMOS with several different threshold values. High-voltage 5V-drain-tolerant devices are optional. The back-end offers 3 to 9 copper metal layers for interconnection plus 1 top aluminium layer for wirebond/flip-chip pad, pad redistribution layer and laser fuses. Low-k dielectric is used as inter-metal insulator in thin metal layers.

Previous investigation of similar technologies in the 130 nm and 90 nm nodes [1] had shown significant differences in radiation characteristics that were attributed to fine details in the fabrication of critical process steps (gate oxides, STI etc.). The investigation on at least one example of this new 65 nm technology is intended to clarify similar issues on this lithography node.

The test chips contain single transistor devices as well as digital and analog prototype circuits. In order to examine the devices' behaviour in the environment of high energy physics experiments, irradiation of the devices was performed using CERN's in-house X-ray generator. The digital blocks were irradiated in a heavy-ion beam facility in order to assess their SEU sensitivity.

The technology under study still presents some drawbacks with respect to previous generations like 130 nm CMOS. First of all, the gate leakage current is more than 15× higher in 65 nm with respect to 130 nm. Moreover newer technologies come with a set of more stringent design rules and forbidden layout patterns, making it more difficult to achieve an optimal layout. Mask fabrication and wafer production costs are higher compared to older technologies.

2 Experimental details

2.1 Test vehicle

Two test chips were fabricated in a single reticle, one test chip with digital blocks and one with analog structures and single transistor devices. The chosen metal stack for the reticle consists of 6 metals (thin M1-M4, thick M5-M6). Both chips are 3×1 mm^2 in size. Pictures of the chips are visible in figure 1 and 2.

The digital prototype circuits are namely a 64-kbit shift-register, a 56-kbit SRAM, and a 1025-elements ring-oscillator. All digital blocks were assembled with the IP available from the foundry,

Figure 3. Probe station and card under the SEIFERT RP149 X-ray generator.

Figure 4. X-ray test setup for single transistor devices, comprising a HP4145 and a Keithley 707.

2012 JINST 7 P01015

including libraries of standard cells and I/O pads, and an SRAM compiler. The digital chip was packaged in a PGA-100 carrier and a custom test board was designed and fabricated for functional and irradiation tests.

The analog blocks consist of a preamplifier for pixel sensors with a 30 ns rise time and a minimum 500 ns shaping time, a low-power discriminator (about 5 μW), a binary-weighted 6-bit DAC and a sub-binary radix DAC with an effective 6-bit precision. This article will not focus on the results obtained on the analog blocks, which will be presented in a future publication.

The single transistor devices were designed as four columns of 24 pads each, giving access to all terminals of NMOS and PMOS transistors of two types: core transistors for 1.2 V applications, I/O transistors with thicker oxide (or dual-gate, DG) available for applications using 2.5 V supply. Several transistor sizes were chosen for core transistors: an array with length L=60 nm and width W from 120 nm to 1 μm, two transistors with W=10 μm (L=1 and 10 μm). All these transistors were designed with the conventional open layout. Additionally an annular ELT transistor with the minimum allowed size of 1480$\times$60 nm was included together with a series of Field Oxide Transistors (FOXFETs) whose source and drain were either n+ diffusions or n-wells. A smaller set was chosen for I/O transistors (W$\times$L = 400 $\times$ 280, 800 $\times$ 280, 2000 $\times$ 280 nm, and 10$\times$1, 10$\times$10 μm).

2.2 X-ray irradiation measurement setup

In order to examine the devices' behaviour in the environment of high energy physics experiments, irradiation of the devices was performed using CERN's in-house 50-kV 3-kW X-ray generator (SEIFERT RP149, in figure 3) up to 200 Mrad (all doses in this paper are expressed in SiO_2). The ambient temperature during irradiation was 25°C.

2.2.1 Setup for transistor devices

Measurements have been performed with the test chips mounted on a Karl-Suss PA200 probe station with a custom probe card installed within X-ray irradiation cabinet. The dose rate was about 41.5 krad/min. Devices were kept under worst-case bias during irradiation, therefore all terminals of the transistors were grounded, except the gate of NMOS transistors, which was kept

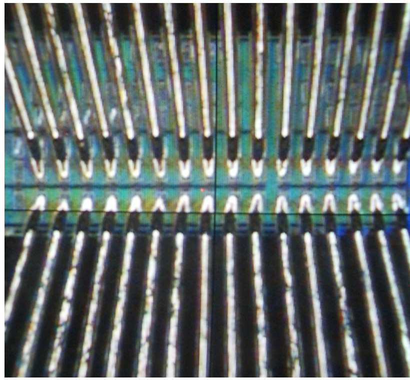

Figure 5. Microscope view of chip under probe tips during alignment.

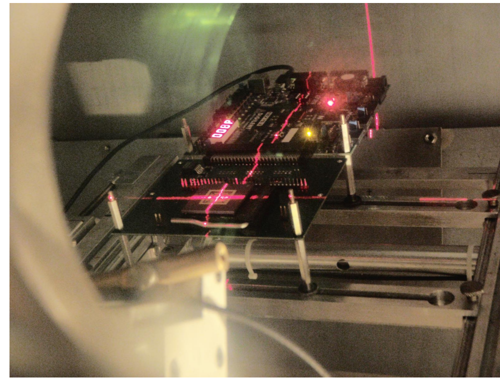

Figure 6. Test card for heavy-ion beam test in vacuum chamber during targeting

2012 JINST 7 P01015

at the nominal power supply voltage V_{dd} (1.2 V for NMOS core transistors and 2.5 V for NMOS I/O transistors).

The custom probe card has 32 probe tips (two columns of 16) which match the size and pitch of the pads in the test chip (see figure 5). A semiconductor parameter analyzer HP4145 (figure 4) performed the static transistor measurements, applying and measuring currents and/or voltages. A Keithley 707 switching matrix connected the measuring channels of the HP4145, or the output of the voltage source, to the appropriate probe tip channels. All the instrumentation and X-ray generator was controlled by a PC running Labview, in particular the full measurement and irradiation of the transistors could be done sequentially and fully automatically.

This unique test setup enabled us to perform all the characterization without the need for any manipulation, hence ensuring that the extremely thin and fragile gate oxide of the transistors under test was not damaged.

No annealing measurement was done yet on single transistor devices.

2.2.2 Setup for digital circuits

The custom test board for the digital chip mounts a Xilinx Spartan 3E FPGA, a USB interface chip for connection to a host computer and a socket for the PGA100 Device Under Test (DUT). The FPGA is programmed to apply checkerboard test patterns to the DUT on command from the host computer and check its response. The test results are sent back to the host computer.

The DUT was placed together with its test board under the X-ray generator, set at a dose rate of 60 krad/min. The digital circuits were operating during irradiation and annealing. In particular for the SRAM and shift-register circuit, the operating clock frequency was 30 MHz. Circuit functionality was monitored and static and dynamic supply currents were measured during and after irradiation as well as after the annealing period. The chip was annealed for 1 week at a temperature of 100°C.

2.3 Heavy-ion beam SEU measurement setup

Samples of the digital prototypes were irradiated in the heavy-ion beam facility in Louvain-La-Neuve (Belgium), in order to assess the SRAM and shift-register SEU tolerance. The same test

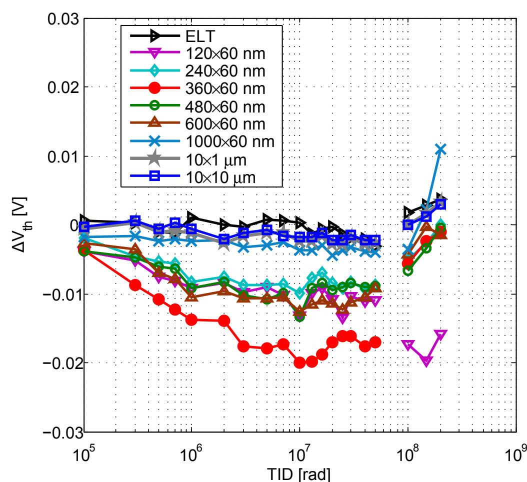

Figure 7. Threshold voltage shift measured for NMOS core devices.

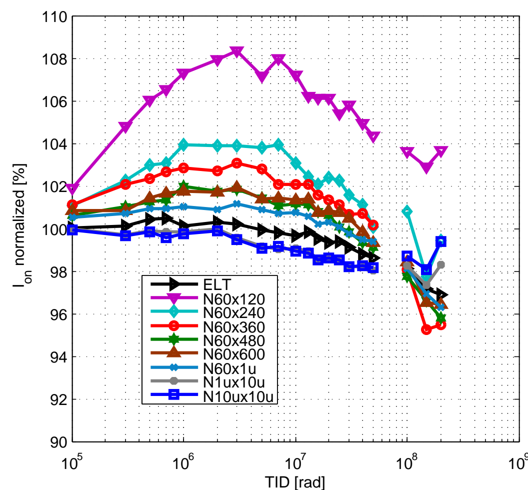

Figure 8. Max. drive current (V_{gs}=V_{ds}=1.2 V) measured for NMOS core devices, normalized to pre-rad.

board as for the X-ray irradiation was used for the SEU test, placed in the vacuum chamber and connected with a host computer outside the chamber (see figure 6). High-penetration ions were chosen for this test.

Two kinds of tests were done for the shift-register: static and dynamic. Only the static test was run for the SRAM. In the static test the data retention of the SRAM and shift-register storage was studied. In the dynamic test, the robustness of the registers to SEUs when the clock is running was investigated.

For the static test the procedure is as follows: a pattern is loaded in the shift-register and SRAM while the beam is off; the clock is stopped and all Device Under Test (DUT) input signals are frozen; the beam is turned on for a specific fluence and then turned off; the clock is run again and the output of the DUT is compared with the original (expected) one.

For the dynamic test the procedure is: an indefinitely long configuration bitstream is loaded in the shift-register chain; at the same time the output bitstream is continuously compared with the original one; the beam is turned on for a specific fluence and then turned off; the clock is stopped.

The SEU cross-sections are derived by dividing the total number of errors observed for each ion Linear Energy Transfer (LET) by the total fluence of the ion beam. The ions used in the test were $^{22}Ne^{7+}$ at 235 MeV energy giving an LET of 3 MeVcm^2/mg, $^{40}Ar^{12+}$ at 372 MeV giving an LET of 10.2 MeVcm^2/mg, and $^{58}Ni^{18+}$ at 567 MeV giving an LET of 20.4 MeVcm^2/mg. All other LET points are obtained by tilting the beam with respect to the chip surface (45° and 60°).

The test was run at two different power supply settings, the nominal 1.2 V and a reduced 0.9 V, in order to evaluate the impact of the reduced power supply on the cross-section, in the vision of using a reduced supply for non-critical digital blocks for low-power applications.

All tests with tilted beam were run with the beam azimuth orthogonal to the chip long side. Only for the $^{58}Ni^{18+}$ ion tilted by 60°, irradiation test was conducted additionally at the other orientation with respect to the beam (along chip long side).

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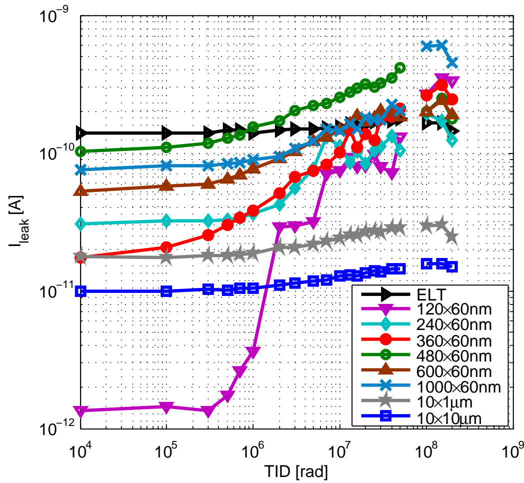

Figure 9. Leakage current measured for NMOS core devices.

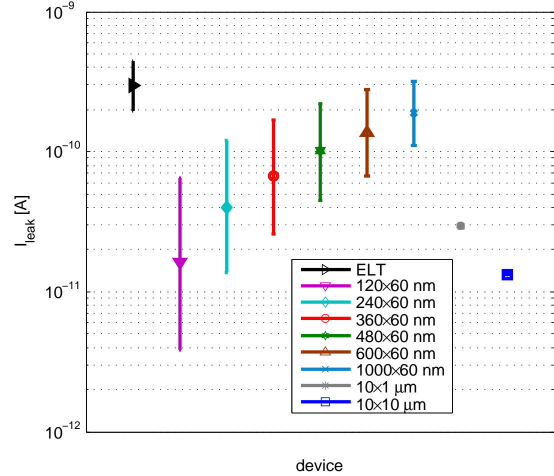

Figure 10. Core NMOS leakage current spread due to $\pm 1\sigma$ process variation from Monte Carlo simulation.

3 TID characterization results

This section presents the results obtained from the measurement of transistor devices and digital blocks. Transistor measurements refer to two identical sets of structures (two chips) which were consecutively irradiated and characterized. Results on digital blocks were obtained from a single irradiated chip.

3.1 Core transistor devices

The threshold voltage of the core NMOS devices changes very little (up to 20 mV) in the explored TID range, as can be seen from figure 7. Some rebound effect is visible only for narrow devices, most likely due to the different contribution of the two opposing effects of charges trapped in the oxide and Si-SiO_2 interface states. The subtreshold slope does not change significantly.

The curve for the ELT device demonstrates a high TID tolerance of the gate oxide of the studied technology, since its threshold voltage shift is practically unnoticeable, as it is for the increase in leakage current, visible in figure 9. Nevertheless, normal-layout NMOS devices suffer from an increase in leakage current, which is more pronounced for narrow devices, showing an edge-dependent effect similar to what observed in the 130 nm technology [2] commonly now used for many detector upgrade projects. Devices wider than 360 nm have an increase in the off-current of less than 10×, while it can rise of 300× in narrower devices. Still, this is a much better performance with respect to the 130 nm technology studied in [2], where all devices were peaking at about 100 nA leakage. These results suggest the possibility of using core transistors without any special layout protection technique against TID. In addition, the changes in leakage current of the transistors are comparable with its spread due to the process variation, as shown in figure 10.

The threshold voltage shift of PMOS devices is limited to 60 mV for the narrower devices, as shown in figure 11, and even less than 10 mV for wide devices (W>1 μm).

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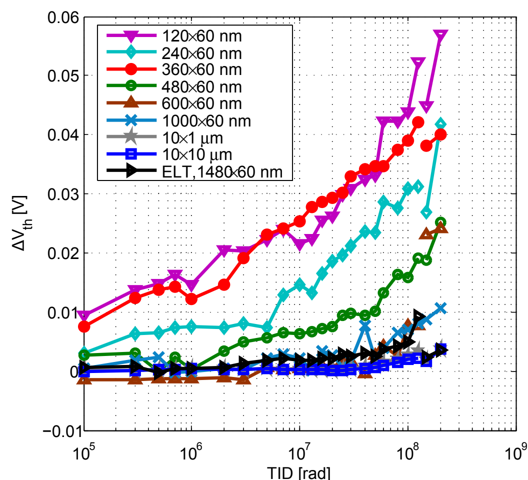

Figure 11. Threshold voltage shift measured for PMOS core devices.

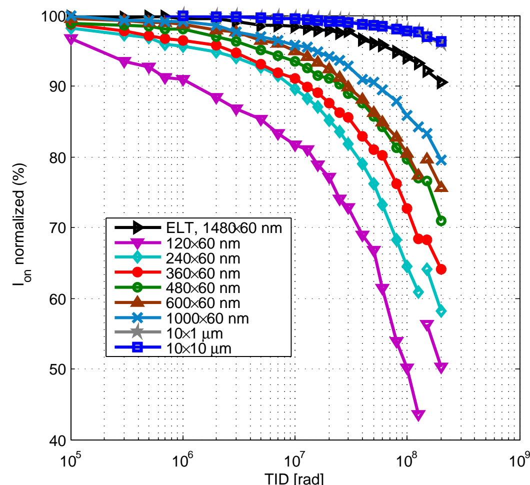

Figure 12. Max. drive current (V_{gs}=V_{ds}=1.2 V) measured for PMOS core devices, normalized to pre-rad.

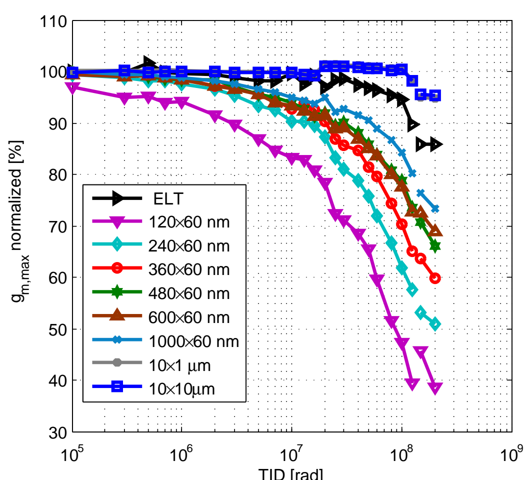

Figure 13. Maximum g_m (strong inversion) for PMOS core devices, normalized to pre-rad.

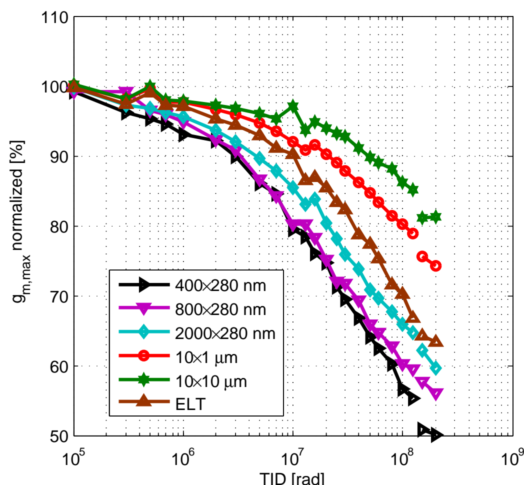

Figure 14. Maximum g_m (strong inversion) for PMOS I/O devices, normalized to pre-rad.

The maximum drive current of PMOS devices degrades with radiation by 50% for the narrowest device, as depicted in figure 12, but this is only partly due to the change in V_{th}. Most of the degradation comes instead from a reduction in the transconductance (g_m) in the strong inversion region as visible in figure 13. The reduction depends again on the width of the transistor, the wider transistors having a smaller decrease. The degradation in drive current can influence the speed of digital logic. The transconductance in weak inversion region does not change with radiation. It is notable that NMOS devices do not show a decrease in transconductance as visible from figure 8.

The leakage current for FOXFETs remained under 0.5 pA/μm (given as current per unit width) in the explored TID range.

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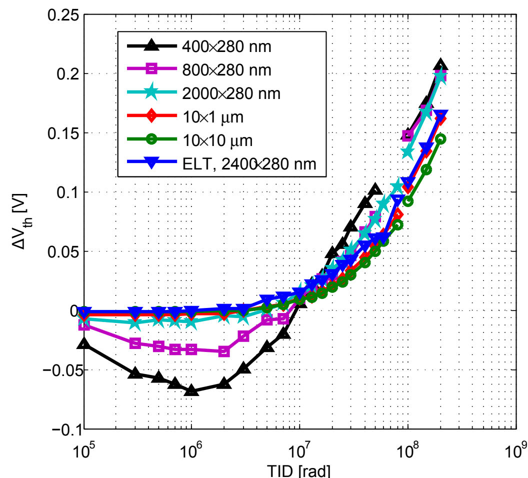

Figure 15. Threshold voltage shift measured for NMOS I/O devices.

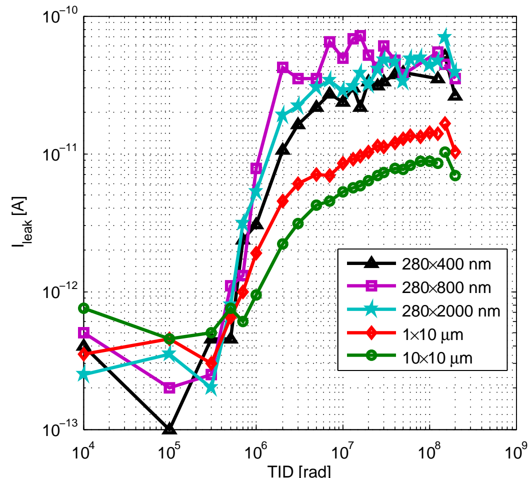

Figure 16. Leakage current measured for NMOS I/O devices.

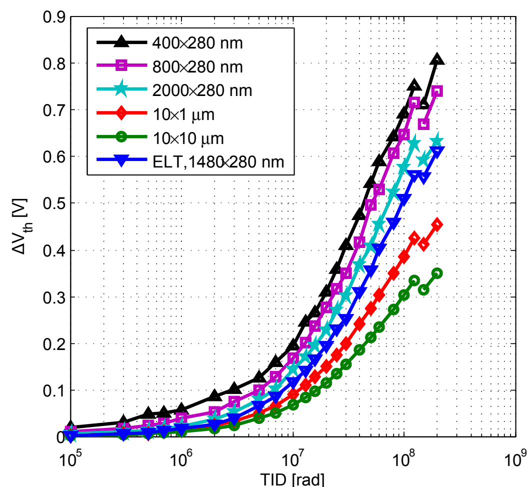

Figure 17. Threshold voltage shift measured for PMOS I/O devices.

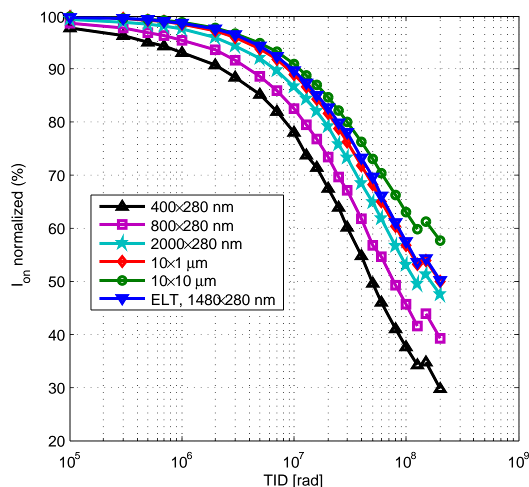

Figure 18. Max. drive current (V_{gs}=V_{ds}=2.5 V) measured for PMOS I/O devices, normalized to pre-rad.

3.2 I/O transistor devices

The threshold voltage shift measured for I/O NMOS devices is within 200 mV, which is about 40% of the typical V_{th} of I/O transistors, and positive for all devices. This means that the devices tend to turn off, slowing down the logic (see figure 15).

The leakage current of the devices increases by 2 orders of magnitude, as visible in figure 16. Most of the change happens at about 1 Mrad. This result suggests that ELT should be employed in I/O design. Once again, the performance of the I/O NMOS transistor in this technology is by far superior to the 130 nm previously referenced, where I/O leakage peaks at 1 μA for similarly-sized devices.

PMOS I/O transistors have a strong degradation in their performance, as can be seen in fig-

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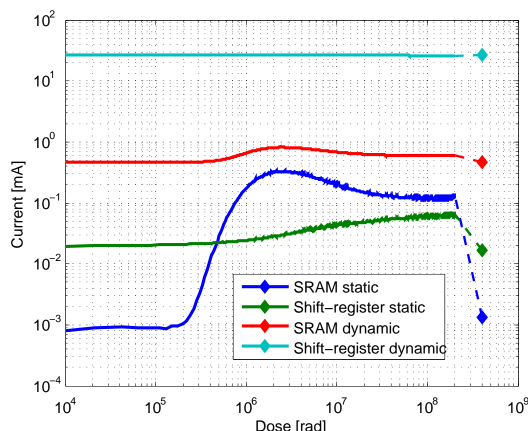

Figure 19. Power supply currents vs TID for SRAM and shift-register blocks. Marked (last) point is after annealing at 100°C for 1 week.

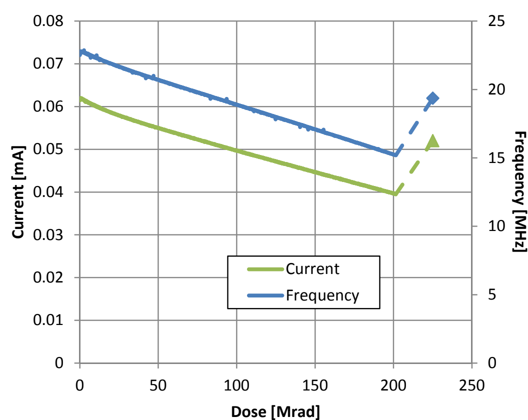

Figure 20. Ring oscillator frequency and supply current vs TID. Marked (last) point is after annealing at 100°C for 1 week.

2012 JINST 7 P01015

ure 17, having a considerable shift of the threshold voltage: up to 800 mV, which accounts for 160% of the typical pre-rad value. This shift is more pronounced for narrow devices, which should be avoided in the design of critical blocks. Figure 18 shows the effects on the drive current of this change in threshold voltage, combined with the reduction in transconductance (see figure 14).

3.3 Digital blocks

The static and dynamic currents of the SRAM and shift-register blocks measured during the irradiation and after annealing are plotted in figure 19. Both blocks were operating and functional throughout the whole irradiation and after annealing.

The SRAM static current increases by a factor 300× with TID and its dynamic current reflects this change with a small rise; the current peaks at about 2.5 Mrad and then decreases partially. This behaviour is most likely dependent on the dose rate, since there is an evidence of a partial annealing effect taking place at room temperature with a short time constant (about 1.5 hours). The final annealing step at 100°C brings back the supply current value to the pre-rad within a factor 1.7×. The SRAM is the block that suffers most from TID, probably due to the use of ultra-narrow transistor (W=80 nm) in the SRAM memory cell.

The shift-register static current changes very little with respect to the SRAM, increasing within a factor 3.3×. Contrary to this, the corresponding dynamic current has a small decrease of about 3%, which probably translates to a proportional speed reduction. Once again the annealing step restores the supply currents to their pre-rad value.

The ring oscillator frequency and current decrease constantly with TID, as visible in figure 20. The circuit slows down from a pre-rad frequency of 22.5 MHz to a minimum of 15.2 MHz and then recovers partly with the annealing to 19.4 MHz, which represents a net 13.8% less speed and power. This should be taken into account in the design of digital circuits by adding a margin in the timing budget of critical paths. This behaviour of the ring-oscillator is most likely due to the reduction of drive current of the inverter's PMOS, which tends to turn off with accumulated TID.

The I/O pad current has a negligible change in the explored TID range.

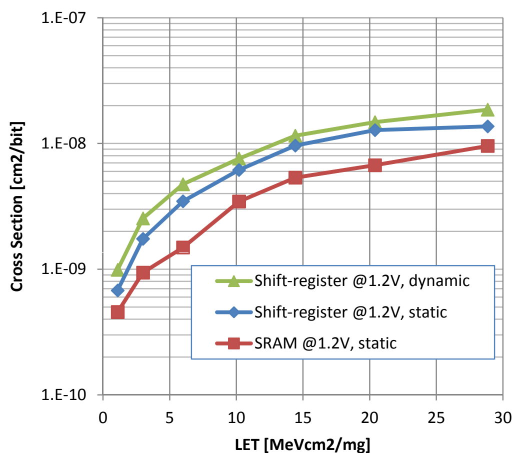

Figure 21. Cross-section vs LET plot for digital blocks powered at 1.2 V supply voltage.

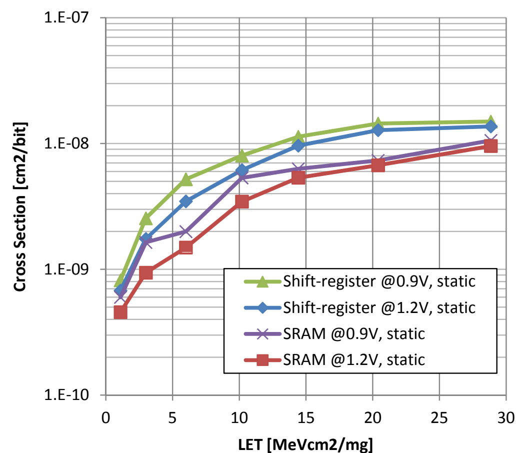

Figure 22. Comparison of cross-section of digital blocks powered at 1.2 V and 0.9 V supply voltages.

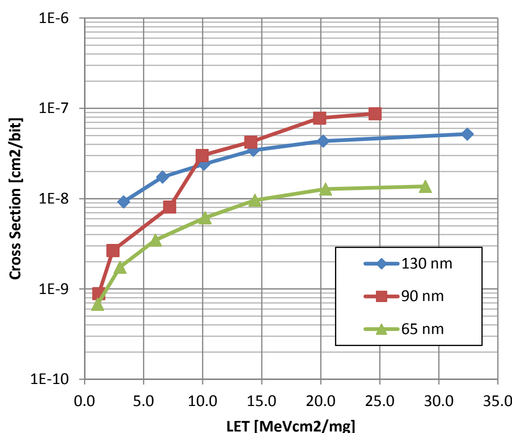

Figure 23. Technology comparison of cross-sections of D flip-flops.

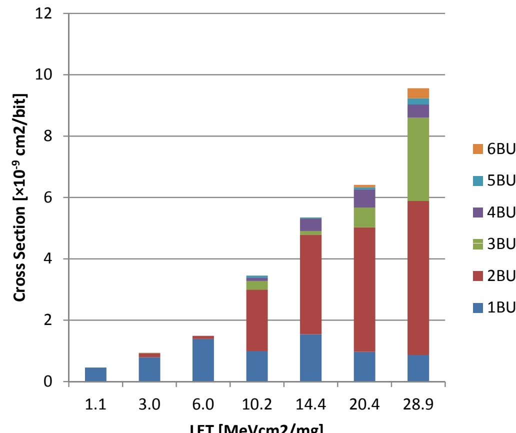

Figure 24. Multiple n-bit upset (nBU in the figure) occurrence in the SRAM circuit, powered at 1.2 V.

4 SEU sensitivity results

The cross-section per bit of the SRAM and shift-register blocks are presented in figure 21 (for 1.2 V power supply). No substantial difference is visible between the static and dynamic tests run on the shift-register. The SRAM cell has an area about 13× smaller with respect to the flip-flop used in the shift-register, therefore it has a lower cross-section, though not strictly proportional to the area. The LET threshold is lower than 1.1 MeVcm^2/mg for both the digital cells, therefore we can expect upsets in the LHC environment and redundancy should be applied for protection against SEU [3].

The shift-register showed an evidence of particle hits on the clock-tree, which caused thousands of errors simultaneously. Even though the cross-section of these events is too low to be plotted, designers should take this effect into account when building SEU-robust blocks.

2012 JINST 7 P01015

4.1 Sensitivity with reduced power supply

The reduction of the power supply voltage to 0.9 V gives an increase of 70% in cross-section in the worst case, as shown in figure 22 for both the SRAM and the shift-register, which have similar results. In a typical application the reduction in power supply can give great savings in power and this increase in cross-section is acceptable.

The dependence on the power supply is slightly bigger compared to data acquired in a 90 nm technology (different foundry) [4].

4.2 Technology comparison

The results obtained for the shift-register at 1.2 V are compared in figure 23 to a standard library register flip-flop available in 130 nm technology and to a custom-made flip-flop in 90 nm (both these from another foundry), previously tested in the same facility [4, 5] at the same supply voltage. All technologies have low LET threshold (<1.1 MeVcm^2/mg).

It is interesting to note that the area ratio between the standard library cells in 130 nm and 65 nm is about 4× and the cross-section scales almost proportionally by a factor 3.4×. Even though the saturation cross-section of the cells in 65 nm is lower with respect to previous technologies, this is far above the one obtained for SEU robust cells, which have also, most importantly, higher LET thresholds [6].

4.3 Multiple bit upsets

Multiple Bit Upsets (MBUs) have a strong contribution to the cross-section in the SRAM sensitivity. Figure 24 shows the importance of simultaneous errors for the SRAM powered at 1.2 V. Most of these errors occur in adjacent cells along the direction of the n-wells present in the SRAM and which run all the way through the block. MBUs of slightly bigger multiplicity are detected when the SRAM is powered at 0.9 V (up to 7 bits upset simultaneously). Though the shift-register showed some double- and triple-BUs, their amount is negligible (less than 1%) with respect to the number of single bit upsets.

The test with beam azimuth transverse to the chip showed a small dependence of the SRAM cross-section on the beam direction, giving 42% more errors with respect to the case of azimuth orthogonal to the chip long side. This can be explained by the fact that the transverse orientation increased the importance of MBUs and their multiplicity (up to 10 bits upset together), most likely because in this case the beam azimuth was along the n-well stripes of the SRAM. The different orientation of the beam didn't impact significantly the cross-section of the shift-register.

5 Conclusions

The results of this irradiation campaign suggest that the studied 65 nm CMOS commercial technology does not require special HBD transistor layouts for digital logic in order to be TID-tolerant up to 200 Mrad. Two digital blocks made with foundry IP, a shift-register and an SRAM, were irradiated while operating and were functional throughout the whole test, with a limited increase in operating current. The measurement done after an annealing period confirm this result, since the supply currents return back to the pre-rad values.

2012 JINST 7 P01015

The TID performance of transistor devices was characterized and suggests that the only requirement to achieve high total dose resistance is that all core devices have width bigger than 360 nm in order to limit the increase in leakage current to 10× for NMOS and the loss in drive current to 30% for PMOS. I/O devices might need to use ELT shape and/or be oversized for TID hardness. Our 65 nm technology demonstrates better TID performance compared to the 130 nm technology currently in use for most of the upgrade projects of LHC detectors.

The SEU cross-section of the standard library register studied is lower than equivalent blocks in other older technologies. Scaling the power supply voltage for lower power consumption seems to affect only marginally the SEU cross-section.

X-ray irradiation at low temperature (-30°C) is planned, in order to evaluate the TID performance without the annealing effect present during irradiation at standard temperature. Results on the analog blocks will be presented in a future publication.

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2012 JINST 7 P01015