Characterisation of the NA62 GigaTracker end of column readout ASIC

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Characterisation of the NA62 GigaTracker end of column readout ASIC

M. Noy,[a,1] **G. Aglieri Rinella,**[a] **M. Fiorini,**[a] **P. Jarron,**[a] **J. Kaplon,**[a] **A. Kluge,**[a] **E. Martin,**[b] **M. Morel,**[a] **L. Perktold**[a] **and P. Riedler**[a]

[a] *CERN,*
CH-1211 Geneva 23, Switzerland
[b] *Universite Catholique de Louvain,*
1348 Louvain-la-Neuve, Belgium

E-mail: matthew.noy@cern.ch

ABSTRACT: The architecture and characterisation of the End Of Column demonstrator readout ASIC for the NA62 GigaTracker hybrid pixel detector is presented. This ASIC serves as a proof of principle for a pixel chip with 1800 pixels which must perform time stamping to better than 200 *ps* (RMS), provide 300 μm pitch position information and operate with a dead-time of 1% or less for 800 MHz-1 GHz beam rate. The demonstrator ASIC comprises a full test column with 45 pixels alongside other test structures. The timewalk correction mechanism employed is measurement of the time-over-threshold, coupled with an off-detector look-up table. The time to digital converter is a delay locked loop with 32 contributing delay cells fed with a 320 MHz to yield a nominal bin size of 97 *ps*. Recently, P-in-N sensors have been bump-bonded to the ASIC and characterisation of these assemblies has begun.

KEYWORDS: Pixelated detectors and associated VLSI electronics; Particle tracking detectors (Solid-state detectors)

[1] Corresponding author.

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1 Introduction

1.1 The GigaTracker

The NA62 [1] GigaTracker [2] (GTK) hybrid pixel detector comprises three stations situated early in the experiment decay line, designed to measure the momentum, angle and traversal time of the incident particles entering the decay line from the target. Figure 1 shows the setup and figure 2 shows the beam and detector profiles.

The requirements on these parameters are driven by the demanding background rejection level necessary for the rare kaon decay measurement. In total, the beam rate incident on the GigaTracker is expected to be around $800\,MHz - 1\,GHz$, which equates to approximately $140\,kHz$ per pixel in the centre, where the intensity is the highest. The total dead time of the detector is required to be less than 1%.

Each detector instruments an area of $60 \times 27\,mm^2$ and consists of an array of 18000 pixels, each one nominally $300 \times 300\,\mu m^2$. Time stamping is required to the level of $200\,ps$ (RMS) for each station. The front end must accommodate a range of input charges from $5000\,e^-$ to $60000\,e^-$. A summary of the key parameters of the GTK system may be found in table 1.

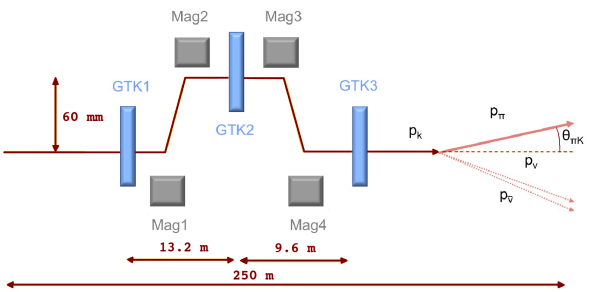

Figure 1. GTK Architecture.

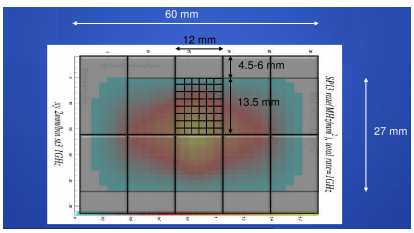

Figure 2. Beam and detector profiles.

Table 1. Key Parameters of the GTK System.

Total Dose	$10^{14} n\,cm^{-2}\,yr^{-1}$
Columns/Readout Chip	40
Pixels/Column	45
Pixel Size	$300\,\mu m \times 300\,\mu m$
Beam Rate	$800\,MHz \rightarrow 1\,GHz$
Dynamic Range	$\sim 1fC \rightarrow 10fC$
Most Probable Charge	$2.4\,fC$
Time Binning	$\sim 97\,ps$
Efficiency	$\geq 99\%$

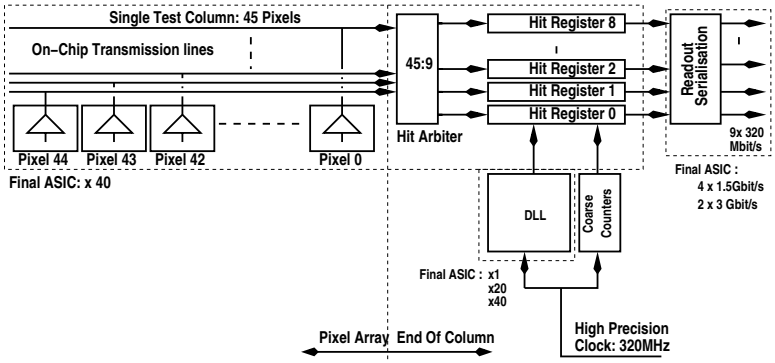

Figure 3. A schematic view of the EOC architecture.

1.2 Demostrator ASIC

A demonstrator ASIC has been designed and fabricated in a commercially available 130 *nm* CMOS technology. The architecture of the implemented design employs a pixel array operating asynchronously with a single-threshold discriminator output, driving an End Of Column (EOC) Delay Locked Loop (DLL) based Time-to-Digital Converter (TDC) via transmission lines. This proof of concept ASIC has a full column of 45 pixels alongside test structures to validate and characterise individual components of the design. A schematic representation of this can be seen in figure 3. Hit register multiplexing is implemented as nine 5:1 hit arbiters, permitting a 5-fold reduction in the number of hit registers required whilst only incurring a dead-time penalty of a fraction of a percent.

Readout is orchestrated in an untriggered, event-driven fashion, similar to that which is envisaged for the final ASIC, with the exception that one 320 MHz serialiser is used for each hit group, whereas a fewer number of multi-gigabit serialisers will be used in the future. The time bin of the TDC is nominally 97 *ps*, achieved by feeding a low jitter 320 MHz clock into a delay line with 32 contributing starved delay cells. The phase of the clock at the output of this delay line is measured with respect to that of the incident clock, and depending on whether this output clock is early or late, the speed of the elements in the delay is decreased or increased respectively. Upon a hit, the state of the delay line is latched into a hit register, providing a linearly encoded bit pattern indicat-

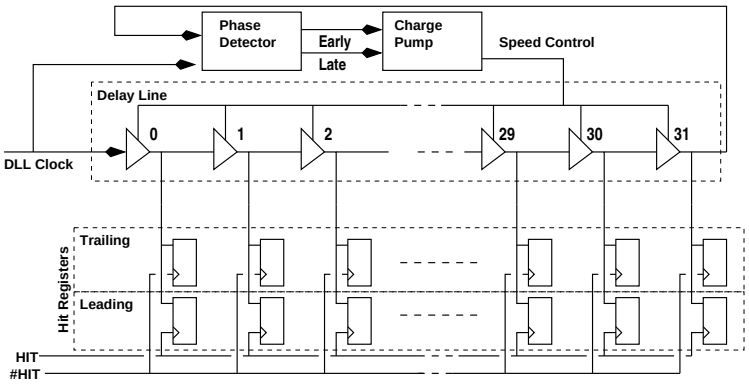

Figure 4. A schematic view of the DLL (1 hit register shown).

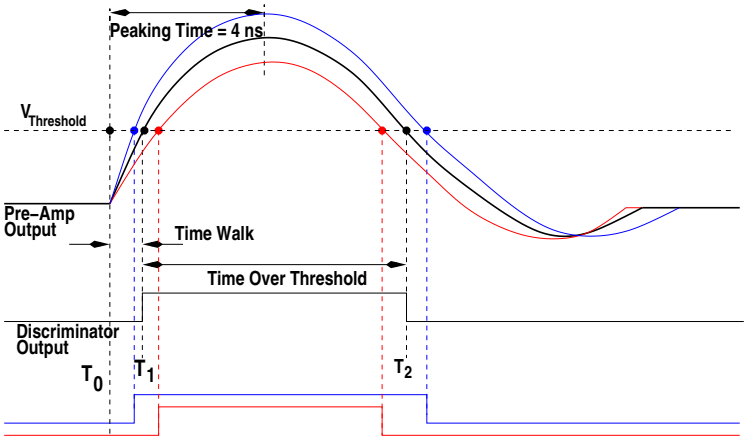

Figure 5. A schematic representation of the front-end amplifier and discriminator outputs for different charges.

ing the phase of the hit with respect to the clock domain. A schematic representation of the delay line showing one leading/trailing pair of hit registers can be seen in figure 4.

Two binary encoded 32-bit coarse counters are used to extend the dynamic range of the TDC, with one being updated on the rising edge of the DLL clock and the other on the falling edge. When a hit occurs, both counter values are latched and all data are serialised off-chip. The fine time then needs to be used to determine the phase of the hit with respect to the clock domain and subsequently which value should be combined with the fine time to construct the final time stamp.

1.3 Time walk compensation

Time-walk compensation of the discriminated front-end amplifier signal is foreseen using a Time-Over-Threshold (TOT) approach, where timestamps from the leading and trailing edges of the discriminated pixel output permit an off-detector look-up of the corrected time. Figure 5 shows a schematic of the signal shapes and their discriminated counterparts for different charges. The key times T_0, T_1, T_2 and the time over threshold are indicated.

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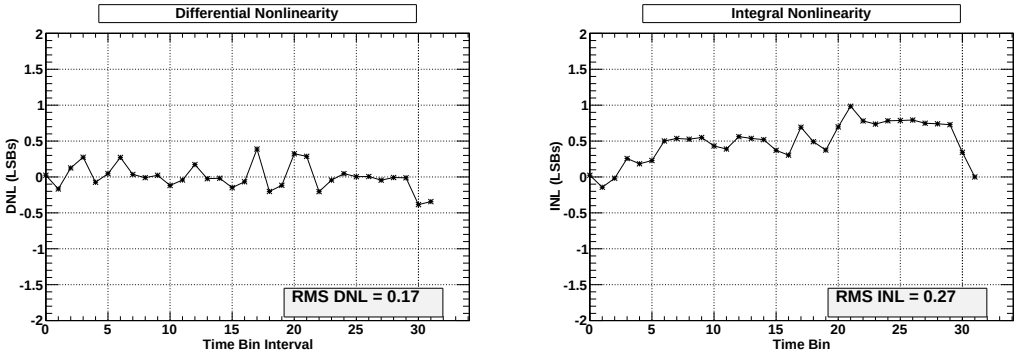

(a) Differential Non-Linearity.

(b) Integral Non-Linearity.

Figure 6. The DLL Differential and Integral Non-Linearities.

2 Results

2.1 TDC

The TDC differential and integral non-linearities (DNL, INL) were extracted from code density measurements, where a large number ($20x10^6$) of random triggers from a flat distibution were applied to the TDC. The resulting time stamps were collected and location of the rising transition extracted. This fine time was then histogrammed, providing an estimate of the probability that a trigger will fall into a given bin. Knowing the clock period and that no triggers are missed, the width of each bin can be estimated. The bin widths permit the calculation of the DNL and INL, shown in figures 6 (a) and 6 (b) respectively.

2.2 Test pixel performance

The behaviour of the discriminated test pixel was investigated over the pertinent charge range ($1 \rightarrow 10\,fC$), both through direct electrical charge injection to the front end via a $20\,fF$ calibration capacitor, and using a high speed $1060\,nm$ laser focussed onto the pixel of a sensor with an opening in the back-side metalisation to permit such investigation.

Figure 7 shows the test pixel T_1 behaviour as a function of charge for these two cases. The pixel is driven at a fixed rate of $100\,kHz$ in both cases. To ensure complete and rapid charge collection, the detector is biased with $300\,V$.

2.3 Full chain performance

The performance of the system full chain has been measured without the detector present at the time of the conference. This includes the pixel front end amplifier, discriminator, transmission line driver and receiver, hit arbiter, TDC and hit registers. The data are serialised off-chip and captured by the DAQ system. In order to demonstrate the necessary behaviour at the system level, a calibration data set was acquired from which the calibration curves necessary to correct the charge dependent time walk of T_1. A statistically independent data sample was then analysed and the random and systemantic components of the corrected time, T_0, plotted.

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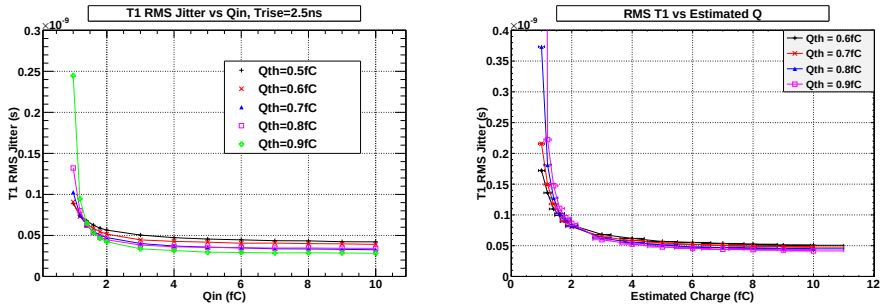


(a) Bare Pixel. (b) Assembly.

Figure 7. Test Pixel T_1 behaviour as a function of input charge without (a) and with (b) detector.

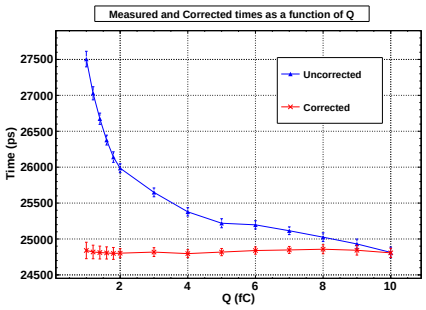
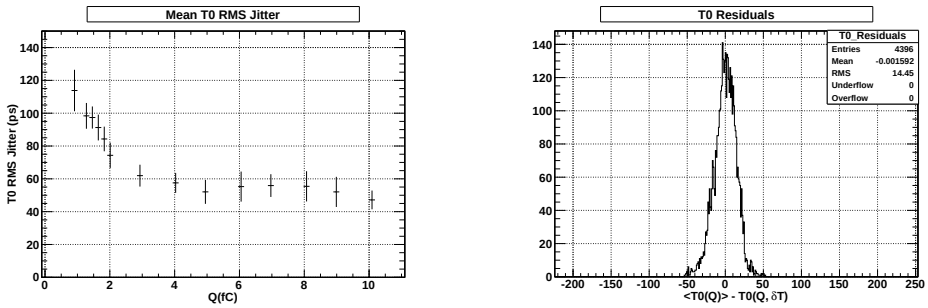


Figure 8. The uncorrected (T_1) and corrected (T_0) times for a single phase.



(a) T_0 Random Jitter as a function of charge. The error bars represent 1σ of the distibution due to the phase.

(b) The T_0 systematic errors histogrammed over all charges and all phases.

Figure 9. The random and systematic components of the charge-independent reconstructed time T_0.

In order to characterise the effects of the TDC digitisation noise, the time of the charge injection was swept through the whole clock period in steps of $10\,ps$ ($0 \rightarrow 3130\,ps$ inclusive) and the data set aquired for each phase. Figure 8 shows the measured T_1 and the calculated T_0 for one such phase. To summarise the performance, the RMS Jitter of the reconstructed time (T_0), averaged over all phases, as a function of charge is shown in figure 9 (a). The corrected time calculated after the calibration still retains some systematic residual components, the magnitude of which, over all charges and all phases, is summarised in figure 9 (b).

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3 Summary and conclusions

A pixel readout ASIC has been designed and fabricated in 130 *nm* commercial techonology, providing time-over-threshold approach to timewalk correction coupled to an EOC DLL-based TDC with a nominal 97 *ps* time bin. Characterisation of this ASIC shows that the performances of the pixel and TDC are at the level required by the experiment. Preliminary measurements of the detector and pixel behaviour with a laser charge injection system indicate that the increase in noise from the detector capacitance is at the expected level. Current research is focussed on deeper evaluation of the assembly behaviour.

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