Multi-Channel Amplifier-Discriminator for Highly Time-Resolved Detection

M. Despeisse, F. Powolny, P. Jarron, and J. Lapington

***Abstract*—A low-power multi-channel amplifier-discriminator was developed for application in highly time-resolved detection systems. The proposed circuit architecture, so-called Nino, is based on a time-over-threshold approach and shows a high potential for time-resolved readout of solid-state photo-detectors and of detectors based on vacuum technologies. The Irpics circuit was designed in a 250 nm CMOS technology, implementing 32 channels of a Nino version optimized to achieve high-time resolution on the output low-voltage differential signals (LVDS) while keeping a low power consumption of 10 mW per channel. Electrical characterizations of the circuit demonstrate a very low intrinsic time jitter on the output pulse leading edge, measured below 10 ps rms for each channel for high input signal charges (>100 fC) and below 25 ps rms for low input signal charges (20–100 fC). The read-out architecture moreover permits to retrieve the input signal charge from the timing measurements, while a calibration procedure was developed to correct for time walk variations of the output pulses. The Irpics circuit therefore shows a high potential of application in multi-channel detection systems requiring a high time resolution, as needed for Time Of Flight systems (TOF), Positron Emission Tomography (PET) or time-resolved spectroscopy.**

***Index Terms*—CMOS circuits, detector instrumentation, fluorescence spectroscopy, high energy physics instrumentation, photodetectors.**

I. Introduction

THE detection of photons and/or charged particles with high-time resolution is of paramount importance for a wide variety of applications. In High-Energy Physics (HEP), stringent timing requirements have to be met for detectors measuring the transit-time of relativistic particles in order to identify the particles momentum and energy. Typical time resolutions below 20 ps rms are required for future experiments [1]. Similar timing requirements are also found in time-resolved spectroscopy experiments. In life-science, Fluorescence Lifetime Imaging Microscopy (FLIM) is for example based on the measurement of the time that a fluorescence system spends in the excited state before returning to the ground state after light excitation. Lifetime evaluation by single-photon measurement with a time resolution below 50 ps rms can provide information about the localization of a specific fluorophore and about its surrounding environment [2], [3]. Moreover, in medical imaging, a time resolution below 200 ps FWHM in the detection of 511 keV gamma-rays in Positron Emission Tomography (PET) permits to apply the Time-Of-Flight (TOF) technique to allow for major improvements in sensitivity over standard PET methods [4]. These different applications therefore share a common need for highly time-resolved detection systems to improve event timing and to increase detector throughput. Electronic circuits are required for vacuum based detector technologies to assure resolutions below 10 ps rms and for solid-state photo-detectors to realize resolutions from tens to hundreds of picoseconds rms. The advantages of solid-state based detection system in comparison to vacuum based technologies in such context are to combine reasonably high-time resolution with higher spatial resolutions, better integration, lower sensitivity to magnetic field and lower costs.

The most stringent time requirements are found in Time Of Flight experiments (TOF) in HEP. In the TOF detector of the ALICE experiment, Multi-gap Resistive Plate Chambers (MRPCs) [5] are read out by front-end circuitry developed at CERN based on the so-called Nino architecture. These channels operate as amplifier-discriminators, allowing for output Low Voltage Differential Signals (LVDS) with less than 20 ps rms time resolution on their rising edge [6]. These circuits are directly read-out by high-performance time to digital converters (HPTDC) [7]. An overall time-resolution of 50 ps rms can be achieved with this readout in the ALICE experiment for a total of more than 150,000 operational readout channels [8]. The Nino circuit can be operated in single-ended or differential modes, and allows for input charge retrieval from the output pulse width measurement. The proposed architecture is of high interest for the direct readout of avalanche photo-diodes (APD) [9], silicon photomultipliers (SiPM) [10], silicon particle detectors [11], vacuum based photomultipliers [12] and MRPCs. While the circuit design remains simple, it allows for a direct adaptation to such variety of detecting device types. However, in order to be used in future highly integrated experiments for life-science, HEP or medical imaging, a higher integration of the channel is essential. The Nino architecture was therefore further optimized in order to decrease the power consumption and to allow for a higher channel density. The Irpics circuit was developed and is detailed in this letter. It integrates 32 channels based on the Nino architecture. The electrical characterizations show the high potential of application of the developed readout technique to highly integrated detection systems.

Manuscript received September 14, 2010; revised November 25, 2010; accepted December 12, 2010. Date of publication January 13, 2011; date of current version February 09, 2011.

M. Despeisse is with Photovoltaics and Thin Film Electronics Laboratory, Insitute of Microengineering, Ecole Polytechnique Fédérale de Lausanne, 2000 Neuchatel, Switzerland (e-mail: matthieu.despeisse@epfl.ch).

F. Powolny and P. Jarron are with CERN, CH-1211 Geneva 23, Switzerland (e-mail: pierre.jarron@cern.ch; francois.powolny@cern.ch).

J. Lapington is with the Space Research Center, University of Leicester, Leicester LE1 7RH, U.K. (e-mail: jon@lapington.com).

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Digital Object Identifier 10.1109/TNS.2010.2100409

TABLE I
PERFORMANCE OF THE NINO CIRCUIT IN 250 nm CMOS TECHNOLOGY

Nino 250 nm CMOS technology	
Nber of Channels	8
Power consumption	20 mW/channel
Peaking time	1 ns
Discriminator threshold	20 to 100 fC
Input resistance	30 to 100 Ω
Front edge time jitter	10 to 25 ps rms

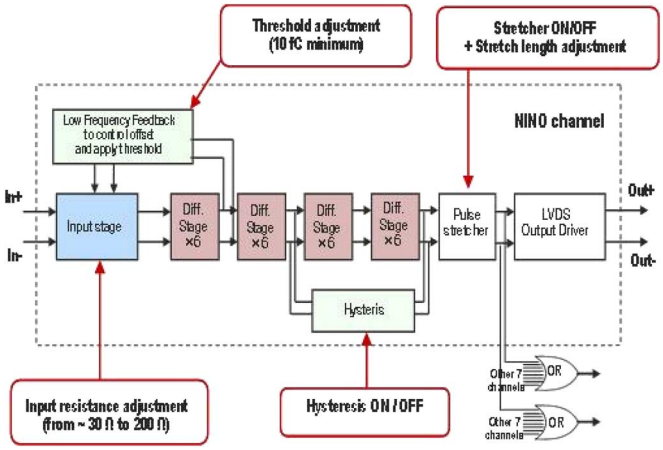

Fig. 1. Block diagram of the Nino architecture, comprising an input stage, 4 cascaded differential stages (each with a gain of 6, referred to as ×6 in the schematic), a feedback loop to control offset and apply threshold, a pulse stretcher and a LVDS output driver. The output connections to OR circuits displayed in this schematic are integrated in the Irpics circuit.

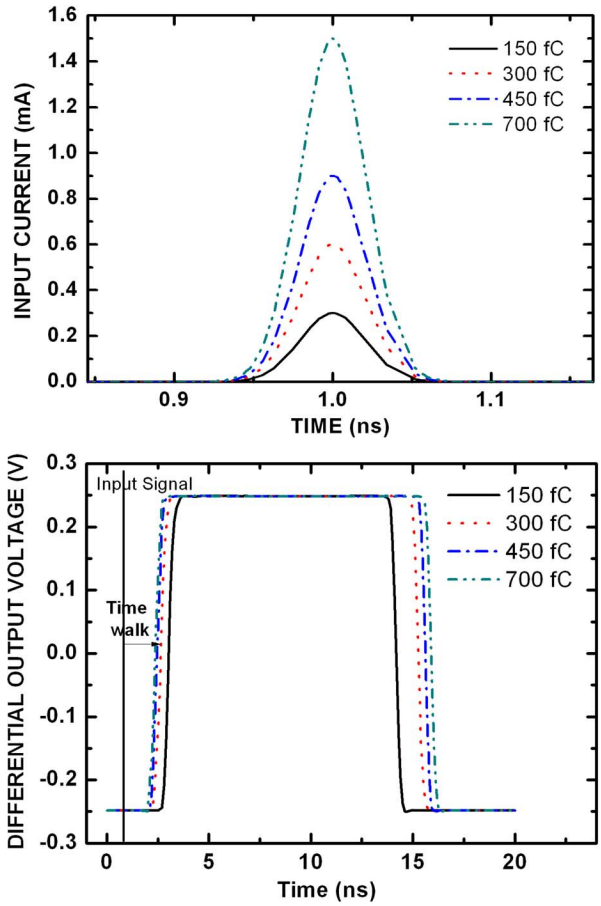

Fig. 2. Illustration of the Nino differential outputs: simulations for input charges varying from 150 fC to 700 fC, with typical signal shape corresponding to MCP detectors with a transit time spread of 50 ps rms. Pulse width increases and time walk decreases for increasing input charge.

II. FRONT-END READOUT ARCHITECTURE FOR HIGH-TIME RESOLUTION DETECTION

A. The Nino Architecture

While state-of-the-art TOF systems in HEP and medical imaging (PET) use flash ADCs processed by FPGA, or Constant Fraction Discriminators (CFDs), the Nino architecture is here proposed as an alternative solution. It is based on a time-over-threshold approach. It was first implemented in a 250 nm CMOS technology and its performances are summarized in Table I and detailed in [6].

A simplified block diagram of the readout architecture is shown in Fig. 1. The circuit is fully differential in order to obtain a large immunity against power supply and ground noises. The circuit can be efficiently used in both differential and single ended modes at its input. The input currents are sensed by the input current-to-voltage converter which is based on a balanced common-gate cascode stage, enabling a low input resistance on each circuit input ([6], Table I). For the readout of high capacitance (>2 pF) detectors such as MRPC or photomultipliers, this low input resistance permits to achieve high bandwidth, low crosstalk and to minimize signal reflection (by matching the circuit input impedance to the resistance of the transmission line connecting the detector to the circuit). The output voltages of the transimpedance input stage have an imposed DC offset acting as threshold as the differential signal is then amplified by 4 cascaded differential amplifiers. These stages provide a sufficient gain to reach saturation of the signal so that the circuit operates as a discriminator. The threshold is set by a voltage difference applied externally on two symmetrical inputs, acting on the DC stabilization feedback circuit and setting the DC voltage difference at the output of the transimpedance stage. This low-frequency feedback circuit is also used as the common mode rejection ratio circuit. A positive feedback loop circuit can also be enabled to add a small hysteresis on the discriminator threshold. Finally, a Low Voltage Differential Signal (LVDS) driver permits to have Nino outputs compatible with any LVDS receiver.

The Nino architecture enables the generation of LVDS pulses for a given input current. As the output pulse width corresponds to the saturation time of signal differences above a certain threshold, it can be approximated as a time over threshold technique [9]. The output pulse width increases for increasing input currents, as a result of the increasing saturation time of the differential amplifiers. It must be noted that the time walk between the input signal and the output pulse leading edge also varies as a function of the input current, decreasing for increasing charges, i.e. for increasing pulse width. These variations in the LVDS output signals are illustrated in Fig. 2 by simulation results obtained for input charges varying from 150 fC to 700 fC and corresponding to typical Micro-Channel Plate (MCP) detector signal shape for single photon detection.

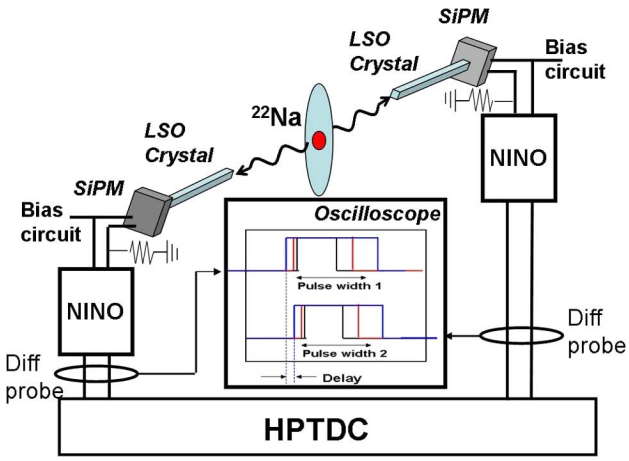

Fig. 3. Schematic of the coincidence setup for TOF-PET application using the developed readout chain: LSO scintillation crystals and SiPM photo-detectors readout by Nino electronics. The Nino outputs can be processed by the HPTDC circuit [7] or directly on an oscilloscope via differential probing.

The pulse width information hence encodes the input charge and permits to correct time walk variations induced by input currents with different amplitudes (even for a large dynamic scale). The LVDS receiver has therefore to provide the timing measurement of both leading and trailing edges in order to retrieve the exact timing and the input charge.

B. An Application to TOF-PET

In addition to the straightforward application of the Nino architecture to the readout of MCPs [12] or of MRPCs [6], this circuit was also shown to be promising for the readout of solid state photo-detectors [9]–[11]. For example, prototypes of TOF-PET channels were first developed at CERN, combining the Nino electronic readout with Avalanche Photodiodes (APDs) and with LSO scintillators [9]. Measurements done with a $^{22}\mathrm{Na}$ source emitting 511 keV γ-rays in coincidence have shown for these prototypes a coincidence time resolution of 1.6 ns FWHM [9]. The resolution was shown to be limited by the low APD gain ($\sim 10^2$) and by the photon production statistics in the scintillation process [9]. The impact of the Nino electronics on the time resolution is marginal in this set-up. Second generation of TOF-PET channels incorporating Silicon Photomultipliers (SiPM) instead of APDs were then constructed, in order to benefit from the higher gain of the SiPM to trigger the signal event on the first photons produced by the scintillation. The system uses LSO crystals of $3 \times 3 \times 15\ \mathrm{mm}^3$ readout by SiPMs (or MPPC) from Hamamatsu, as shown in Fig. 3.

While SiPM readout is so far typically configured with a single-ended connection to the front end amplifier input [13], [14], we propose a differential connection to the front end amplifier (Fig. 4). A connection scheme was developed to connect both the anode and cathode ports of the SiPM to the differential inputs of the Nino circuit. This type of input connection has the advantage of superior rejection of ground and supply voltage noises, a key feature for a fast multichannel readout ASIC for

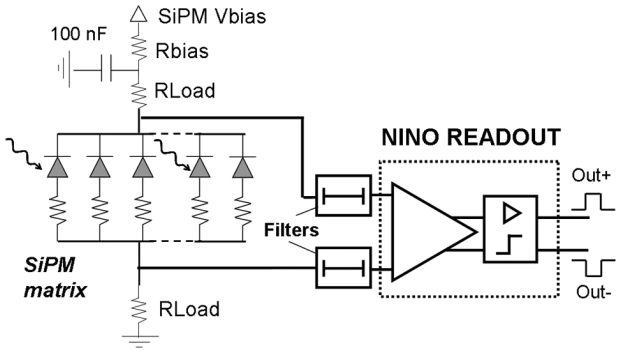

Fig. 4. Differential readout scheme of a SiPM matrix with the Nino circuit via optimized filter connections realized on printed circuit board.

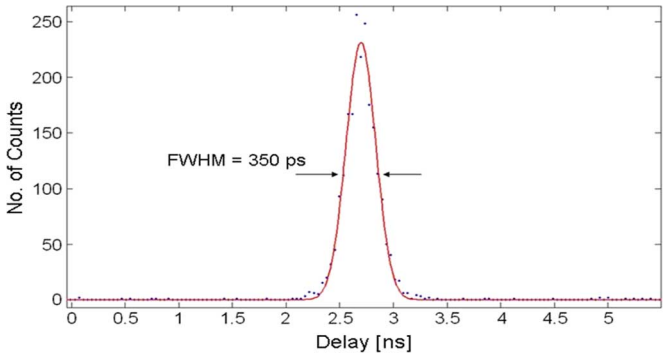

Fig. 5. Coincidence time resolution after photopeak selection and time walk correction.

TOF-PET applications where common mode noise can easily be transformed into electronic time jitter.

With the developed TOF-PET channels, the γ-ray energy can be estimated through the Nino output pulse width; while the timing performance is determined from the output pulse leading and trailing edges time information. An automated data processing can be realized by using the HPTDC circuit developed at CERN [7] and already interfaced with Nino in the ALICE experiment. In the present tests, the data processing was realized by directly reading out the differential output signals with a digital oscilloscope Lecroy Wavepro 7100; and by recording the leading edge and trailing edge times of pulses in coincidence. Off-line data analysis was carried out for photo-peak selection and time walk correction (as defined in Section III). The SiPM high gain ($\sim 10^6$) permits to set the Nino threshold at the level of the first detected photons, improving the timing resolution resulting from the photon production statistics [10]. The coincidence time resolution with the developed channels is thus measured down to 350 ps FWHM, as shown in Fig. 5, demonstrating that the system is precise enough to perform TOF-PET. The main remaining limitations on time resolution are then supposed to come from the crystal geometry (a reduced crystal length would result in decreased photon transit time and time jitter) and from the SiPM single avalanche signals triggered by thermal noise [10]. It should be noted that similar time resolution of $\sim$390 ps FWHM could be achieved with PMTs and CFDs [10]. This further suggests that the strongest limitations still arise rather from the crystal and the photon production statistics than from intrinsic timing capability of the front-end electronics.

III. The Irpics Multi-Channel Integrated Circuit

A. Low-Power Nino Channel Integrated in the Irpics Circuit

The first Nino circuit shows the great potential of the proposed architecture for high time resolution readout of different types of detectors. However, it exhibits a power consumption of about 20 mW for the amplifier-discriminator stage and of 12.5 mW for the output LVDS driver, which can still limit its implementation into highly integrated systems. In order to decrease the biasing currents of the different stages of the circuit and to allow for a higher integration potential, several optimizations were carried out in the full discriminator chain, leading to the design in a 250 nm CMOS technology of the Irpics circuit. This chip integrates 32 optimized channels, has a modified pin-out to simplify multi-chip layout, and is available with internal or external LVDS output termination to allow for an optimum compromise between power dissipation and footprint.

The circuit architecture of the optimized Nino channel is similar to that shown in Fig. 1. The input impedance depends on the current biasing the input stage branches. This current can be adjusted externally with a digital potentiometer, allowing for an input resistance to be set between 30 and 200 Ω. The input amplifying stage is then followed by 4 cascaded differential stages, a stretcher option to increase by about 8 ns the output pulse width, and a LVDS driver. The circuit power consumption could be limited by reducing the currents in each of these stages. This could be realized while maintaining similar time-resolution and similar threshold levels than for the initial circuit thanks to a careful re-sizing of all transistors of the circuit, of all resistors, and by an appropriate layout to limit parasitic capacitances at some critical nodes of the circuit. This full re-design of each part of the channel could lead to a factor 2 reduction in power consumption. The optimized channel, also developed in a 250 nm CMOS technology, shows a power consumption of 10 mW, while the consumption of the output LVDS driver could also be reduced to 7.5 mW.

The Irpics chip was then designed, integrating 32 channels of the optimized Nino version. In comparison to the 8 channels chip, several additional features were also added in order to provide higher flexibility for application in highly integrated systems. A test circuitry was designed for the circuit calibration. Injection capacitances are integrated in the chip and connected to each channel input. They can be addressed externally and are independent of the channels input connected to the detector under readout. This allows for a precise calibration of each channel simply by applying voltage steps to the dedicated test pads of the circuit, resulting in a fast current pulse at the input of the channel under calibration. This can be done while the electronic readout is connected to the detector, so that the calibration of each channel can be realized in the operating conditions of the device (with the appropriate input capacitance load). Another additional feature in the Irpics circuit is that each channel output has also a parallel connection to an OR circuitry. There are 4 different OR circuits each grouping 8 channels of the chip, and delivering LVDS output signals. For each OR circuit, the output signal is therefore triggered in the case that at least one of the 8 channels grouped onto the corresponding OR circuit was triggered. Finally, the chip pin-out was optimized to have the input

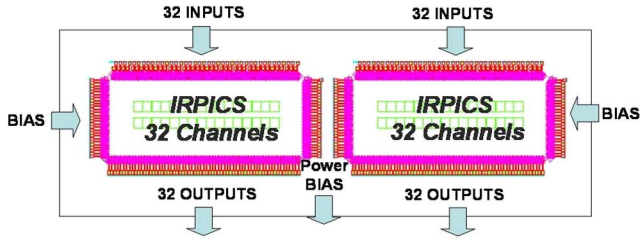

Fig. 6. Schematic representation of the possible mirror-like mounting of the Irpics circuit to allow for increased integration potential.

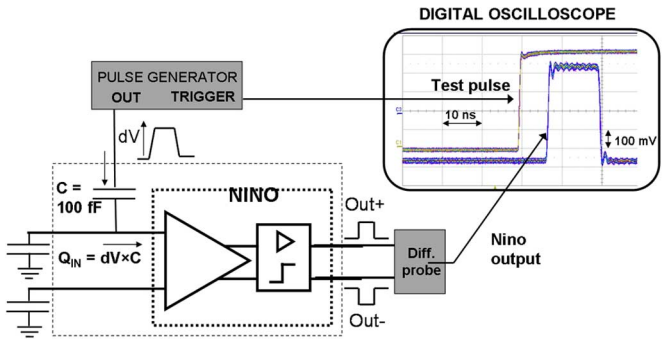

Fig. 7. Schematic representation of the test set-up for an individual Irpics Nino channel using the integrated injections capacitance and a voltage pulse generator.

pads on the top side of the chip, the output pads on the bottom side, and the pads for the chip biasing at the left and at the right sides of the circuit. The biasing scheme was intentionally realized so that connection on either the left side or the right side only is sufficient, so that either the right or left side pads can be let floating. This permits an improved integration of the circuit onto the printed circuit board, as two circuits can be mounted in a mirror-like configuration and be both biased, as shown in Fig. 6. This leads to an improved integration and to an equivalent 64 channels design.

B. Performance Evaluation of the Irpics Circuit

The performances of the 32 channels of the Irpics circuit were evaluated by generating input current pulses by applying voltage steps to the 100 fF injection capacitances integrated in the chip between the input pads and each channel input, while the input pads of each channel were connected to a load capacitance of 5 pF to reproduce a photo-detector terminal capacitance (see Fig. 7).

A pulse generator with output signals exhibiting 800 ps rise and fall times was used to generate the test signals in each channel. Measurements of each channel output were then carried out using a differential probe connected to a digital oscilloscope Lecroy Wavepro 7100. The pulse generator trigger signal was also fed to the oscilloscope. The time differences between the trigger signal and the leading edge and trailing edge of each output signal were recorded, as shown in Figs. 7 and 8.

For each channel, measurements were carried out for different input signal amplitudes, set using different voltage pulse amplitudes from the generator, resulting in total charges of 20 fC to 250 fC. For each channel and for each input charge level, 1000 measurements of the LVDS output signals were recorded.

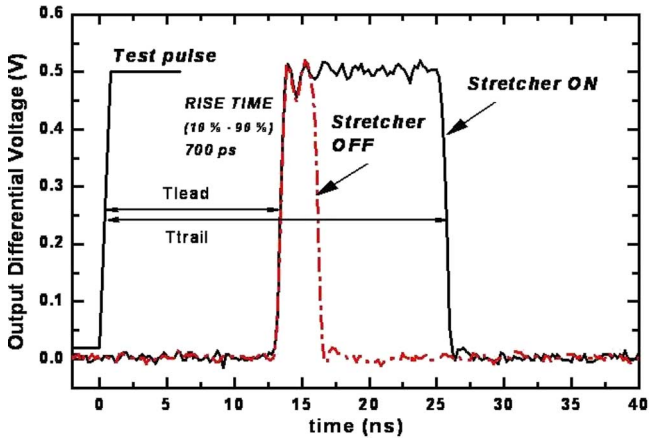

Fig. 8. LVDS Output Signal Shape measured with a differential probe on one of the 32 channels of the Irpics circuit. The two signals correspond to the same input current, and to the case of stretcher switched off or on.

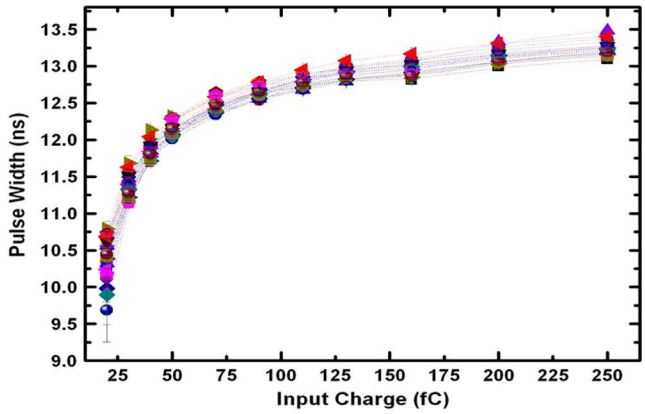

Fig. 9. Measured pulse width as a function of applied input charge for the 32 channels of the Irpics circuit.

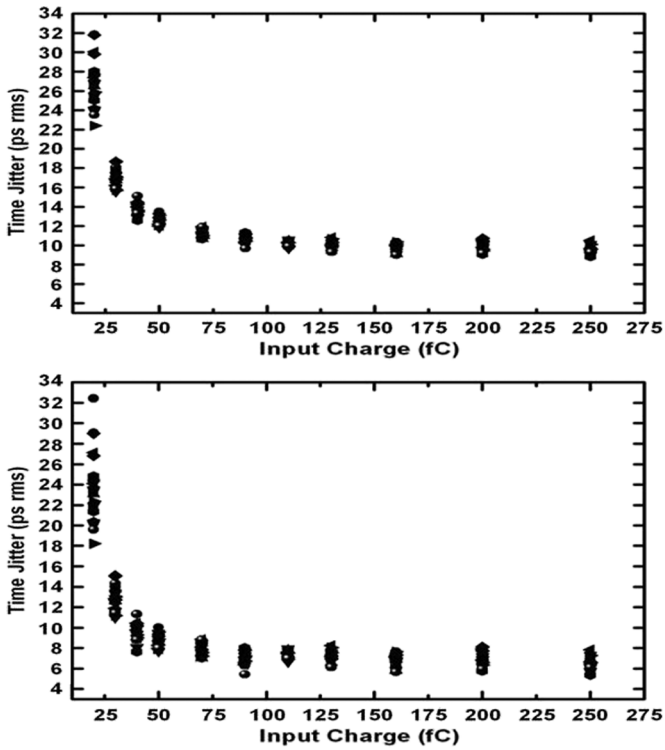

Fig. 10. Time jitter on the LVDS output pulse leading edge estimated from 1000 pulse measurements for each input charge, and for the 32 channels of the Irpics circuit. Top: measured time jitter, bottom: measured time jitter corrected from the pulse generator and the oscilloscope contributions.

For each measurement, the time difference t_{lead} between the leading edge of the LVDS output pulse and the pulse generator trigger was recorded. In addition, the time difference t_{trail} between the trailing edge and the trigger was also acquired for each measurement. For each channel and each input charge, a set of 1000 measurements of (t_{lead}, t_{trail}) was thus acquired (as shown in Fig. 8), so that pulse width, time-walk and time precision on both leading edge and pulse width are measured. The output LVDS pulse exhibits 700 ps rising and falling times, and can have a pulse width of 1.5 to 5 ns, or a pulse width of 10 to 14 ns if the pulse stretcher option is used (so as to ease the LVDS readout by HPTDC chip, [6]). The typical signals measured with a differential probe at the LVDS output of a channel are shown in Fig. 8, illustrating the effect of the stretcher option for 2 similar input signals, the small ringing on the output pulse originating from measurement artifacts.

The output pulse width $(t_{trail} - t_{lead})$ variations with respect to the input charge measured with the stretcher switched on are displayed in Fig. 9 for the 32 channels. These experimental results show very close matching between all 32 channels, with a typical pulse width varying from 10 ns to 13.5 ns for input charges from 15 fC to 250 fC, respectively. While this shows the possibility to retrieve charge information from the output pulse width measurement, a non-linear relation is also observed, with a maximum sensitivity for the lower charges. In order to efficiently use the charge encoding possibilities of the circuit with an optimum resolution, the threshold level of the circuit must therefore be tuned so as to maximize the sensitivity around the working point of a specific application. Achievable resolutions are therefore directly dependent on the input signal shape, amplitude and dynamic range in the application.

The time jitter on the output pulse rising edge was first retrieved for each input charge from the 1000 corresponding measurement points, and for each channel. This jitter represents the jitter measured for signals with a similar charge at the circuit input. Measurements show a very high time resolution of 10 ps rms for charges above 100 fC (Fig. 10). Such low values have contributions from the pulse generator and oscilloscope jitters, estimated to be of 8 ps rms. The intrinsic time-jitter performance of the Irpics channels can thus be evaluated by assuming a quadratic sum of these different contributions. Corrected results are shown in Fig. 10, demonstrating a time jitter between 5 and 7 ps rms for all the 32 channels and for charges above 100 fC. For charges between 20 fC and 100 fC, time jitters below 25 ps rms are measured.

C. Time-Walk Corrections and Minimum Time-Resolution Realized With the Irpics Circuit

A characteristic of the Nino architecture is that the circuit output pulse leading edge time t_{lead} depends on the input signal amplitude, as already illustrated in Fig. 2. All the t_{lead} time measurements acquired for the different input charges on one of the

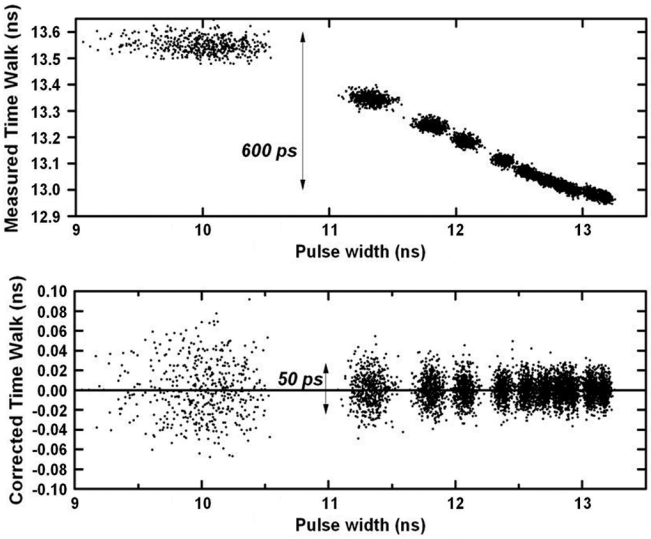

Fig. 11. Top: Measured Time walk on the LVDS output pulse leading edge versus measured pulse width, with display of 500 pulse measurements for each input charge, for a single channel (channel 10) of the Irpics circuit. Bottom: Time walk after off-line corrections applied to compensate variations of time walk with pulse width, with display of 500 pulse measurements for each input charge, for a single channel (channel 10) of the Irpics circuit.

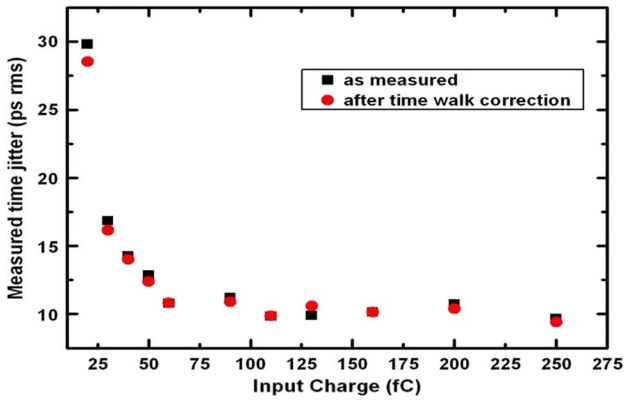

Fig. 12. Measured Time jitter on the LVDS output pulse leading edge estimated from 1000 pulse measurements for each input charge, and for a single-channel (channel 10) of the Irpics circuit. Comparison between measured time jitter and time resolution after time walk corrections.

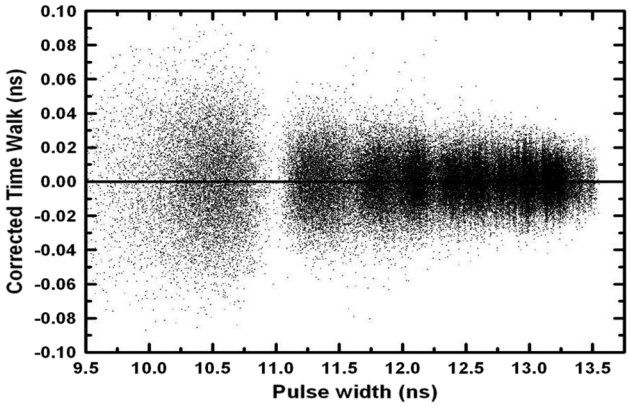

Fig. 13. Time walk after off-line corrections applied to compensate variations of time walk with pulse width, with display of 500 pulse measurements for each input charge per channel, and with performance of all the Irpics circuit 32 channels shown.

32 channels are displayed in a scatter plot in Fig. 11 as a function of the measured pulse width. The time walks presented include systematic walk due to the propagation of the signal to the oscilloscope and a variable contribution t_{lead_var} due to the signal formation in the electronic channel. These time walk variations are contained in clusters of less than 1 ns for input charges varying from 15 fC to 250 fC. From the calibration measurement shown in Fig. 9, it is possible to retrieve an equation defining the average relation between time-walk variation t_{lead_var} and pulse width. This relation $t_{lead\_var} = f(t_{trail} - t_{lead})$ permits to estimate from the data set (t_{lead}, t_{trail}) the absolute t_{lead_var} information. It therefore allows for correcting the time-walk variations, so that $(t_{lead} - t_{lead\_var})$ is used as absolute measured time information. This technique, applied off-line, permits to have a high-time resolution even for input signals amplitude varying on a large dynamic scale. In the presented study, the relation used for the time walk correction is a simple linear regression between the 12 calibration points (each point is defined by the average time walk measured for a given average input charge).

This time walk correction procedure was applied event by event, leading to the scatter plot shown in the bottom of Fig. 11. For each cluster of data points, the variations now correspond to the uncertainty in the time information t_{event} that can be expected for a signal with such input charge.

The measured and corrected time walk are shown in Fig. 11 for one of the 32 measured channels, while the measured time jitter and the time resolution determined after time walk correction are presented in Fig. 12.

The uncertainties in the measured and corrected time information are of about 30 ps rms for a 20 fC input charge and below 10 ps rms for charges above 100 fC (here limited by the generator and oscilloscope noises). It can be noted here that the measured jitter at a fixed charge and the retrieved time resolution after time walk correction are very close, thanks to a sufficient time precision on the trailing edge to not impact too much overall time precision.

The time walk correction procedure was then applied to all measured data points acquired for the 32 channels, and the resulting measured variations in the leading edge for all channels can be seen in the scatter plot of Fig. 13, which displays all the measured and corrected points.

Finally, the overall time resolution of the full circuit can be estimated, after both time walk corrections and corrections of the pulse generator and oscilloscope additional noises. The resulting performances obtained are shown for the 32 channels on Fig. 14. The overall excellent time-resolution measured for an input charge Q can therefore be perfectly retrieved in the case of a system involving input signals varying onto a large dynamic scale. This is realized thanks to the channel calibration which permits to extract the function relating time walk and pulse width, and thanks to the time walk correction procedure applied off-line to the measured data points. The overall time precision which can be attained for a particular application and with a particular detection system will then depend on the statistical distribution of the input signals amplitude which will be readout during the experiment, as low charge signals exhibit a higher time uncertainty than signals with a charge higher than

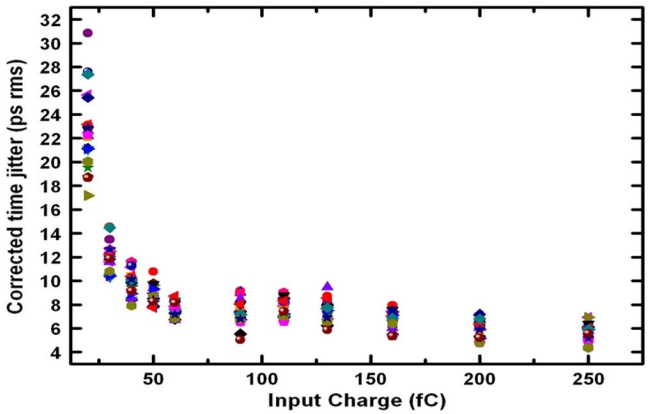

Fig. 14. Overall time resolution on the LVDS output pulse leading edge estimated from 1000 pulse measurements for each input charge, and for all channels of the Irpics circuit. Corrections are applied to compensate additional noise from the pulse generator and the oscilloscope and to correct time walk variations due to pulse width variations.

100 fC. In the case of high input signals (>100 fC), one can note that very low time resolutions down to 4 to 7 ps rms are measured systematically on all 32 channels of the Irpics circuit.

IV. Summary

The Irpics integrated circuit was developed in a 250 nm CMOS technology to allow for the construction of highly integrated time-resolved detection systems for future experiments in HEP, life-sciences, bio-technologies or material sciences. It integrates 32 channels of low-power time-resolved amplifier-discriminators called Nino. The proposed readout architecture is based on a time over threshold approach, and has a high potential for the readout of solid state photo-detectors and of detectors based on vacuum technologies. While high-time resolution can be achieved even for input signals varying on a large dynamic scale, the circuit technique can also permit to estimate the input signal charge. An integrated circuitry permits to do a calibration of each channel in operating conditions (i.e when connected to the detector), allowing to extract the function relating time walk and pulse width, and the function relating pulse width and input charge. These calibrations then allow for the time walk correction procedure applied off-line to the measured data points and for the estimation of the input signal charge. The performances of the Irpics circuit measured on all 32 channels and presented in this paper are detailed in Table II.

The low-power consumption of the circuit (<10 mW/channel), the high time resolution (measured down to 4 ps rms), the input charge encoding and the high integration level of the developed readout technique therefore show that the Irpics circuit and the Nino architecture concept can be of high interest for communities requiring multi-channel high time resolution detection systems.

TABLE II
Performance of the IRPICS Circuit in 250 nm CMOS Technology

IRPICS 250 nm CMOS technology	
Number of Channels	32 – chip pin out allowing for 64 channels configuration
Power consumption	10 mW/channel
Peaking time	700 ps
Discriminator threshold	20 to 100 fC
Input resistance	30 to 200 Ω
Front edge time jitter	4 to 25 ps rms
Additional features	Calibration circuitry + OR circuits

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