ATLAS ABCD Hybrid Fatal Charge Dosage Test

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ABSTRACT: The Semi-Conductor Tracker (SCT) in the ATLAS experiment at the Large Hadron Collider (LHC) could be subject to various beam loss scenarios. If a severe beam loss event were to occur, it would be beneficial to know how SCT components would be affected. In the SCT detector modules, a key component is the ABCD application specific integrated circuit (ASIC), the onboard readout electronics of the system. This ASIC has design specifications that it should withstand a 5 nC charge application within 25 ns, which is the period of the LHC bunch crossing. The first test performed is designed to test this limit, reaching a maximum of 10 nC deposited in 25 ns.

One model for beam loss predicts that a large charge, of the order of 10^6 MIPS, could be incident on the detector. According to detector studies, this causes a local field breakdown between the backplane of the sensor, held at 450 V, and the strips. In this case the signal seen on the readout strip has a rise time of about 1 μs due to a charge screening effect. A second test is designed to test this discharge scenario, with a maximum of 90 nC deposited in 1 μs.

KEYWORDS: Front-end electronics for detector readout; Radiation-hard electronics; Digital electronic circuits.

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Contents

1. Introduction

The Semi-Conductor Tracker (SCT) in the ATLAS experiment at the Large Hadron Collider (LHC) operates near the beam and could be subjected to large amounts of instantaneous charge deposition in the event of beam loss due to a failing magnet or some other type of beam steering problem. The original design specification for the ABCD ASIC (application specific integrated circuit) included a requirement that each channel be able to withstand a voltage step of 450 V with a cumulative charge of 5 nC within 25 ns (the period of the LHC bunch crossing) in order to handle such beam loss scenarios. The 450 V requirement covers potential breakdown between the sensor backplane (held at up to 450 V) and the strips that provide input to the readout circuit, which could occur if sufficient charge is deposited in the sensor. The 5 nC limit was an estimate of the charge deposited per strip at the time of the ABCD final design review in 2001. To meet this requirement, the input channels of the ABCD include protection diodes designed to absorb this charge and voltage. Analyses of the ABCD circuit design including simulations were performed showing that it would meet the requirements but no tests were performed on fabricated parts prior to construction. Some tests have since been performed exposing assembled modules (silicon sensor plus readout chip) to laser pulses to simulate the beam loss and some electrical tests have also been attempted directly on the ABCD chip [1]. The latter produced variable results, which may have been due to the circuit designed to deliver the charge pulse to the ABCD, which employed a mechanical switch. The purpose of the study reported was to reproduce the test of the ABCD isolated from a sensor in order to validate the chip specification directly with an improved apparatus for injected large charge pulses and to provide a test apparatus for future studies. The charge injection circuit used an FET switch and could select various pulse rise times by choice of components. Controlling the rise time is essential to accurately reproduce physical beam loss scenarios especially for future studies.

The two parts of the chip specification (450 V and 5 nC in 25 ns) were separated into two test sequences with a longer rise time of 1 μs for the 450 V component since our sensor studies have shown that breakdown develops more slowly due to charge screening [2]. To test beyond the specification in order to find the failure point, the charge deposition test scanned up to the equivalent of 10 nC in 25 ns and the 450 V test ran up to 90 nC in 1 μs.

2. The Test Program

2.1 Experimental Apparatus

The experimental apparatus is shown in Fig. 1. The 12-chip ABCD hybrid is shown at the top, mounted on a cooling block. Two of the chips, each containing 128 readout channels, have been wired for testing. On the bottom left are the charge injection circuits, connected to the hybrid through a jumper board. The data readout circuitry is seen on the right, which connects the hybrid to a standard SCTDAQ system so that the functionality of the ABCD chips could be verified before and after charge injection.

The diagram in Fig. 2 shows a simplified version of the charge injection circuit. The MOSFET gate is driven with commercial high-side gate driver ICs, and the 1 Ω resistor is used to measure the current flowing into the chip. There are two of these circuits that are used in the study: one that is capable of up to 80 V step signal with transition time of 40 ns [1], and another that is capable of up to 450 V step signal with transition time of 1 μs.

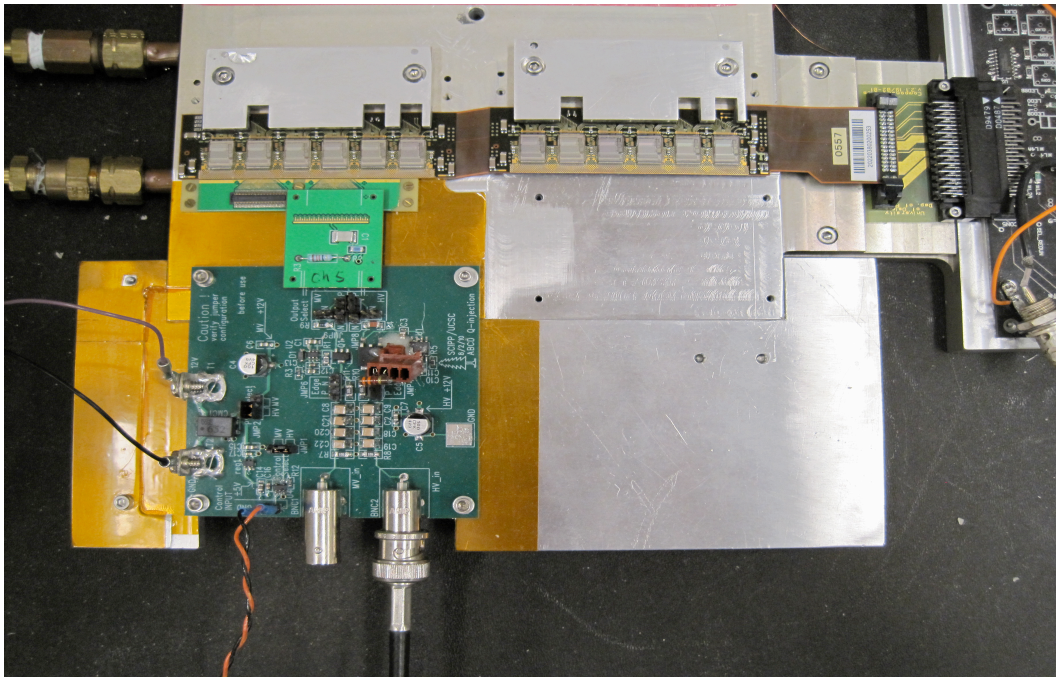

Figure 1: Experimental Apparatus

[1] We assume that the most important feature of the input protection circuity is the amount of current it can absorb. We, therefore, scale the injected charge by 5/8 to achieve the equivalent 25 ns test.

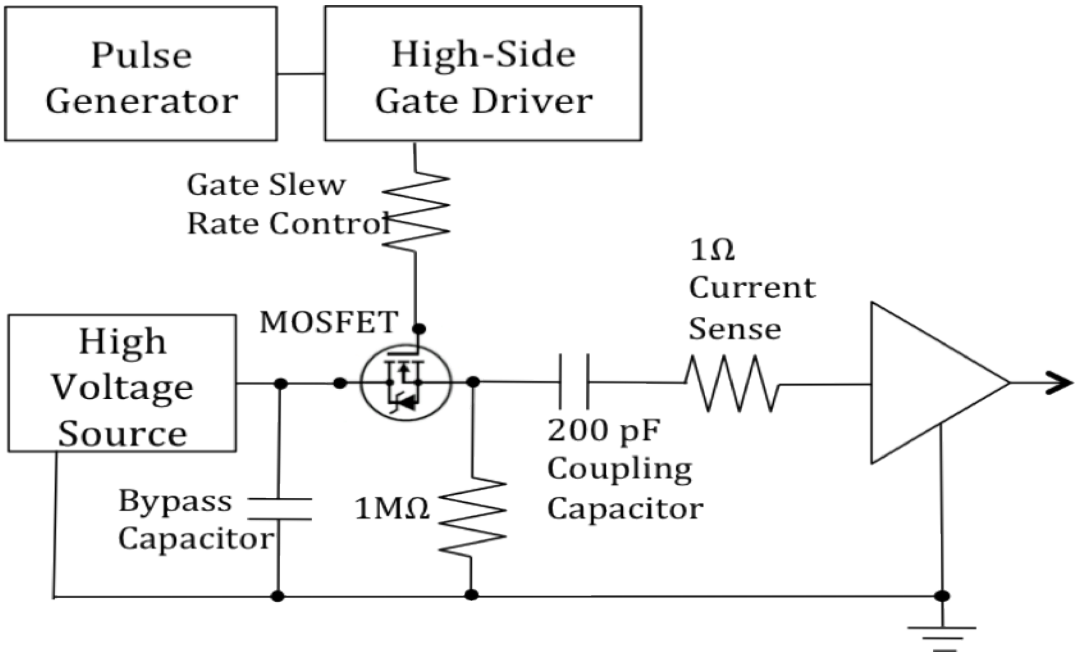

Figure 2: Block Diagram of the Charge Injection Circuit

2.2 Test Validation

Two checks were performed to ensure the tests were operating as designed. First, a check was made to show that the current into the ABCD channel from the rising edge of the voltage step is much greater than from the falling edge. Because the magnitude of the charge deposited ($Q = CV$) is equal, and $I = \Delta Q/\Delta t$, the differentiating factor is the duration of the charge deposition. The oscilloscope reading in Fig. 3 shows the voltage step in white and the amplifier input in yellow. It is clear from these measurements that the duration of the rising edge is much shorter than that of the falling edge. Thus, the current from the rise of the voltage step is much greater and the effects of the falling edge can be ignored.

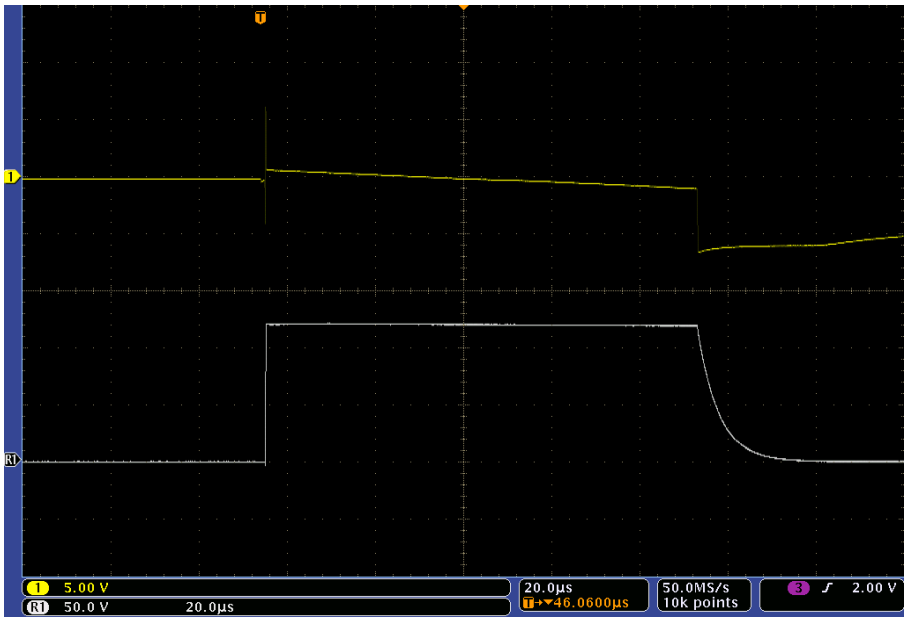

Figure 3: Voltage Step in White, ABCD Input in Yellow

The second check was to make sure the desired amount of charge was deposited into the ABCD channel in the desired amount of time. To do this, the voltage across the 1 Ω current sensor is measured. This gives a measurement of the instantaneous current dQ/dt. By integrating over a certain period of time, the charge deposited can be found. The oscilloscope reading in Fig. 4 shows this measurement, with the voltage on each side of the 1 Ω resistor in white, and the difference in red. In this case, there is about 8 nC deposited in 40 ns and slightly more than 5 nC deposited in the first 25 ns, thus exceeding the ABCD specification.

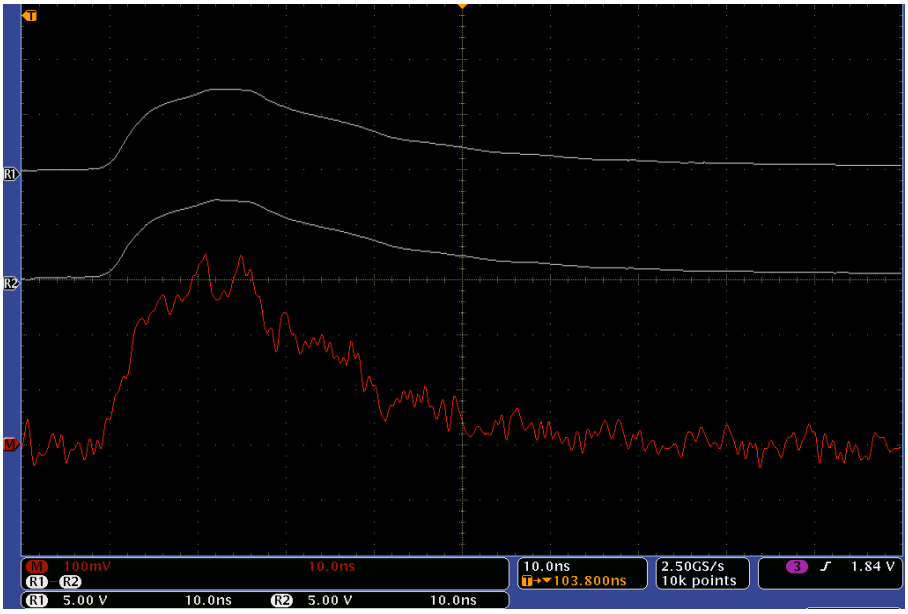

Figure 4: Voltage on Either Side of Current Sense Resistor in White,
Difference of the two Traces in Red Equals Current Injected.
Note the different scale of the latter trace.

2.3 Test Procedure and Results

To test the performance of the chips, the charge injection circuit was connected to the input of a single channel. The pulse generator was turned on for 10 s with a 500 ms period, resulting in 20 charge pulses delivered to the channel. The charge injection circuit was then disconnected from the ABCD chips. The data readout system, called SCTDAQ, was then used to perform response curve and three-point gain tests to determine whether the chip was still properly functioning.

The first test was aimed at validating the ATLAS collaboration specification that the ABCD survive 5 nC deposited in 25 ns, or an average of 200 mA. In the tests that validated this specification, two different input voltages were used: 40 V and 80 V. With 80 V input, the charge deposited was 16 nC in 40 ns, which is an average of 400 mA, double the specifications. For this test, five channels were tested on one chip, along with two on another chip. No failures were seen on any of the channels.

The second test was aimed at testing a situation where a large charge deposition causes a local field breakdown between the backplane, held at 450 V, and the strips. Charge screening effects result in a long signal rise time of about 1 μs. With 450 V applied to the coupling capacitor of 200 pF, the charge applied to the ABCD is 90 nC. For this test, five channels were tested on one chip, along with two on another chip. Again, no failures were seen on any of the channels.

Input Voltage	Coupling Capacitor	Charge Deposited	Length of Pulse	Average Pulse Current	# of Channels Tested	# of Pulses/Channel	Test Results
40 V	200 pF	8 nC	40 ns	0.2 A	7	20	Pass
80 V	200 pF	16 nC	40 ns	0.4 A	7	20	Pass
450 V	200 pF	90 nC	1 μs	0.09 A	7	20	Pass

Table 1: Results of Charge Deposition Tests of the ABCD ASIC

Note: the first row (8 nC in 40 ns) is the equivalent current to 5 nC in 25 ns, the ABCD spec.

3. Conclusion

In the tests performed, no failures were seen in the ABCD ASIC. The ABCD channels were able to survive current pulses of 90 mA, 200 mA and 400 mA, twice the magnitude specified in the design.

Further tests are currently being explored. In a true LHC beam loss, charge could build up across many channels of the sensor for hundreds of microseconds before the beam is dumped. This could result in large area sensor breakdown, which would lead to the charge stored in the hybrid bias filter to be distributed across the readout channels connected to the affected strips. This could potentially lead to much greater charge injection quantities into a single chip than have been studied thus far. We plan to first understand the dynamics and limits of the beam loss scenarios, translate those into more realistic requirements for the readout chip robustness and then adapt our equipment to test the ABCD against those limits.

Acknowledgments

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