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The Gigabit Link Interface Board (GLIB), a flexible system for the evaluation and use of GBT-based optical links

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ABSTRACT: The Gigabit Link Interface Board (GLIB) is an evaluation platform and an easy entry point for users of high speed optical links in high energy physics experiments. Its intended use ranges from optical link evaluation in the laboratory to control, triggering and data acquisition from remote modules in beam or irradiation tests. The GLIB is an FPGA-based Advanced Mezzanine Card (AMC) conceived to serve a small and simple system residing either inside a Micro Telecommunications Computing Architecture (μTCA) crate, or on a bench with a link to a PC. This paper presents the architecture of the GLIB, its features as well as examples of its use in different setups.

KEYWORDS: Data acquisition circuits; Modular electronics; Digital electronic circuits

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1 Introduction

The Gigabit Link Interface Board (GLIB) is an evaluation platform and an easy entry point for users of high speed optical links in high energy physics experiments. Its intended use ranges from optical link evaluation in the laboratory to control, triggering and data acquisition from remote modules in beam or irradiation tests. Each GLIB card can process data to/from four Small Form Factor Pluggable Plus (SFP+) transceiver modules, each operating at bi-directional data rates of up to 6.5 Gbps. This performance matches comfortably the specifications of the GigaBit Transceiver (GBT) / Versatile Link project [1, 2] with its targeted data rate of 4.8 Gbps. In its simplest form, one GLIB board thus interfaces with up to four GBT channels.

Figure 1 highlights the baseline configuration of a GBT — Versatile Link — GLIB system. On the left side, front-end (FE) ASICs are electrically connected to the GBT ASIC through e-links [3] while the GBT high-speed serial data streams are converted to/from the optical domain through the Versatile Link FE transmitter/receiver. On the other end, the GLIB converts data to/from the optical domain, implements the GBT protocol and codes/decodes the user payload at the link back-end.

The GLIB I/O capability can be further enhanced with two FPGA Mezzanine Cards (FMCs) [4]. This gives users the flexibility to adapt the GLIB interface to their system, for instance by adding connectivity to the Timing, Trigger and Control (TTC) network at the backend, or connecting to e-links at the front-end. Figure 2 illustrates a case where two GLIB boards are interconnected

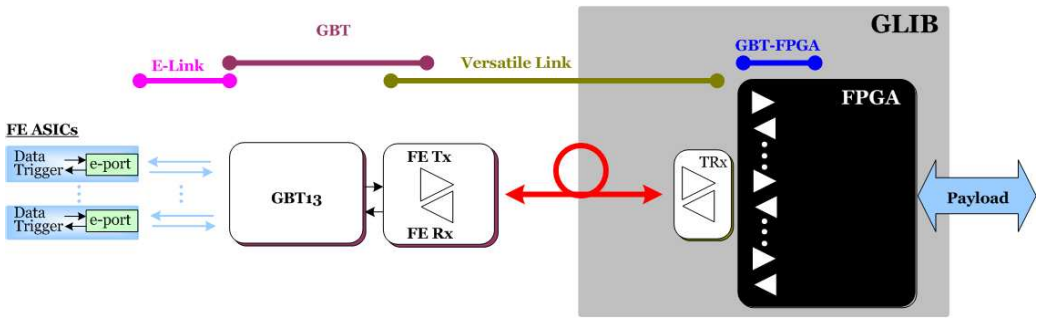

Figure 1. The GLIB board in a GBT-Versatile Link system.

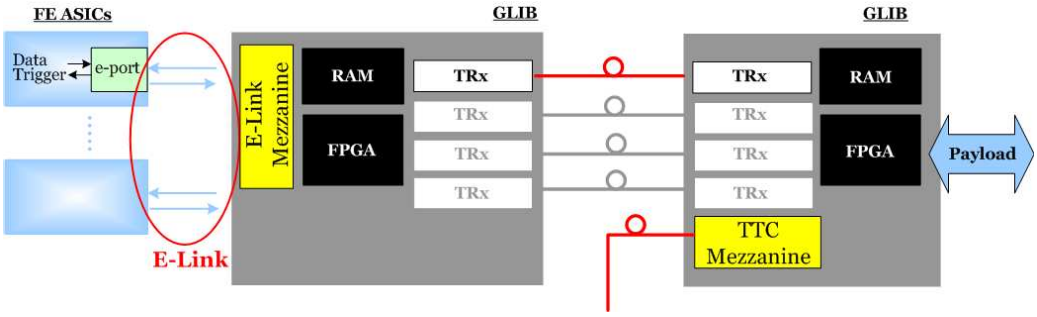

Figure 2. Back-to-back interconnected GLIB boards with customization mezzanines (TTC and E-Link).

back-to-back, allowing implementing and experimenting with GBT-based systems well before full-fledged GBT ASICs become available.

2 Implementation

The GLIB is an Advanced Mezzanine Card (AMC) [5] in Double-Width Mid-Size format (180 mm $\times$ 148 mm $\times$ 18 mm) conceived to serve a small and simple system residing either inside a Micro Telecommunications Computing Architecture (μTCA) [6] crate or on a bench with a link to a PC. Figure 3 shows a block diagram of the GLIB. The card is based on the XC6VLX130T FPGA of the Virtex-6 family by Xilinx Inc. The FPGA includes twenty Multi-Gigabit Transceivers (MGTs) operating at up to 6.5Gbps that are organized in groups of four (quads).

Concerning the AMC high speed serial connectivity, the GLIB provides two Gigabit Ethernet (GbE) and two 2nd generation four-lane PCI Express (PCIe Gen2 4x) interfaces. It is important to mention that the GLIB gives users the possibility of implementing various other high speed serial data protocols (for custom applications) instead of PCIe. This is possible mainly thanks to GLIB's sophisticated clock distribution circuitry that is based on cross-point switches and programmable clock multipliers. This circuitry offers a large selection of input clock sources (AMC clocks, the FMC clocks, front panel clock connector or on-board oscillators).

The two high-pin-count FMC sockets each provide up to 80 user-specific differential I/O pairs directly connected to the FPGA as well as two differential clock inputs and two differential clock outputs. The primary FMC also provides four optional 6.5Gbps transceiver lines, thus allowing extending the optical I/O capability to eight links by using e.g. a quad-SFP+ FMC[1] that is commercially available. Additionally, many other FMC functionalities could be implemented such as:

- FMC for TTC reception that could be implemented either based on custom ASICs or commercial Clock and Data Recovery ICs.
- E-link FMCs for direct communication with front-end modules not equipped with GBT.
- Other optical interface extension FMCs equipped with other types of optical modules where various protocols could be implemented (e.g. 10 Gigabit Ethernet).

[1]The maximum component height allowed on the component side of a mid-size AMC is 12.9 mm. The maximum height of an FMC with 8.5 mm and 10 mm stacking height is 11.4 mm and 12.9 mm, respectively. A 10 mm stacking height FMC can accommodate SFP+ cages, since their height is typically 9.7 mm.

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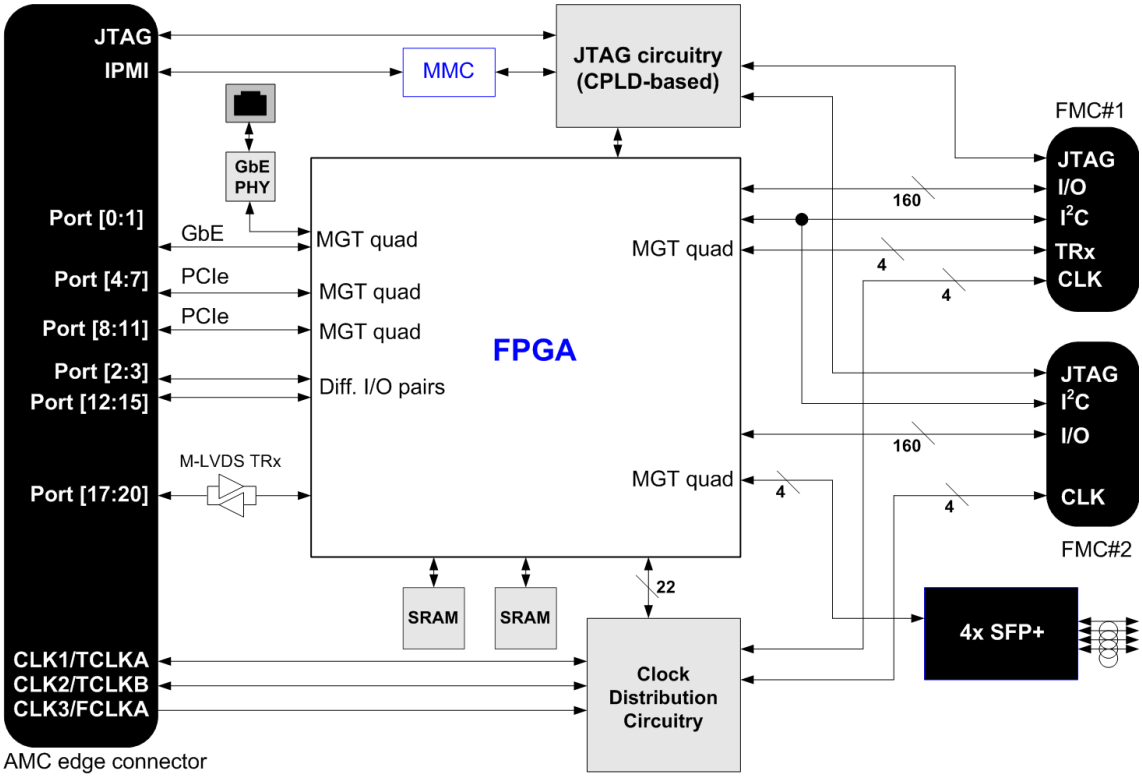

Figure 3. Block diagram of the GLIB AMC.

For the board initialization when in an xTCA environment as well as for other management tasks (e.g. temperature/voltage monitoring) a Module Management Controller (MMC) mezzanine card [7] is used. The MMC is based on a microcontroller by ATMEL.

For configuration purposes, a very flexible Joint Test Action Group (JTAG) circuitry based on a Complex Programmable Logic Device (CPLD) is also available. The CPLD acts as a JTAG switch selecting the JTAG master source between the dedicated JTAG connectors, MMC or AMC JTAG lines for the configuration of the FPGA and the associated EEPROM. The JTAG switch is also useful for boundary scan testing purposes.

The GLIB carries a GbE PHY as well as an Ethernet plug in order to interface to a PC through a standard Ethernet cable, while in bench-top operation. The Ethernet plug is located in the interior of the board, thus it is not accessible when the GLIB is installed in a crate. Interfacing to a PC while the GLIB is used on a bench could be also achieved with a PCIe adapter card attached to the AMC edge connector.

For temporary data storage, two 72Mb SRAM devices are available on-board.[2] The GLIB has the possibility of using higher capacity (up to ∼1Gb) SRAM devices once they become available. It is important to note that the two SRAMs have independent address/data buses.

For the powering of the AMC, high efficiency switching regulator modules with improved thermal performance are used, requiring minimal cooling. Concerning the cooling of the FPGA,

[2]On-board SRAM devices have been used instead of Single In-line Memory Modules (SIMM) due to the lack of space in the printed circuit board.

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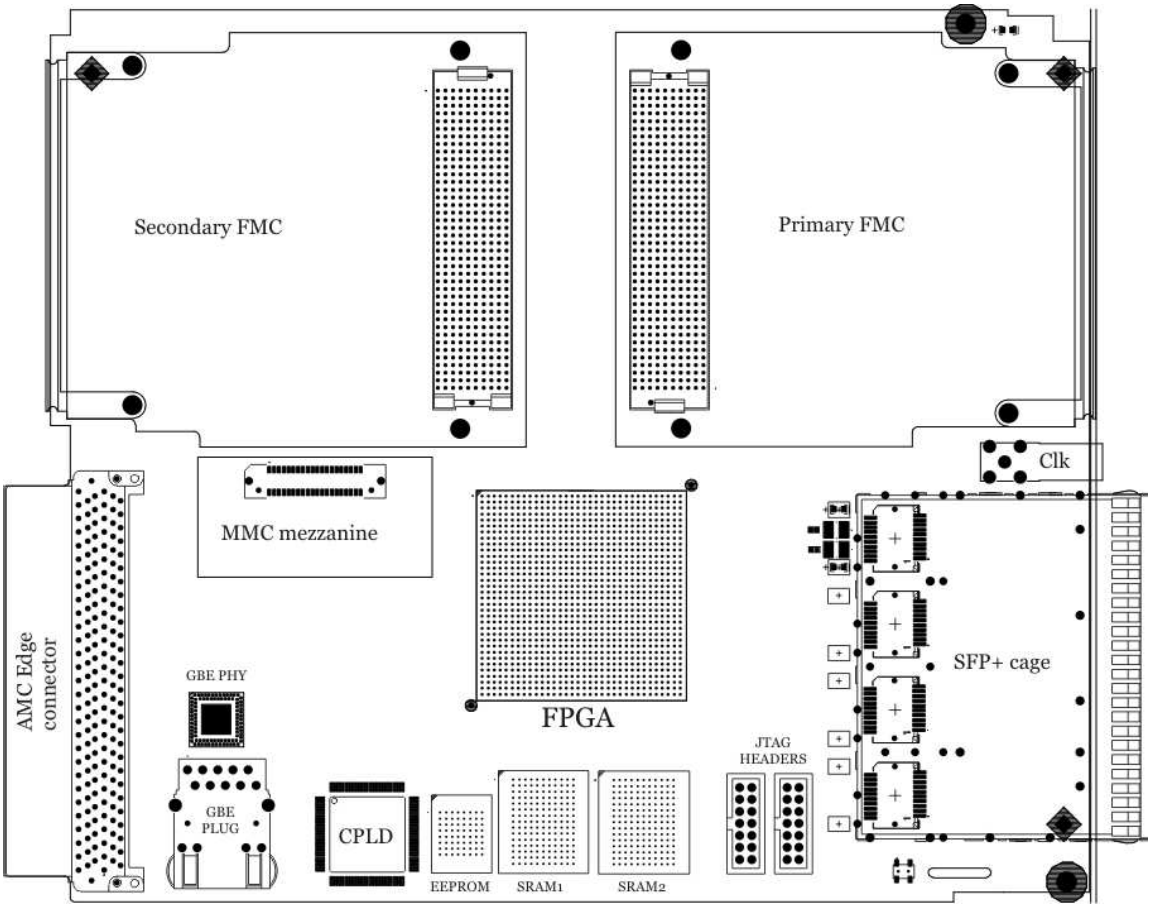

Figure 4. Preliminary placement (component side).

the use of a low-profile heat sink is sufficient for in-crate operation. For bench-top operation, the use of a heat sink equipped with a cooling fan is foreseen.

Figure 4 shows the component placement (top-side view). The AMC edge connector is located on the left side of the card while the front panel is on the right. The orientation of the FMC sockets is such that the primary FMC is accessible by the front panel and the secondary from the rear. Additionally, the front panel provides access to the four sockets for SFP+ modules as well as to an external clock connector. The switching regulator modules, as well as other active components (e.g. the clock distribution circuitry) are not shown in figure 4 since they are placed on the bottom side of the board.

3 Typical use cases

The flexibility of the GLIB with its variety of optical and electrical interfaces enables it to be used in various configurations. Three possible setups are discussed below. Figure 5 shows a bench-top beam test setup. In this setup, the GLIB communicates with the front-end via GBT links. The TTC information is received by the GLIB through an FPGA Mezzanine Card (TTC FMC, shown as a small yellow rectangular block). The configuration of the GLIB as well as the transfer of

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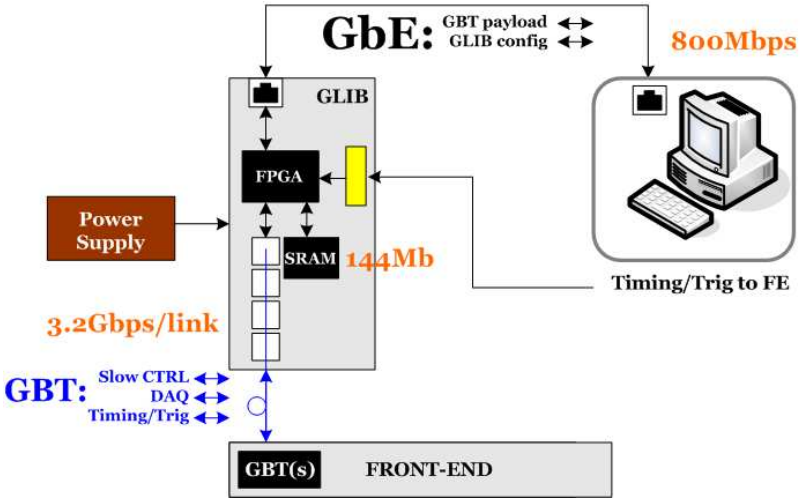

Figure 5. Bench-top beam test setup.

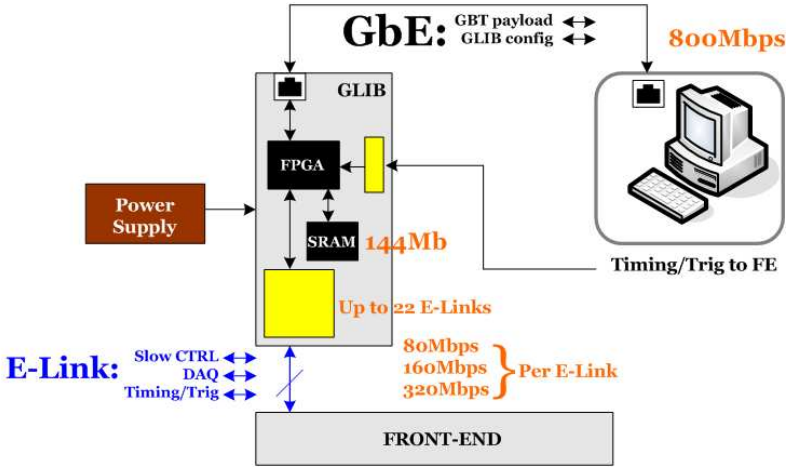

Figure 6. Bench-top front-end module test setup.

the GBT payload from/to the PC is done through a GbE connection. The SRAM can be used for intermediate storage, if necessary.

Figure 6 shows a bench-top setup for testing front-end modules not equipped with GBT. For the direct communication with the front-end chips, the GLIB is equipped with an e-link FMC emulating a GBT-e-port functionality (shown as a large yellow square block). The GLIB is also equipped with a TTC FMC. The configuration of the GLIB as well as the transfer of the GBT payload from/to the PC is done through a GbE connection. The SRAM can be used for intermediate storage, if needed.

For the powering of both bench-top setups highlighted in figures 5 and 6, an external power supply is used. Figure 7 shows a system test setup in a μTCA crate. The crate is managed by a MicroTCA Carrier Hub (MCH) controlled through a GbE link. The GLIB is equipped with a TTC FMC. The GLIB communicates with the front-end via GBT links. The configuration of the GLIB as well as the transfer of the GBT payload from/to an AMC CPU is done through the MCH

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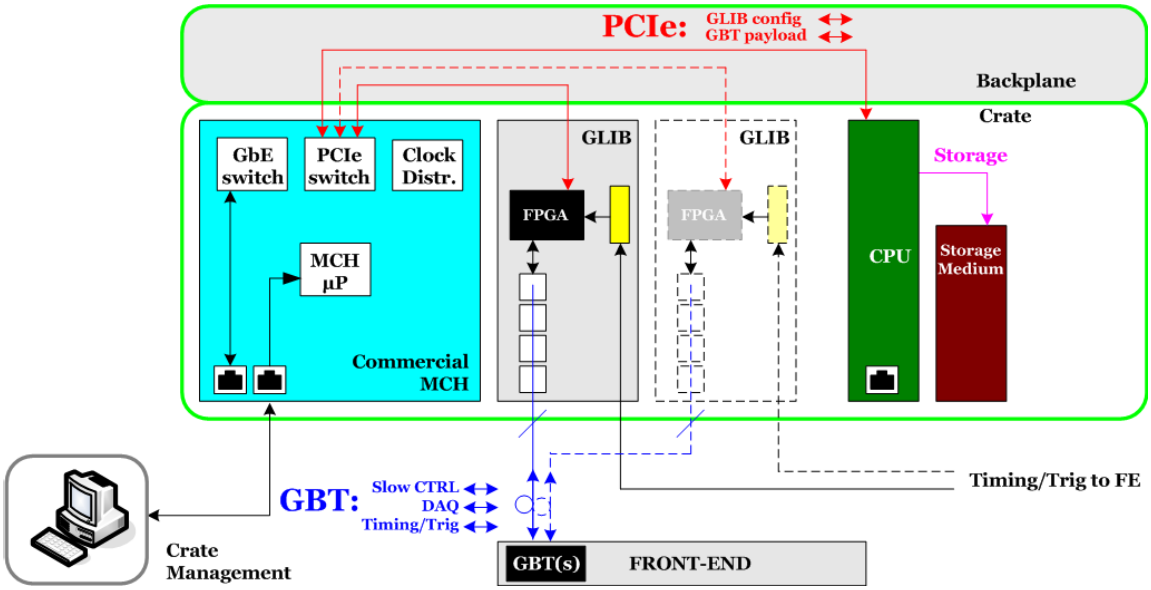

Figure 7. μTCA crate system test setup.

PCIe switch. The AMC CPU can store the data to an AMC storage medium through a Serial Advanced Technology Attachment (SATA) link.

4 Summary and status

This paper has introduced the GLIB, an evaluation platform currently under development for users of high speed optical links in high energy physics experiments. Its architecture and main features as well as some of the various possible configurations have been presented. The PCB layout of the board is on-going and is expected to be completed by the end of 2010. A first prototype of the board is expected in early 2011. We envisage that the GLIB board will be easily adapted to various other applications thanks to its variety of interfaces. More details and up-to-date information about the GLIB project can be found in the GLIB project web page [8].

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