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Low-cost bump bonding activities at CERN

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ABSTRACT: Conventional bumping processes used in the fabrication of hybrid pixel detectors for High Energy Physics (HEP) experiments use electroplating for Under Bump Metallization (UBM) and solder bump deposition. This process is laborious, involves time consuming photolithography and can only be performed using whole wafers. Electroplating has been found to be expensive when used for the low volumes which are typical of HEP experiments. In the low-cost bump bonding development work, electroless deposition technology of UBM is studied as an alternative to the electroplating process in the bump size / pitch window beginning from 20 μm / 50 μm. Electroless UBM deposition used in combination with solder transfer techniques has the potential to significantly lower the cost of wafer bumping without requiring increased wafer volumes.

A test vehicle design of sensor and readout chip, having daisy chains and Kelvin bump structures, was created to characterize the flip chip process with electroless UBM. Two batches of test vehicle wafers were manufactured with different bump pad metallization. Batch #1 had AlSi(1%) metallization, which is similar to the one used on sensor wafers, and Batch #2 had AlSi(2%)Cu(1%) metallization, which is very similar to the one used on readout wafers. Electroless UBMs were deposited on both wafer batches. In addition, electroplated Ni UBM and SnPb solder bumps were grown on the test sensor wafers. Test assemblies were made by flip chip bonding the solder-bumped test sensors against the test readout chips with electroless UBMs. Electrical yields and individual joint resistances were measured from assemblies, and the results were compared to a well known reference technique based on electroplated solder bumps structures on both chips. The electroless UBMs deposited on AlSi(2%)Cu(1%) metallization showed excellent electrical yields and small tolerances in individual joint resistance. The results from the UBMs deposited on AlSi(1%) metallization were non-uniform and closer inspection revealed micro cracks at aluminum — electroless nickel interface. UBM deposition was also done for Timepix wafers and solder ball placement process was prototyped with 40 μm balls.

KEYWORDS: Hybrid detectors; Manufacturing

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1 Introduction

Bump bonding of pixel detectors has been shown to be the major cost-driver for some of the LHC vertex detectors [1, 2]. The bump bonding procedure comprises of depositing bumps on sensor and readout wafers, dicing of wafers and Flip Chip (FC) bonding of individual dies. The conventional flip chip bump used in a hybrid pixel detector consists of an electroplated Under Bump Metallization (UBM) and a solder alloy bump. The electroplating process is laborious and has been found to be expensive for low wafer bumping volumes, which is the case for HEP experiments. Wafer bumping costs could be reduced by using Electroless Nickel (EN) deposition technology for UBMs in combination with advanced solder transfer techniques.

EN deposition technology enables various Flip Chip (FC) assembly scenarios, doesn't require lithography and is a high-volume capable batch processing technique. For these reasons the technology is cost-efficient and attractive. In the past, Electroless Nickel (EN) technology was quickly adopted by the electronics industry without careful characterization. This led to failures and reliability issues and to the poor reputation of electroless technology. However, during the last 10 years many of the technical challenges have been understood [3], and fully automated process equipment lines allowing precise online control of the plating chemistry have been developed. This has contributed to improved quality, reproducibility and reliability of EN depositions.

Solder ball placement systems have become commonly available during the last 5 years. Solder ball placement technology is cost-effective because of its simplicity and fully automatic operation. At the moment the finest solder balls available have 40 μm diameter. The solder balls have a very well controlled volume facilitating high yields in flip chip assembly. The novel solder ball placement technologies aim at having a 100% bumping yield by controlling the quality with

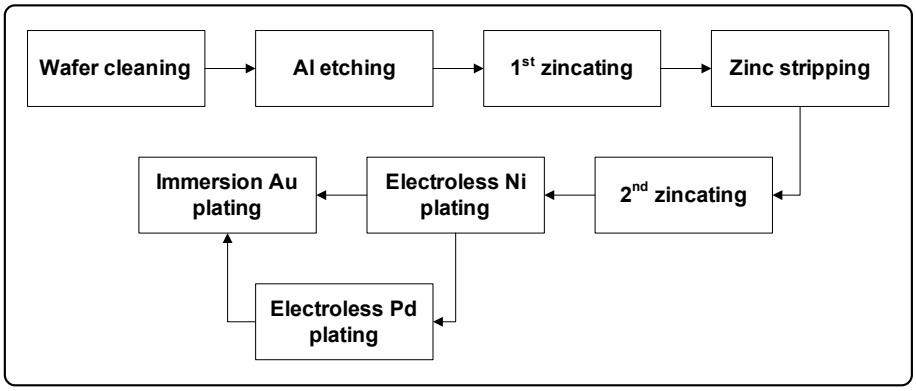

Figure 1. Process flow chart of ENIG/ENEPIG UBM deposition using double zincating process.

automated vision system before and after the solder transfer. If bumping defects are recorded, the solder bumps will be reworked. The optimization of the bumping throughput and quality requires both individual solder ball placement and wafer-level mass transfer techniques. Currently, mass transfer is done with 60 μm solder balls, but the technique is developing rapidly and is foreseen to move to 40 μm in near future. The 40 μm balls, which allow for a bumping pitch of $\sim$100 μm, could already be used in some HEP pixel detector systems, such as in outer tracking layers. However, since this requires covering of large areas, the issue related to the prevailing high FC assembly costs has also to be solved.

In this work EN deposition of UBMs is studied as an alternative for electroplating in fine pitch wafer bumping processes. The yields and electrical properties of EN UBMs are characterized on test vehicle structures. In addition, solder ball placement technology with 40 μm bumps has been demonstrated on Timepix chips with EN UBMs. Although the development of cost-effective FC assembly techniques are also essential for low-cost bump bonding, they are not included in this paper.

2 Electroless Nickel (EN) process description

The process flow of Electroless Nickel - Electroless Palladium — Immersion Gold (ENEPIG) and Electroless Nickel — Immersion Gold (ENIG) used in this work are illustrated in figure 1. The process begins with a series of activation steps which contribute to the surface pre-treatment of Aluminium (Al). The first step is a cleaning cycle, in which all organic contaminates and Si residues are removed from the wafers. After the cleaning step, the native oxide of aluminium is removed by an etching process to enable the growth of Zn in the subsequent zincating steps.

In the zincating process a thin layer of Zn is nucleated on Al pads. The zincating step is a prerequisite for the autocatalytic deposition of Ni on Al pads. The catalytic nucleation process of Zn is based on an exchange reaction between the exposed Al on the wafers and the zinc complexes in the zincating solution. In the double zincating process that is used here, the first Zn layer is stripped in nitric acid solution, which results a more uniform Zn layer with a finer grain structure in the second zincating step [4]. The fine-grained and uniform Zn layer has been found to result in a more uniform Ni growth in the subsequent process steps and also to increase the adhesion at Al-Ni interface [5].

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The deposition of Ni is started by dissolving Zn into the plating solution and replacing it with Ni. Once the surface of the Zn layer has been completely covered by Ni, the autocatalytic plating reaction of Ni begins. The growth of Ni is isotropic, and this has to be taken into account in the design of bump structures. The deposited Ni follows the surface of the passivation very closely, but does not adhere to it. The mechanical contact is created only to the Al pad and not to the passivation.

Immediately after the plating of Ni, either a thin layer of gold (Au), or palladium (Pd) followed by Au, is deposited onto the Ni to protect it from oxidation. The plating reaction in immersion Au process is a self-limiting exchange reaction and typically results a gold layer with a thickness of 50 nm - 100 nm. The optional Pd layer is complementary to immersion gold and it helps to maintain the solderability of the UBM after long or multiple heating cycles. The Pd layer also hinders the formation of the Inter Metallic Compounds (IMC) between tin and nickel.

3 Solder ball placement technologies

Individual solder ball placement systems have been developed from gold wire bonding systems using the precision placement capabilities of the equipment. These systems place preformed solder spheres on the bump pads one by one. Typically, the individual bump placement systems can achieve a rate of the order 10 bumps a second. This is economical for wafers with low number of I/Os ($<$ 200,000) or eventually for single chip area arrays. If a higher number of I/Os are used, the individual solder ball placement process ceases to be economical. The conventional systems make a contact to the wafer, while transferring the solder bump from the nozzle to solderable UBM. However, new contact-free methods have been emerging during the last years. Pac Tech's advanced solder placement tool SB2 has a nozzle with a high-power laser. Solder spheres are injected to the nozzle one by one and they are instantly melted by the laser in inert ambient and "spit" on the chips. This technique is well adapted for chips and wafers with solderable UBM like ENIG. This technology is especially interesting in single chip bumping of readout chips made in MPW runs. If EN is deposited on I/O pads, solder could be easily deposited on the chips.

The most powerful solder ball placement technique is the mass transfer method in which all the solder balls are moved on wafer with UBMs in one step. Pac Tech has introduced the so-called Gang Ball Placement (GBP) technology, which seems to be one of the most promising low-cost bumping solutions currently available. In GBP a stencil grid is used in combination with vacuum on the arm side to hold the wafer-level array of solder balls and to compress them against the UBM pads. The stencil is a replica of the I/O matrix of the wafer to be bumped. The solder balls are picked up from a platter using a vacuum which is applied behind the stencil plate. The balls fill all the holes and an ultrasonic vibration pulse is subjected to shake off the excess balls. An automated vision system scans through the stencil grid to analyze the bumping quality. If "pass" signal is given by the vision system, the solder balls will be transferred on the UBM pads over the whole wafer. If there are too many defects (missing bumps & solder ball clusters) in the stencil, all solder balls are dropped and reloaded. In addition, the individual solder ball placement machines can be used to rework single bump defects after the mass transfer. In electroplating processes the control of the bumping quality cannot be done at this level, and therefore solder transfer processes are expected to have better yields.

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4 Experimental procedures

4.1 Test vehicle description

A test vehicle was designed for characterization of the electrical properties and yields of the electroless UBMs. The vehicle consists of a test sensor chip and a test readout chip, each of which have 21 000 solder bumps. The bump matrix is divided to areas with a pitch of 110 μm and 55 μm, both having a bump pad size of 20 μm. When FC bonded together the test sensor and readout chips form a test vehicle with 32 daisy chain structures and two Kelvin bump test structures, KB-1 and KB-2. The daisy chains have lengths of 512 (26 chains), 768 (2 chains) and 2048 (3 chains) solder joints. The test structures are wired to a row of probe pads for electrical measurements. The daisy chain structures are used for gathering statistical information about the electrical yields of the solder joints after the flip chip process and the Kelvin structures are used to measure electrical properties of individual solder joints.

4.2 Test vehicle wafers

Two mask sets were created for processing test sensor and test readout wafers. Both wafer types contained 44 chips on 150 mm wafers. Two batches of test wafers were processed, both including sensor and readout wafers. Batch #1 had AlSi(1%) wiring layer metallization, which is similar to the one on the pixel sensor wafers used at CERN. Batch #2 had AlSi(2%)Cu(1%) wiring metallization, which is similar to the one used on pixel readout wafers. The 8" IBM CMOS wafers which are used at CERN have AlSi(1%)Cu(0.5%) as topmost metal. However, due to the unavailability of a sputtering target of that particular alloy, AlSi(2%)Cu(1%) metal was used instead. In total, 24 Batch #1 and 17 Batch #2 wafers were processed by the authors at VTT Micronova facility in Espoo, Finland.

Both wafer batches went through an electroless UBM deposition process at Pac Tech, Germany. 12 wafers from Batch #1 were run through an ENIG process and 13 wafers from Batch #2 were processed with ENEPIG. The target UBM thicknesses were 6 μm and 4 μm for the ENEPIG and ENIG processes, respectively. In addition to the EN UBMs deposited on wafers from Batch #1 and Batch #2, tin-lead solder bumps with nickel UBMs were electroplated on five wafers (without EN) from Batch #1with VTT's standard process. The used bumping technology has been well characterized and it is known to have good FC yields. Therefore it was chosen as a solder bump deposition technology and as a reference technology.

4.3 Assembly procedures

All the wafers were then diced and the chips were visually inspected prior to flip chip assembly. Only the chips with flawless bumping quality were chosen for FC assembly. Test assemblies were constructed by tack bonding test sensor chips with electroplated solder bumps against test readout chips with electroless UBM pads. Two sets of assemblies were made using test readout chips from Batch #1 (8 assemblies) and Batch #2 (16 assemblies). 8 reference assemblies were constructed similarly by tack bonding test sensor chips with electroplated solder bumps against test readout chips with electroplated thin solder bumps. SET FC150 flip chip bonder was used in all the assemblies. The tack bonding sequence was followed by a collective assembly reflow process in formic acid ambient at 230 °C.

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Table 1. Results from Daisy Chain (DS) with different solder structures.

		Short DS		Medium DS		Long DS		
FC process #	**Chips #**	**OK**	**All**	**OK**	**All**	**OK**	**All**	**Yield**
Reference	8	208	208	16	16	24	24	100.0%
1st batch	8	91	208	7	16	16	24	50.5%
2nd batch	16	413	416	31	32	48	48	99.3%

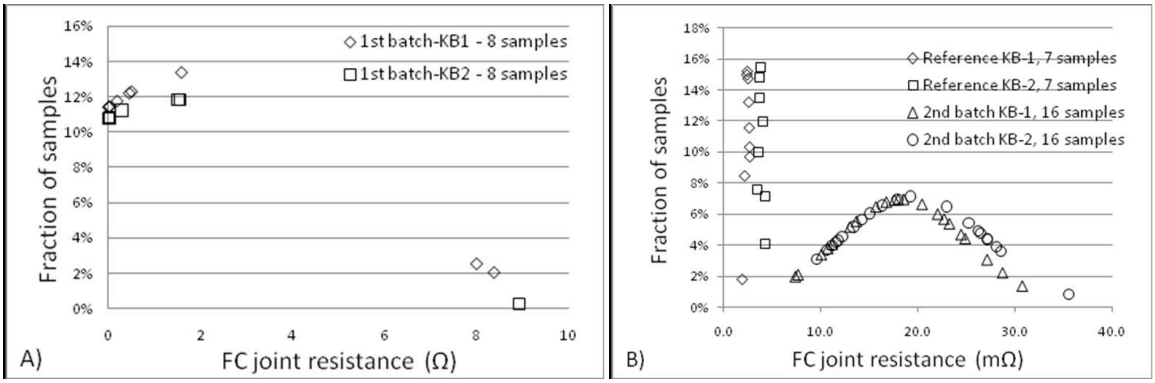

Figure 2. Distribution of single joint resistances for A) batch #1, B) batch #2 and reference assemblies.

5 Results and discussions

After the electroless deposition of UBM pads on the test wafers, the deposition yield and quality were visually estimated. Only very few visually observable defects were seen on the wafers and the yields were estimated to be better than 99.9% for both batches. The typical defects were EN growing from cracks in the passivation layer and missing UBM pads. As the EN process is maskless, the metal will grow from all the pinholes and cracks that reveal the underlying Al. Therefore, moving from electroplating to electroless deposition will require wafers with very good quality passivation. The passivation layer on the sensor wafers currently used in some CERN pixel detectors has been observed to contain pinholes and thus might not fulfil these requirements.

The daisy chains and Kelvin structures were measured from the test assemblies with a probe station and an Agilent 34970A data acquisition unit. If the average resistance of a single joint in a chain exceeded 1 Ω, the chain and all the joints in it, were classified as nonfunctional. This is a very stringent rating policy considering that the shortest daisy chains have 512 joints. The results of the daisy chain measurements are summarized in table 1 and the results of joint resistance measurements from Kelvin bump structures are plotted in figures 2A and B. It should be noted that the measured values of joint resistance, especially from the reference samples, are close or even below of the measurement equipment's capabilities and should therefore be considered as indicative values.

As expected, the reference technology using electroplated tin-lead solder bumps had a perfect yield and a very low solder joint resistance of few mΩ. The test assemblies from Batch #2 also

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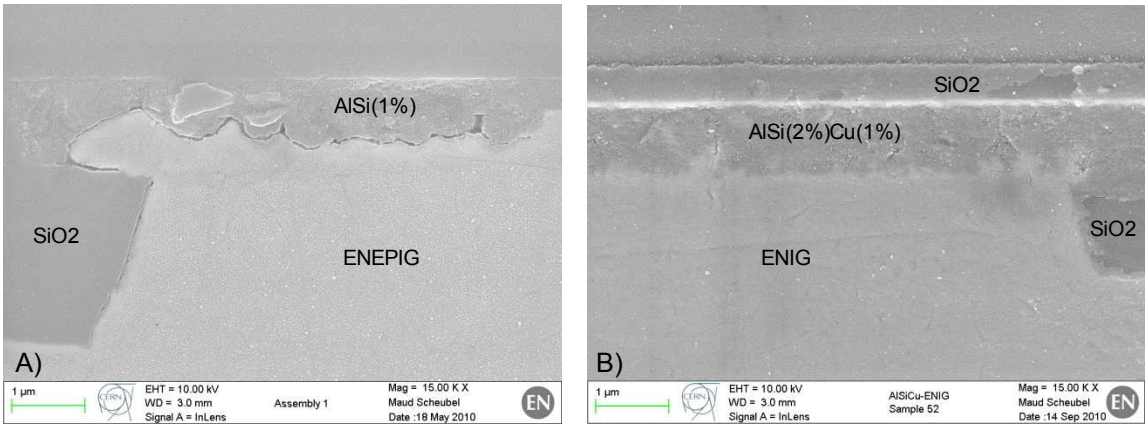

Figure 3. A) AlSi(1%)-ENEPIG interface, and B) AlSi(2%)Cu(1%)-ENIG interface.

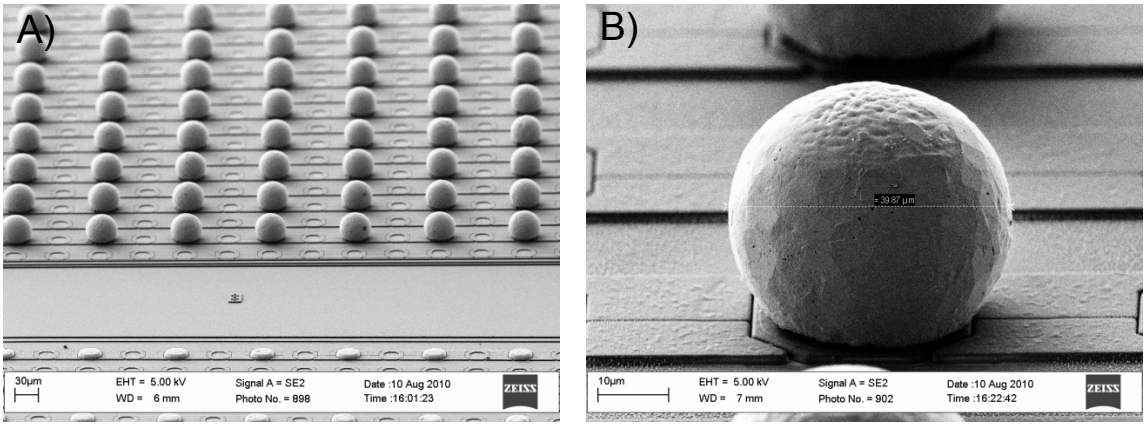

Figure 4. A) 40 μm solder bumps deposited at ENEPIG UBM pads with 110 μm pitch. B) Close-up of an individual solder bump.

showed good results, with yield of 99.3% and a mean joint resistance of $\sim$20 mΩ. However, the assemblies from Batch #1 measured poor yields and variation of many decades in the joint resistances, as can be seen from figure 2A.

To understand the reason behind the variation of solder joint resistances in the assemblies from Batch #1, cross-sectional samples were made of assemblies from both batches and studied with Scanning Electron Microscopy (SEM). Cracks shown in figure 3a were found frequently in between Al and Ni layers in assemblies from Batch #1. Besides the cracks, Al layer was strongly etched and the Al - Ni interface was rough. In the samples from batch #2 (figure 3b) the Al-Ni interface was significantly smoother, there was less etching of aluminum and most importantly there were no signs of cracking. The cracks at Al-Ni interface are a very logical explanation for the high joint resistance values measured from batch #1 assemblies.

It has been previously reported that small amounts of Cu in Al bond pad metallization improves the electroless plating quality [3]. This effect can also be clearly seen in the results here. By alloying 1 % of copper in the Al pad metallization in batch #2 wafers, the deposition quality of EN was significantly improved.

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Pac Tech's SB^2 solder ball jetting system was demonstrated on Timepix chips having ENEPIG UBM pads (figure 4). The UBMs were grown at 110 μm pitch using a protective photoresist layer to mask every second pixel row and column, and 40 μm solder balls were jetted on $\sim$ 16 k I/O pads. 80 missing bumps were counted on the first prototyping sample, which equals to 99.5% yield. With increasing number of samples, the process will become more optimized and the bumping yield is expected to improve respectively. Shear strength tests were done for 30 individual solder bumps at Pac Tech and the average shear strength of 8 g/bump was measured, which is good. The individual solder ball deposition tests will continue soon with bumping of single Timepix chips and they are followed by the flip chip bonding.

6 Conclusions

Deposition of EN UBM structures was done on two sets of test wafers with different bump pad metallization to characterize the process. Chips with electroplated solder bump structures were FC assembled against chips with the EN UBMs and the test structures in the assemblies were electrically characterized. The results indicate that the alloying of Cu in Al pad metallization significantly improves EN UBM deposition quality. The AlSi(2%)Cu(1%) metallization used in the Batch #2 test wafers is very similar to the topmost metal on the IBM CMOS wafers used at CERN. Therefore, the electroless UBM technology has potential to be used as a low-cost alternative for electroplated UBMs on readout wafers. Further development is needed to optimize the process also for AlSi(1%) metallization that is commonly used in sensor wafers. Furthermore, in order to fully realize the cost saving potential of the EN UBM deposition technology, low cost solder bumping processes, such as solder ball placement methods, need to be developed for the bump pitch window of 50–100 μm. Individual solder ball placement tests were successfully demonstrated on a single Timepix chip using 40 μm balls and 110 μm pitch.

References

[1] D. Muenstermann, *ATLAS upgrade week*, 25 Feb. (2009), http://indico.cern.ch/getFile.py/access?contribId=1&resId=0&materialId=slides&confId=52298.

[2] A. Kluge, *Design, production and first operation of the ALICE Silicon Pixel Detector system*, TWEPP-2008 conference, http://indico.cern.ch/contributionDisplay.py?contribId=131&confId=21985.

[3] A. Strandjord et al., *Electroless nickel-gold reliability, UBM, flip chip and WLCSP*, IMAPS symposium, 8–12 Oct. (2006).

[4] Y. Yang, J. Cai, S. Wang and S. Jia, *The impact of zincation on the electroless nickel UBM for low cost flip chip technology*, in *6th International Conference on Electronic Packaging Technology*, 30 Aug.–2 Sept. 2005, pp. 229-233.

[5] G. Qi, X. Chen and Z. Shao, *Influence of bath chemistry on zincate morphology on aluminum bond pad*, *Thin Solid Films* **406** (2002) 204.

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