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MULTIPLE TIME DIGITIZERS AND TRIGGER SYSTEM FOR DRIFT CHAMBERS

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ABSTRACT

The architecture of a read-out system is described which will be used in conjunction with the muon detector in the UA-1 experiment at the $\bar{p}p$ collider at CERN. In addition to measuring drift time for spatial information, the system provides a fast trigger (< 1 μsec after drift time) and a second level trigger decision based on a fast microprocessor. The fast trigger part allows the use of the muon detector as an active trigger element, while a second level trigger decision using the detailed digitizer data is included for adequate reduction of the trigger rate. The Multiple Time Digitizer (MTD) is based on the use of fast RAMs (256 x 4) as 125 MHz shift registers, giving time bins of 8 nsec and a time range of 2 μsec (256 x 8 nsec). The high input rate has imposed a fast read-out and transfer to a buffer in the controller. The data in this buffer is reordered according to wire number and corresponding times. Together with look-up tables this allows fast processing of the data for a second level trigger.

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1. INTRODUCTION

Electronic systems for particle detectors are intimately related to the specific requirement on the detector and therefore determine very often the properties of such a detector. A presentation is made of the architecture of a read-out and trigger system which will be used in conjunction with the muon detector of the UA1-experiment at the $\bar{p}p$-collider[1] to cover a sensitive area of $\simeq$ 500 m^2. Large drift chambers (4 m x 6 m), described elsewhere in these proceedings[2], are constructed with 4 planes of drift tubes, which are glued together. The tube cross-section of 45 mm x 150 mm leads to a maximum drift length of 70 mm, corresponding to a drift time of 1.4 μsec. An average spatial resolution of 0.3 mm has been achieved everywhere in the tube. Even with only one wire every 150 mm and a typical tube length of 4-6 m, the total system contains about 5200 sense wires.

A track from a muon candidate, leaving the 1 m thick iron of the magnet yoke, is measured in two orthogonal projections, with 4 planes per projection. The tube arrangement is shown in Fig. 1. Two adjacent planes of staggered drift tubes help to solve the left-right-ambiguity, inherent to drift chambers, whereas the long lever arm between the plane doublets allows a good determination of the particle direction.

At the $\bar{p}p$-collider 5×10^4 interactions/sec are expected at a luminosity of 10^{30} cm^{-2} sec^{-1}. However, the total data recording rate is limited to typically 30 events/sec. Hence the trigger logic for the selection of rare events, which contain a high momentum muon, has to reduce the input rate by at least a factor 10^4, without introducing too much deadtime. It is a property of the electronic system that a passive drift chamber can be turned into an active trigger device. Unfortunately the use of drift chambers in a trigger scheme has disadvantages in two respects: firstly, the complete information is only available after the max. drift time, and secondly, read-out systems in general need in the order of a few hundred microseconds before detailed space information is available to be used for the trigger. A two stage trigger scheme is therefore proposed. The first level decision, available about 1 μsec after the max. drift time, is based only on the hit pattern of the wires. It does not

introduce any dead time, since the beams are bunched with a time structure of 4 μsec. A further event reduction is achieved by the second level trigger, provided by fast microprocessors, which are fed with drift time information. To keep the dead time of the second level trigger short, a fast data transfer from the digitizers to the microprocessors is as important as a fast processing time.

2. SYSTEM CONFIGURATION

The scheme of the read-out and trigger system is shown in Fig. 2. Up to 16 Multiple Time Digitizers (MTD) with 32 inputs are placed in a CAMAC crate (but with special power supplies and ECL signals at the dataway) together with a clock fan-out, a crate controller and two microprocessors Motorola 68000. The clock oscillator, the clock controller and the stop interpolator (LSB = 1 nsec) are in common to all MTD crates. The fast trigger logic spies on the signals from the drift chambers on their way to the MTD digitizers and records the wire hit pattern, disregarding the individual drift times. The hit pattern is connected to the 10 address lines of 1 K memories, as shown in Fig. 1. The memories are programmed in such a way that only tracks pointing within a cone of ±150 mrad to the $\bar{p}p$ interaction vertex are accepted. The use of programmable memories for track finding allows a certain flexibility, even in the fast trigger. The output of each memory indicates whether a valid track is recognized within the considered cone. The first level trigger decision is obtained by combining the tracks in the X-planes with those in the Y-planes together with additional spatial information from the hadron calorimeter. This reduces the input event rate by about a factor 10^2. For further reduction, performed by a more precise tracking to the vertex, the individual drift times from the MTDs are needed. The total data transfer time to the crate controller is about 5 μsec (needed for the scan of the MTD memory) plus 200 nsec per data word. These data are processed by two microprocessors per crate. In order to reduce their processing time, the data are ordered according to wire numbers and corresponding drift times by a "reordering memory". In addition, two tables with pointers, as indicated in Fig. 3, are also created during the

transfer of the reordered data to the microprocessor memories. The total transfer of the data from the MTDs to the microprocessor memories will only take about 30 μsec. The reordering memory can also be used as a data buffer, in which case the dead time, produced by the second level trigger, is considerably reduced. The information about the cone in which a track candidate was found by the first level trigger, together with additional information from the experiment, will reduce the time for track finding and reconstruction. The estimated processing time of about 70 μsec for the M68000 microprocessors introduces a dead time, due to the second level decision, which will not exceed 10% for the event rates at the $\bar{p}p$-collider.

3. PRINCIPLE OF THE M.T.D.

A simplified functional diagram of the M.T.D. is given in Fig. 4. The time measuring principle is based on the use[3] of shift registers (in this case 256 bits) as multiple time digitizers (Fig. 5). In this application a shift register has the following advantages:

- It is a multi-step synchronizer;
- No overflow circuitry is needed since after 256 clock pulses the data is finally shifted out.
- The recording is continuous.
- A very high number of hits (wire signals used as starts) can be handled, basically only limited by the duration of the wire signals and the length (bits) of the register.

Shift registers capable of operating at 125 MHz only exist with a few bits per integrated circuit. However, with the fast RAMs available nowadays, it is possible to construct long shift registers[4] which will operate at this frequency. In this case the address counter is continuously clocked (as the transport clock in a real shift register), and the length of the register equals the number of memory locations in a column. The memory used in this scheme is the MB 7071E of Fujitsu. It is a RAM with typically 12 nsec access time and it is organized as 256 words of 4 bits. Used in the normal way, with a binary address counter and write pulses, it will not operate at 125 MHz rate. However a detailed description of

the Fujitsu address decoder[5] intimated an alternate "write mode". If the write line is kept at write level the data becomes latched in the current address location at the moment when this location becomes deselected. As address counter we adopted a gray counter[6-9] which has the advantage that for each increment only one bit will change at a time, and consequently a change of address takes place without unwanted addressing during the transition (Fig. 6).

Clock frequencies in excess of 125 MHz are possible in this way. For a time digitizer it is important that there is not much spread in the time bins (= 8 nsec in this case). In the present case some spread will occur because every location of the memory has a small difference in set-up and hold-time, which is even dependent on the previous state of the selected location. To suppress this dependence a separate "write synchronizer" in front of the memory is incorporated. The read-out is done by scanning through the memory, with the output of the read synchronizer connected to the edge sensitive clock input of a D flip-flop. The read synchronizer does not only take away the spikes of the memory output while scanning, but it also allows a higher scan speed, since it divides the propagation delay of the scan loop into two parts. The two synchronizers are constructed with 4-bit shift registers with parallel load facility. The parallel load mode is used for the synchronization function. The shift register mode is used to enter test patterns without additional electronics (Fig. 7).

The event trigger is the time reference for the drift time measurement and it often arrives later than the earliest signals from the drift chambers. The digitizer records continuously until the arrival of the event trigger which stops the write clock and hence the measuring process an adjustable time later (called "stop" hereafter) in order to allow for maximum drift time. This location corresponds to time zero. The previous location will be 8 nsec and the next one 2040 nsec before the stop. The binary time counter (Fig. 4) is preset to 2040 nsec and is then counted down during the read scan. During the read scan the hit detection is sensitive to the leading edge of the recorded signal and stops the scan clock. At this moment the data of the binary counter corresponds to the measured drift time.

The clock controller controls both the WRITE and the READ clock. In this way the max. drift time can be adjusted in common for all MTDs in the experiment (Fig. 2).

4. REORDERING MEMORY

The reordering memory is constructed with two memories, which are differently addressed for writing and reading (Fig. 8). Instead of reserving a fixed memory space per wire, a system with pointers is used, which are created during the write phase and used to indicate the reading order during the read phase. For the write sequence, memory 1 (last time pointer) is addressed with the wire number and has the current address of memory 2 (time + previous time pointer) as data. Memory 2 is addressed by the write counter and has the time and the previous time pointer from memory 1 as data. For the read sequence the data has to be read in wire order and corresponding times. The read counter is used to scan memory 1 in wire order. If a "previous time pointer" not equal to zero has been found, memory 2 becomes addressed with this pointer, so producing the time data and the next pointer indicating where to find the next corresponding time. If this next pointer is zero there are no more corresponding times, so the scan with the read counter continues. In this way the amount of hits on the same wire can be variable, but the total amount of hits is limited to 255 out of a group of 256 wires.

5. SUMMARY

A time digitizer and trigger system has been developed which is well adapted to large drift tube chambers. A high multiple hit capability over the maximum drift interval adjustable up to 2 µsec has been achieved using fast memories as shift registers. The 8 nsec LSB of the digitizer does not significantly spoil the spatial resolution of chambers with large drift spaces, especially since the common time reference is measured with an accuracy of 1 nsec. If required, a LSB of 4 nsec can be reached when 2 channels are used in parallel with a time delay of 4 nsec. With 32 channels per single CAMAC module and 512 channels per crate, the packing density of the system is very high. A read-out time of about 30 µsec

per event is achieved. The data are ordered according to wire number and corresponding times. Together with data pointers this reduces the processing time of the microprocessors located in the same crate.

REFERENCES

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FIGURE CAPTIONS

Fig. 1 First level trigger decision. The long lever arm between the plane doublets allows a good determination of the particle direction. 1 K x 1 bit memories are used as programmable combinatorial logic, supplied with the HIT-pattern only.

Fig. 2 Information from 16 Multiple Time Digitizers with 32 inputs and from first level trigger logic is fed to second level trigger logic, composed of two microprocessors.

Fig. 3 Data tables for one microprocessor. The processing time is reduced by the use of pointers to the reordered data.

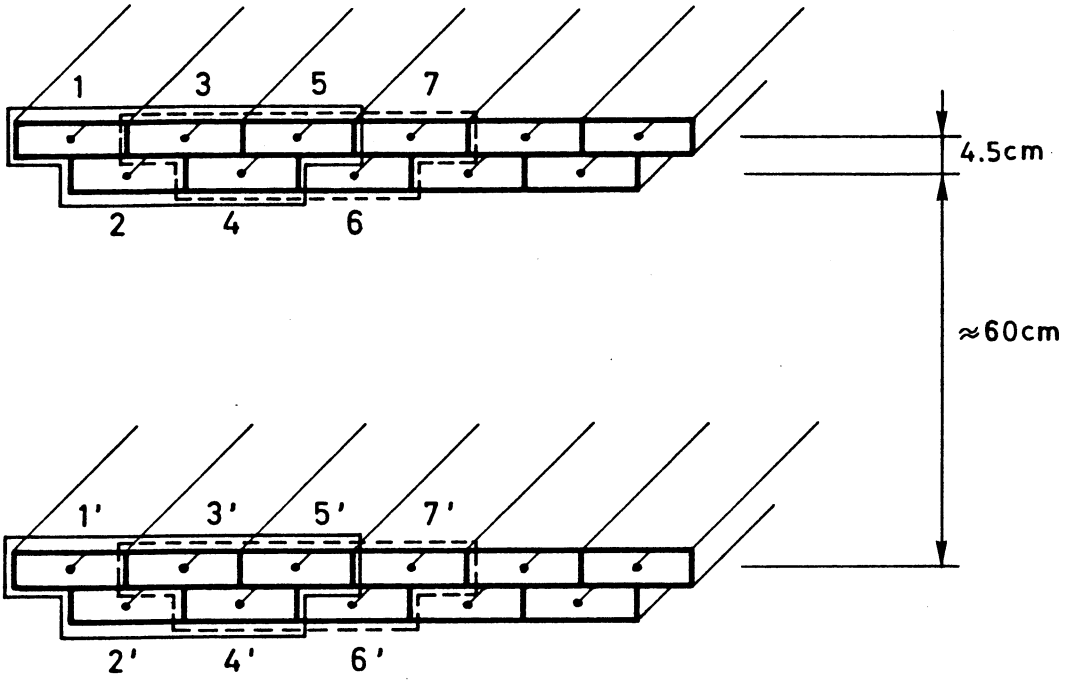
Fig. 4 Multiple Time Digitizer principle. The simplified diagram indicates the signal-path of one input only. Although the writing is continuous, only the time information corresponding to the leading edge of the stored wire signals is read out.

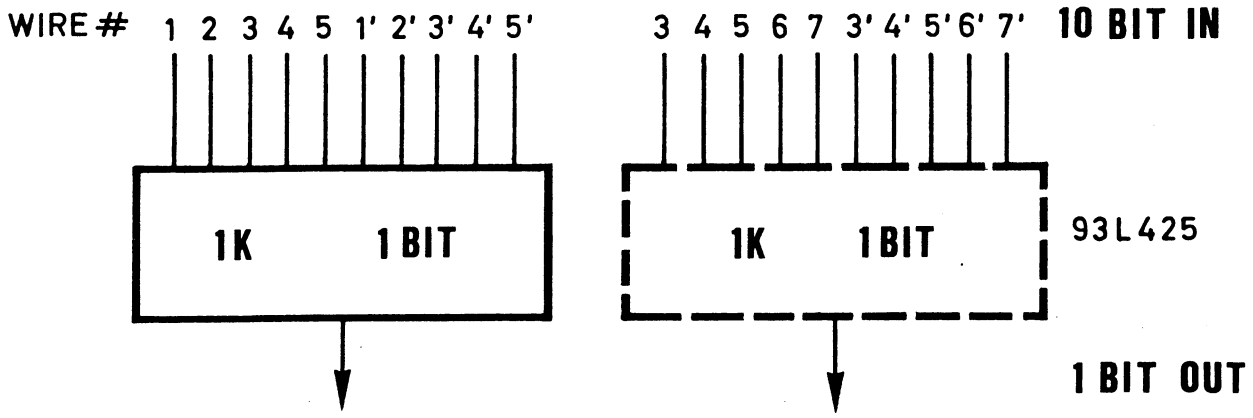
Fig. 5 Time measurement with shift register.

Fig. 6 Synchronous Gray counter. Exclusive ORs are used to convert the binary code to Gray Code. The I.C. 100.141 is used as 8 D flip-flops with a common clock.

Fig. 7 M.T.D. test mode. The I.C.'s F10.000 used as WRITE and READ synchronizer in the MTD are shift registers. In shift mode they simulate test signals. Different wiring before and after the memories makes fault diagnosis easier.

Fig. 8 Reordering memory. This is housed in the crate controller and serves both to buffer and to reorder the data from the MTDs.





PATTERN PROGRAMMABLE

$3 \in 4, \quad 4 \in 4$

LEFT - RIGHT AMBIGUITY SOLVED

Fig. 1

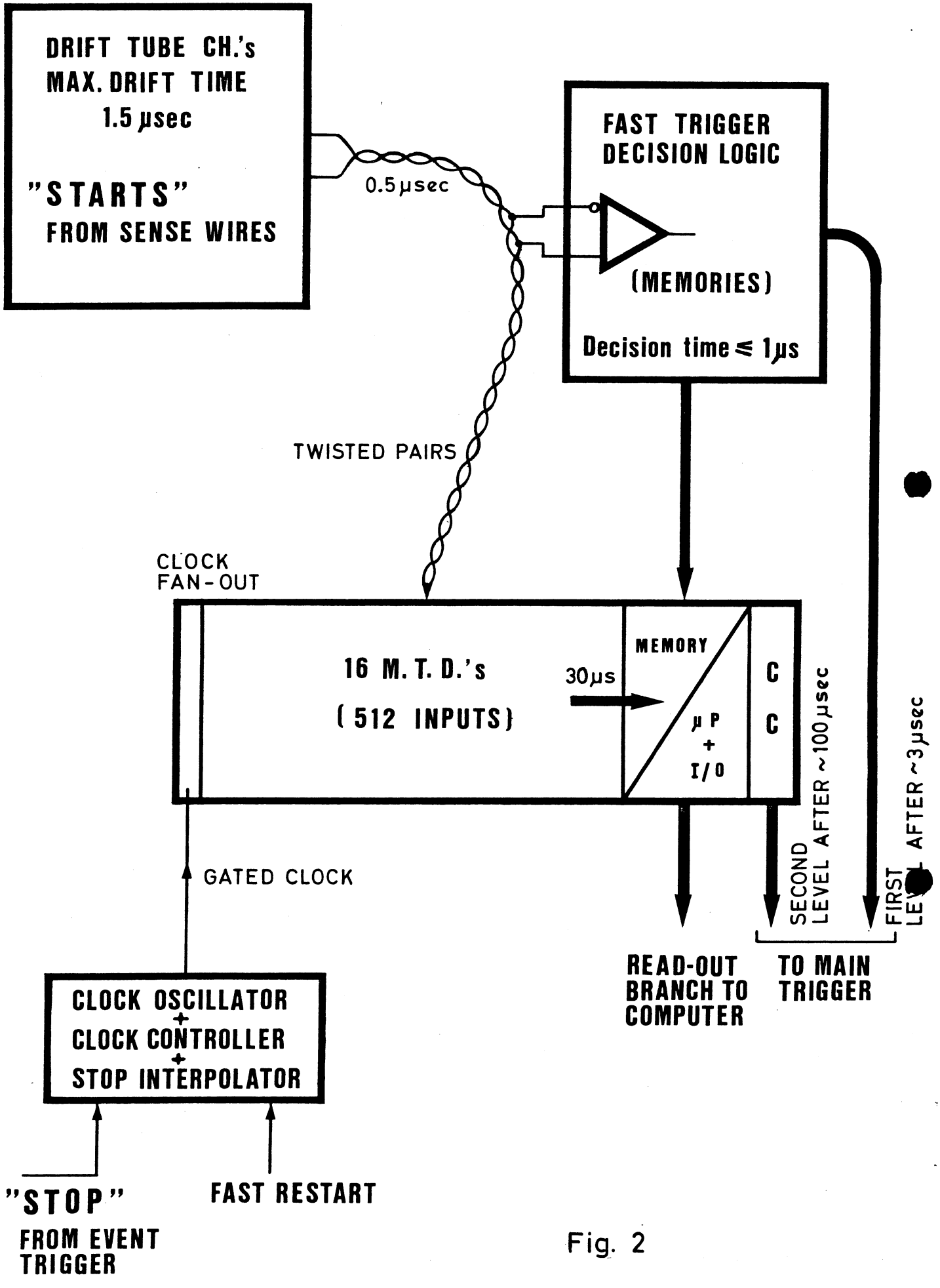

DRIFT TUBE CH.'s
MAX. DRIFT TIME
1.5 μsec
"STARTS"
FROM SENSE WIRES
0.5 μsec
FAST TRIGGER
DECISION LOGIC
(MEMORIES)
Decision time ≤ 1μs
TWISTED PAIRS
CLOCK
FAN-OUT
16 M. T. D.'s
(512 INPUTS)
30μs
MEMORY
μP
+
I/O
C
C
SECOND
LEVEL AFTER ~100 μsec
FIRST
LEVEL AFTER ~3 μsec
GATED CLOCK
READ-OUT
BRANCH TO
COMPUTER
TO MAIN
TRIGGER
CLOCK OSCILLATOR
+
CLOCK CONTROLLER
+
STOP INTERPOLATOR
"STOP"
FROM EVENT
TRIGGER
FAST RESTART

Fig. 2

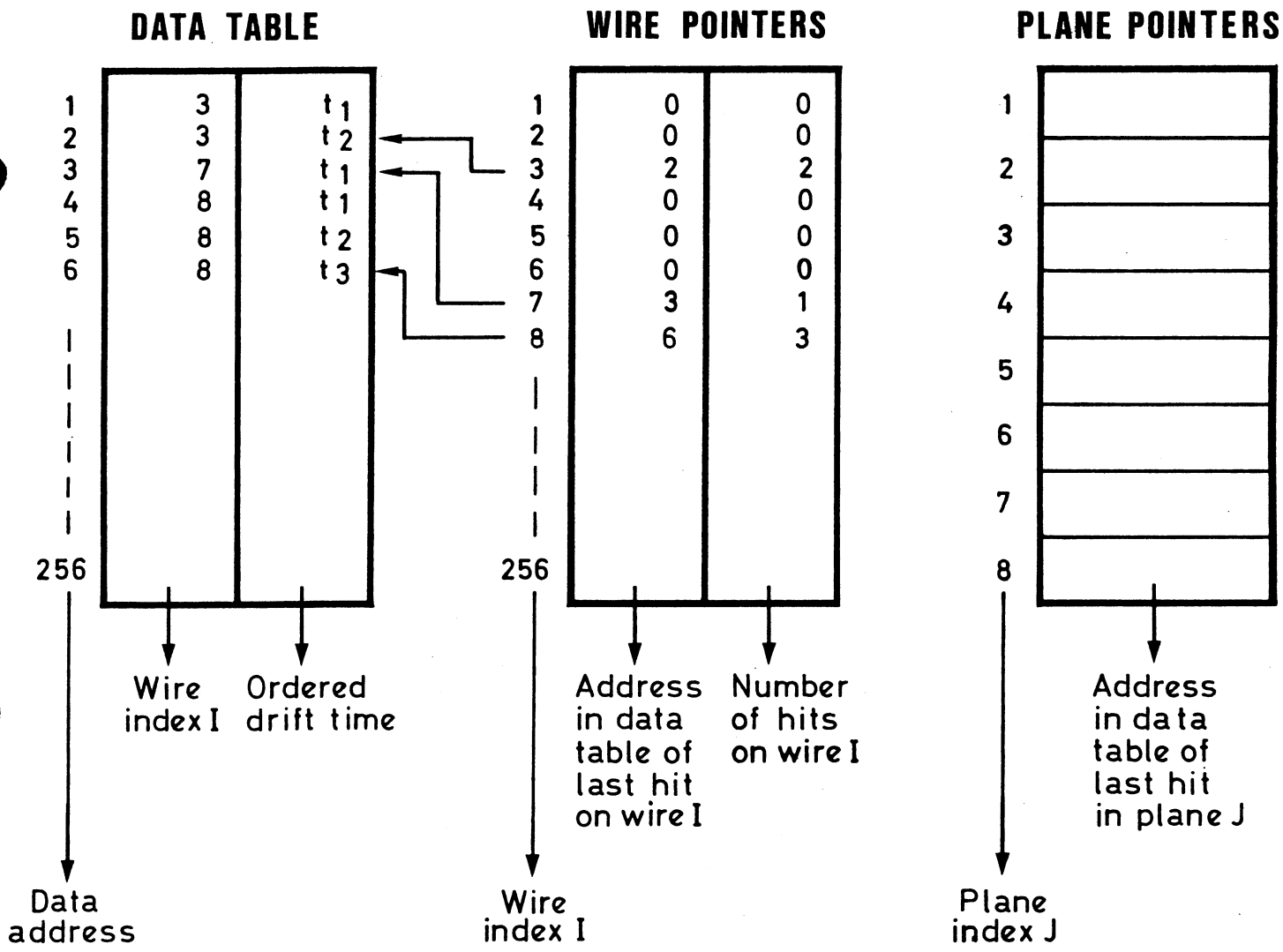

DATA TABLE
WIRE POINTERS
PLANE POINTERS
1
2
3
4
5
6
256
3
3
7
8
8
8
t1
t2
t1
t1
t2
t3
Wire index I
Ordered drift time
Data address
1
2
3
4
5
6
7
8
256
0
0
2
0
0
0
3
6
0
0
2
0
0
0
1
3
Address in data table of last hit on wire I
Number of hits on wire I
Wire index I
1
2
3
4
5
6
7
8
Address in data table of last hit in plane J
Plane index J

Fig. 3

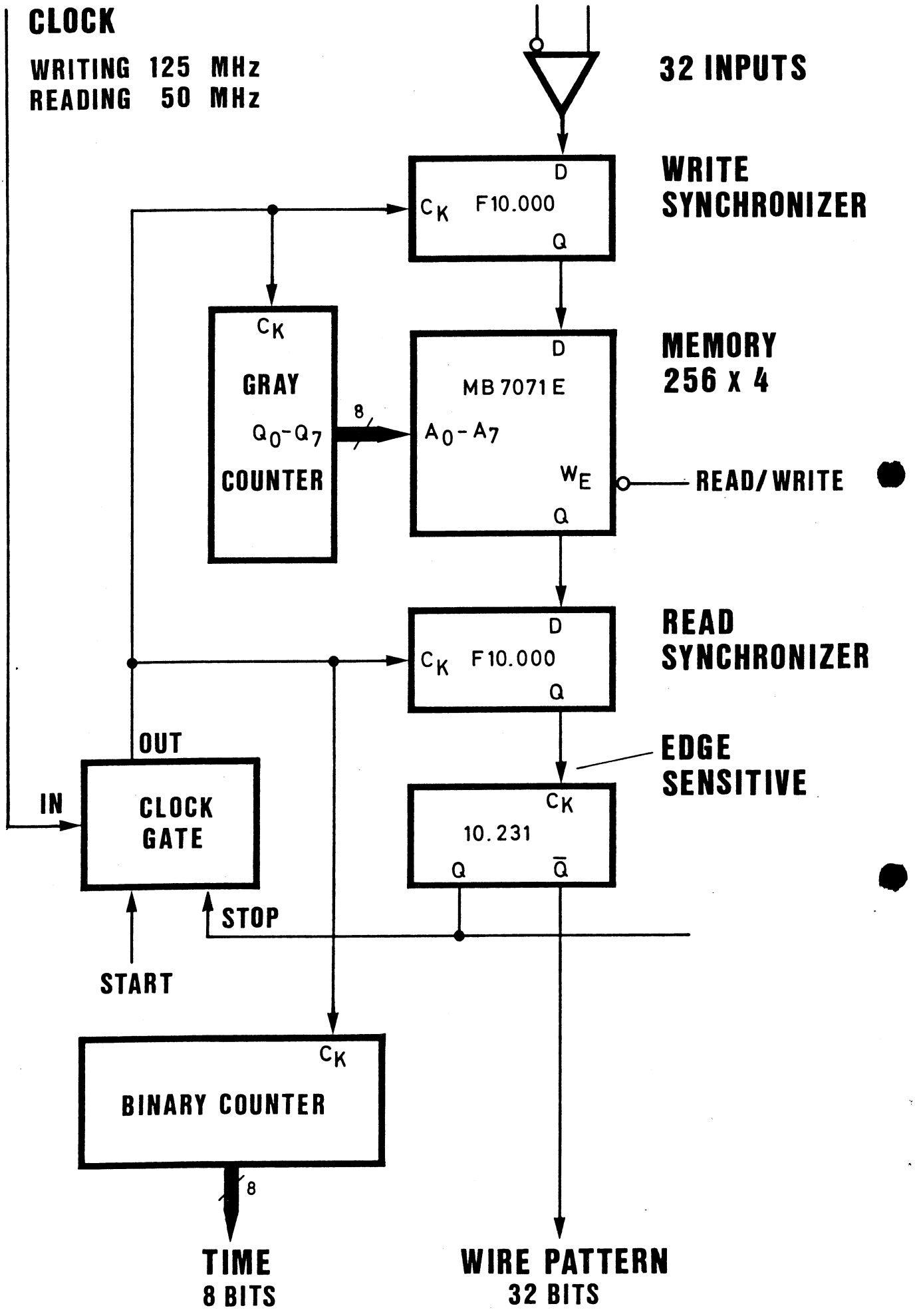

CLOCK
WRITING 125 MHz
READING 50 MHz
32 INPUTS
D
CK F10.000
Q
WRITE SYNCHRONIZER
CK
GRAY
Q0-Q7
COUNTER
8
D
MB 7071 E
A0-A7
WE
Q
MEMORY 256 X 4
READ/WRITE
D
CK F10.000
Q
READ SYNCHRONIZER
OUT
IN
CLOCK GATE
EDGE SENSITIVE
CK
10.231
Q
Q̄
STOP
START
CK
BINARY COUNTER
8
TIME
8 BITS
WIRE PATTERN
32 BITS

Fig. 4

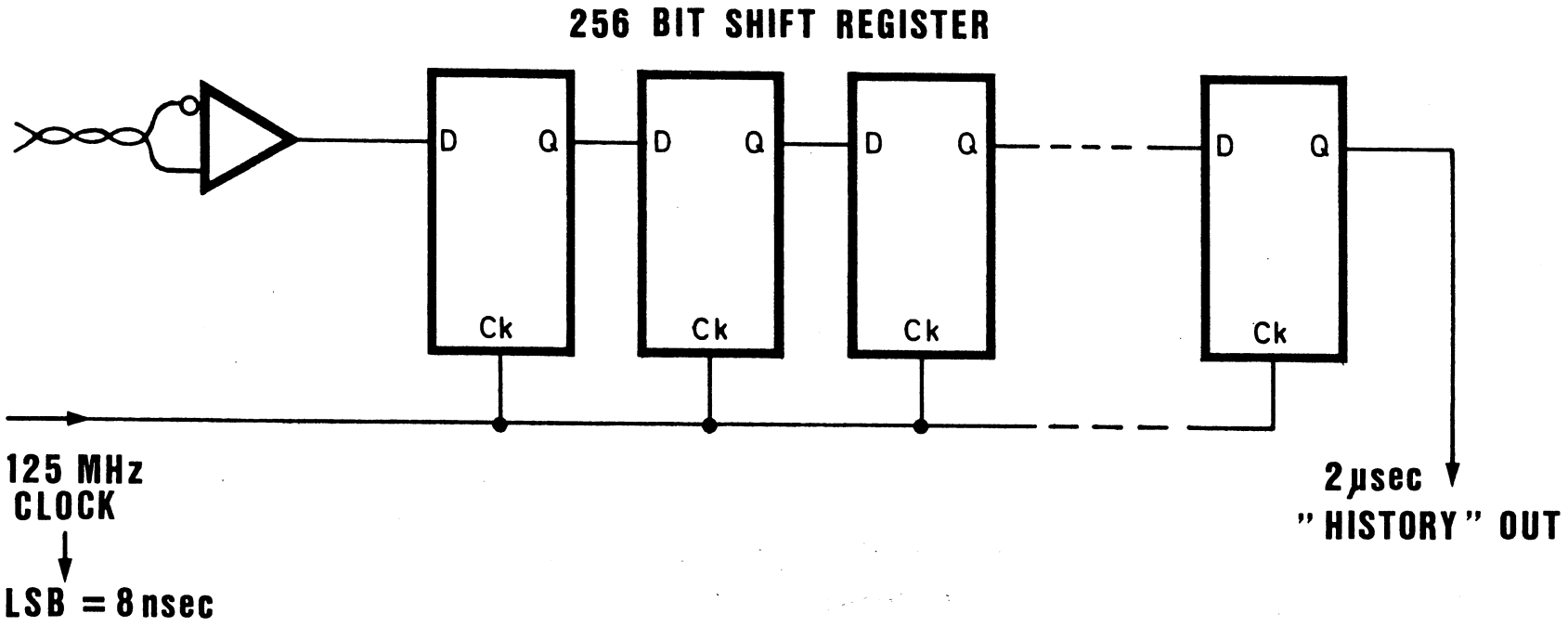

256 BIT SHIFT REGISTER
D
Q
Ck
D
Q
Ck
D
Q
Ck
D
Q
Ck
125 MHz
CLOCK
LSB = 8 nsec
2 µsec
" HISTORY " OUT

Fig. 5

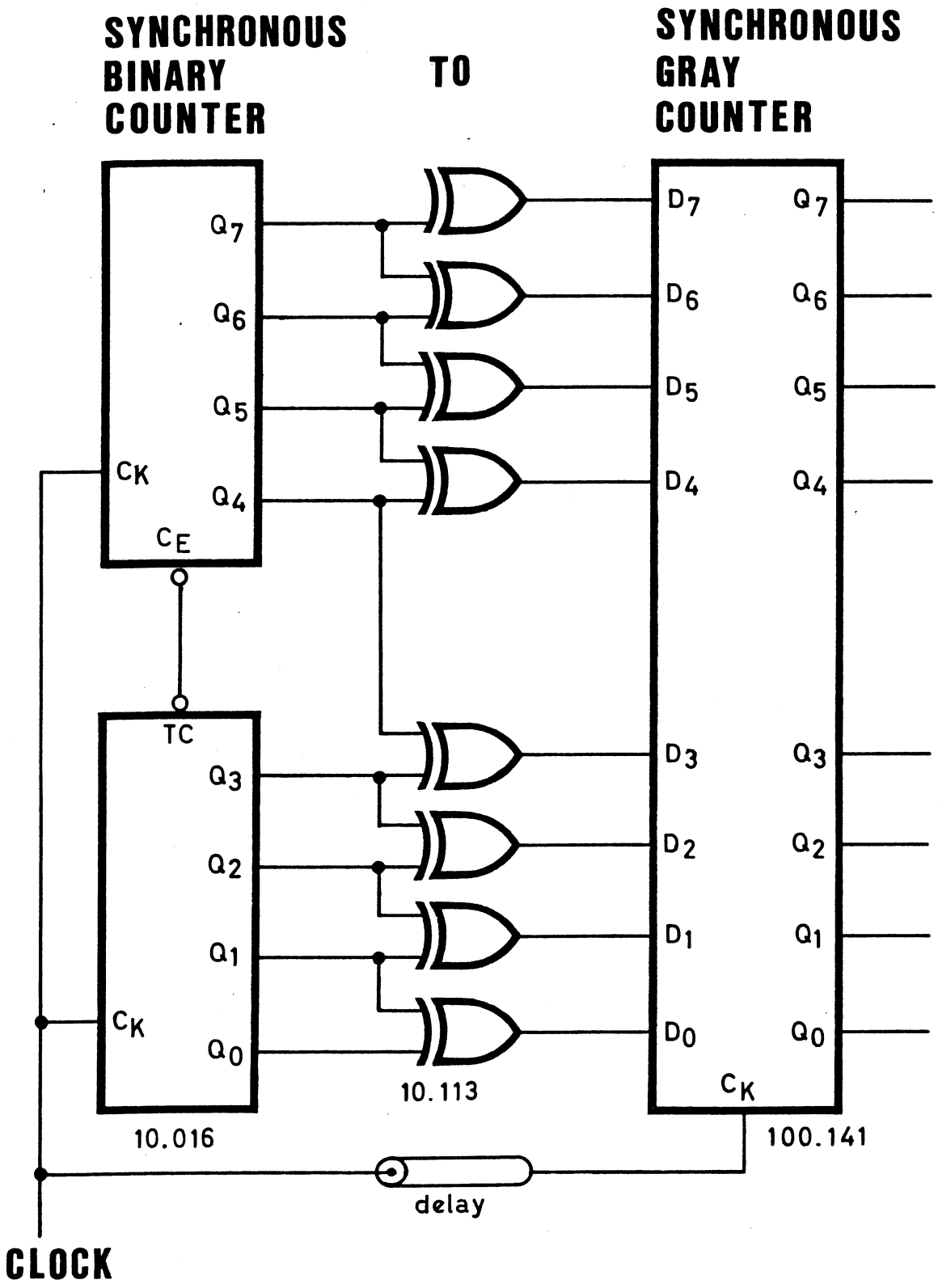

SYNCHRONOUS
BINARY
COUNTER
TO
SYNCHRONOUS
GRAY
COUNTER
Q7
Q6
Q5
CK
Q4
CE
TC
Q3
Q2
Q1
CK
Q0
10.016
10.113
D7
D6
D5
D4
D3
D2
D1
D0
CK
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
100.141
delay
CLOCK

Fig. 6

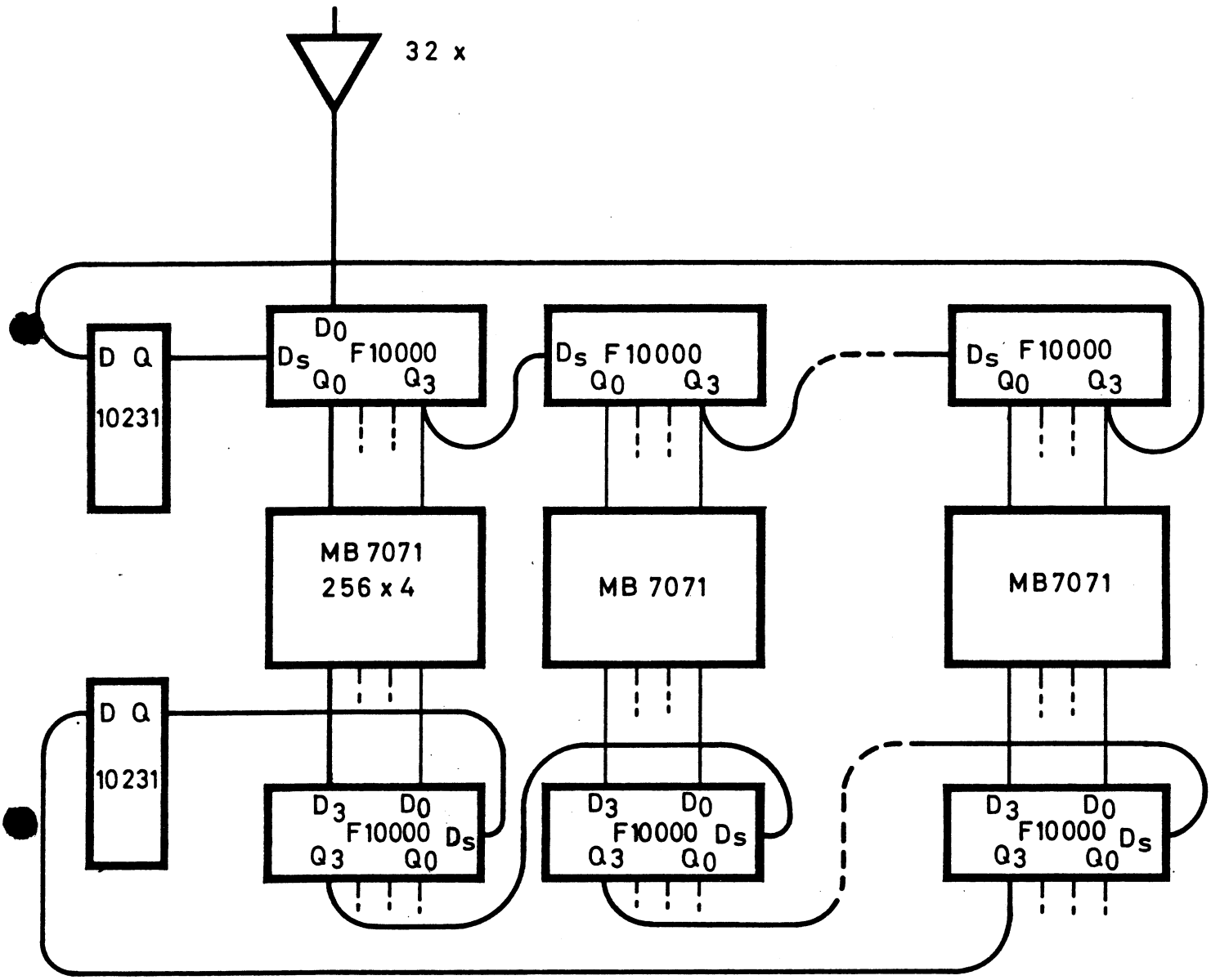

32 x
D Q
10231
D0
Ds F10000
Q0 Q3
Ds F10000
Q0 Q3
Ds F10000
Q0 Q3
MB 7071
256 x 4
MB 7071
MB7071
D Q
10231
D3 D0
F10000 Ds
Q3 Q0
D3 D0
F10000 Ds
Q3 Q0
D3 D0
F10000 Ds
Q3 Q0

Fig. 7

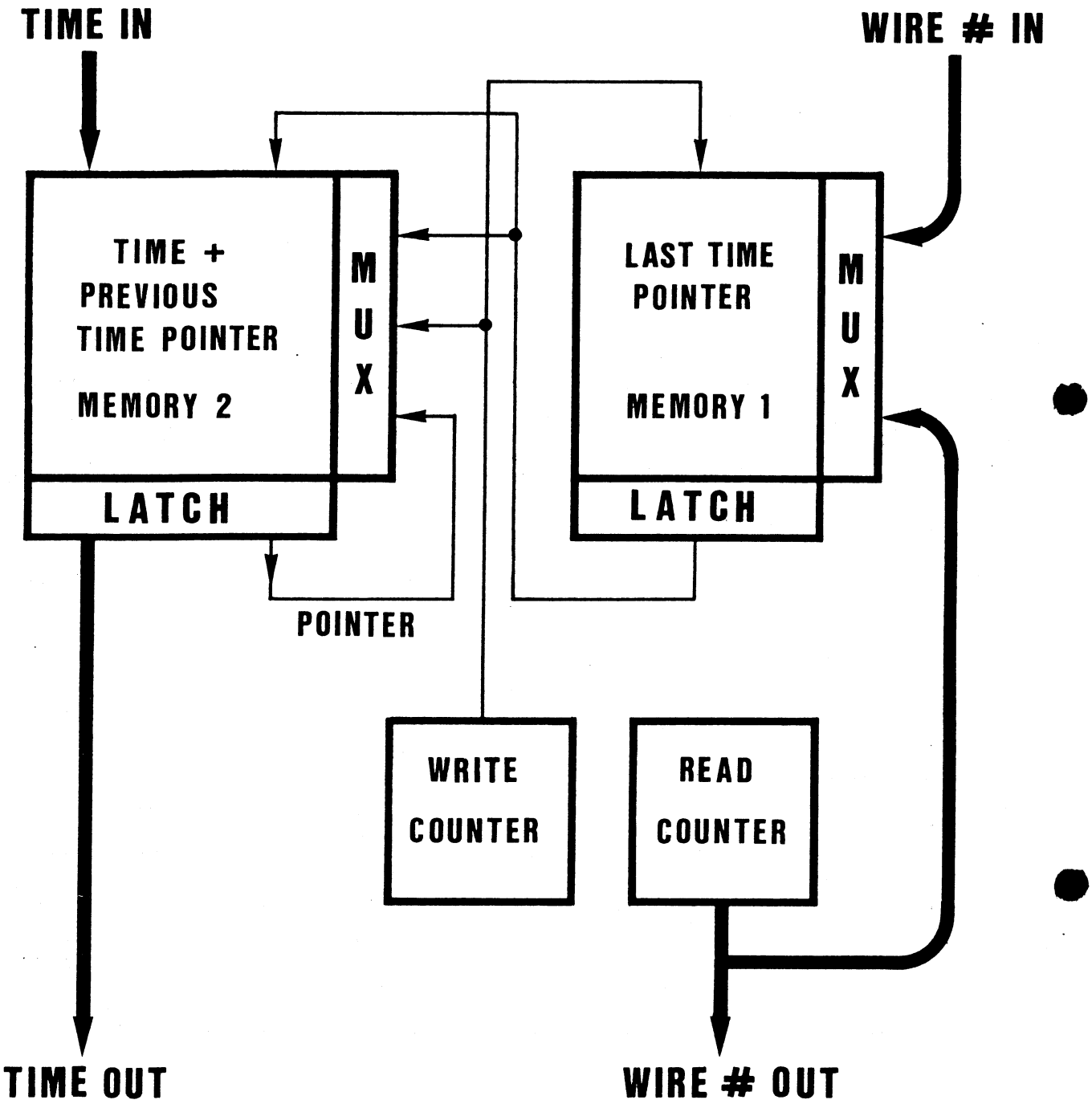

TIME IN
WIRE # IN
TIME +
PREVIOUS
TIME POINTER
MEMORY 2
MUX
LAST TIME
POINTER
MEMORY 1
MUX
LATCH
LATCH
POINTER
WRITE
COUNTER
READ
COUNTER
TIME OUT
WIRE # OUT

Fig. 8