A serial powering scheme for the ATLAS pixel detector at sLHC

2010 JINST 5 C12002

(http://iopscience.iop.org/1748-0221/5/12/C12002)

PUBLISHED BY IOP PUBLISHING FOR SISSA

RECEIVED: *October 15, 2010*
ACCEPTED: *November 15, 2010*
PUBLISHED: *December 1, 2010*

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS 2010,
20–24 SEPTEMBER 2010,
AACHEN, GERMANY

2010 JINST 5 C12002

A serial powering scheme for the ATLAS pixel detector at sLHC

L. Gonella,[1] **D. Arutinov, M. Barbero, A. Eyring, F. Hügging, M. Karagounis, H. Krüger and N. Wermes**

Physikalisches Institut, Universität Bonn,
Nussallee 12, D-53115 Bonn, Germany

E-mail: laura.gonella@physik.uni-bonn.de

ABSTRACT: Powering concepts, such as serial powering and DC-DC conversion, are in development for the silicon trackers at sLHC to achieve an efficient power distribution with a minimum volume of cables. This paper will describe the serial powering scheme developed for the upgraded ATLAS pixel detector, with focus on the scheme architecture and on the main components involved: the Shunt-LDO regulator and the protection scheme. Issues connected to system aspects will be discussed, and the advantages in terms of material reduction provided by the proposed serial powering scheme will be presented.

KEYWORDS: Voltage distributions; Particle tracking detectors (Solid-state detectors)

[1]Corresponding author.

doi:10.1088/1748-0221/5/12/C12002

Contents

2010 JINST 5 C12002

1 Introduction

As explained in [1], the independent and parallel powering schemes used by the LHC trackers suffer from low efficiency, and given the required cable cross section are very massive. In the present ATLAS pixel detector for instance, the power efficiency is around 20%, the amount of power cables has become a significant fraction of the detector material, and the cable channels are saturated. At the higher granularity and currents expected for the inner detectors at sLHC,[1] these powering schemes will not meet the requirements. New powering concepts have to be investigated which allow to transmit power at low currents and high voltages, to achieve high power efficiency while keeping the material budget low. Serial Powering (SP) offers one possibility to address the sLHC powering challenges [3, 4].

In a SP scheme, a chain of n modules is powered in series by a constant current (figure 1), and the voltages are generated by regulators implemented locally. Only two lines per chain are needed. Depending on the number of modules connected in series, SP allows a drastic reduction of the number of power lines, as well as of the transmitted current (figure 1, 2). Moreover, in SP the voltage drop on the cables is not fixed by safety concerns on the regulator,[2] but only by the allowed power density and by the output voltage capability of the current source. Thus the power dissipation on the cables can be chosen to find the optimal trade off between material and power efficiency. These features lead to a great reduction in cable mass (less cables with smaller cross section), whilst increasing efficiency (smaller resistive loss on the cables) and reducing costs (reduced number of power supplies needed). SP requires, however, a protection scheme to avoid loosing an entire chain in case of failures in one of the modules, and to have control over single

[1] According to the current layout for sLHC [2], the number of channels of the ATLAS pixel detector increases approximately by a factor 6, the total current consumed by the electronics is about three times higher than presently, and the power consumption almost doubles.

[2] The input voltage that a regulator sees, when powered via a voltage source, is the supply voltage minus the voltage drop on the cables ($V_{in} = V_{supply} - V_{drop}$). Considering the worst case assumption that a zero voltage drop on the cables can occur, the supply voltage cannot exceed the maximum allowed input voltage of the regulator. This in turn sets an upper limit on the voltage drop on the cables.

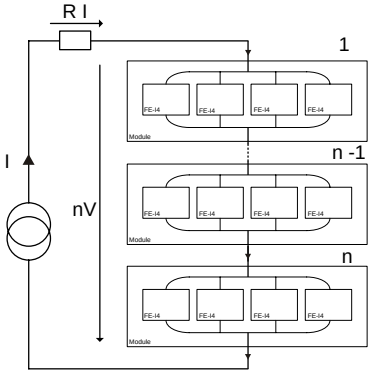

Figure 1. Schematical design of a SP scheme. The current is reduced by a factor n, where n is the number of modules in the chain, with respect to a parallel powering scheme where the same number of modules is powered by a constant voltage.

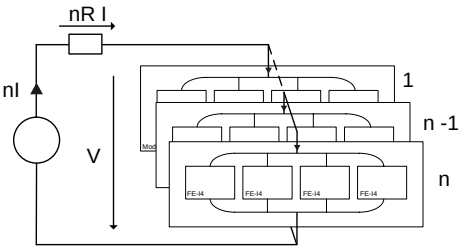

Figure 2. Schematical design of a parallel powering scheme.

modules as in the traditionally used powering schemes. Issues connected to system aspects such as AC-coupled module readout and HV distribution have to be considered as well.

Based on the experience acquired with an alternative powering scheme for the ATLAS pixel detector [5], a SP scheme is proposed for the upgrade of the ATLAS pixel detector at sLHC. The scheme architecture as well as its main elements will be discussed in this paper, after a brief description of the ATLAS pixel detector design for sLHC.

2 The ATLAS pixel detector at sLHC

The current design of the ATLAS pixel detector for sLHC foresees 4 to 5 barrel layers, and 6 disks per side in the foreward region. Given the different requirements, two dedicated developments are ongoing for the two innermost layers, and for the outer layers and disks respectively. The design of the inner layers requires advanced technologies to cope with the high rate and the radiation environment. For the outer layers and the disks which cover a very large area at lower radiation levels and particle rates, the main requirements are simplicity and reduction of construction costs and time. The idea is thus to extend the available hybrid pixel technology to large area detectors, i.e. identify and counteract main costs drivers.

As a consequence of this choice, the developement of a stave concept and of a first prototype for the outer layers is proceeding fast. Figure 3 illustrates the stave concept [6]. In the baseline design, modules consists of arrangements of 2 by 2 FE-I4 chips.[3] 32 modules are mounted on each stave, 16 on the top and 16 on the bottom. Each stave quarter (i.e. 8 modules) is an electrical unit served by one stave cable and one End Of Stave (EOS) card. The stave cable is a multi-layer cable integrated in the stave structure with pre-bent tabs glued on the stave surface. A module flex with

[3]FE-I4 is the new ATLAS pixel front-end chip [7]. Its development targets both the Insertable B-Layer (IBL) project [9] and the ATLAS pixels outer layers at sLHC.

2010 JINST 5 C12002

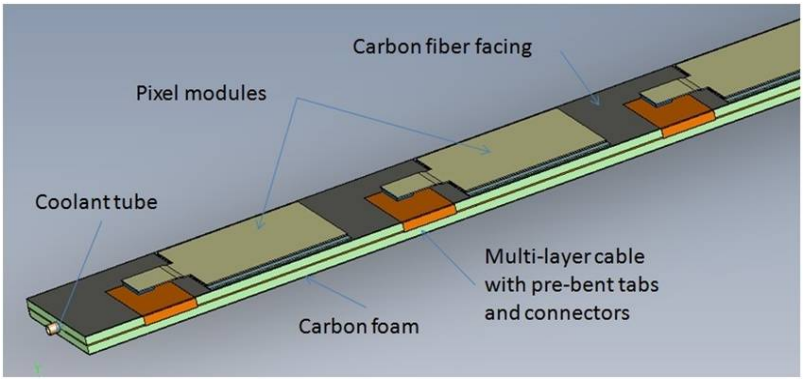

Figure 3. Mechanical drawing of an outer layer stave of the ATLAS pixel detector at sLHC [6]. The stave is double sided with modules mounted on the top and on the bottom of the stave.

pigtail connects to the tabs for electrical connection between the modules and the stave cable. The Detector Control System (DCS) and the GBTX [8] are mounted on the EOS card.

3 Serial powering architecture for the upgraded ATLAS pixel detector

Following the baseline stave concept for the ATLAS pixel detector outer layers at sLHC, a SP scheme is being developed for power units of 8 modules. The nominal current distributed to every SP chain is the current needed for one module (about 2.4A) plus some extra current needed by the regulator. On the module, the current is distributed in parallel to the 4 FE chips. In every chip two Shunt-LDO regulators convert the current to 1.5V and 1.2V, respectively used as the analog and digital supply of the FE-I4.

The Shunt-LDO is a new regulator concept developed for serial powered systems, which combines a shunt transistor and a Low Drop Out (LDO) voltage regulator (figure 4). Two prototypes demonstrated the working principle and showed the good performance of both the regulator standalone and of regulators placed in parallel or in series. A detailed description of the regulator, as well as characterization results for the first prototype are presented in [10]. The design of this regulator makes it very robust against process variations and mismatch, and allows safe parallel operation of the regulators. In addition, parallel operation of regulators generating different output voltages is possible. This is shown in figure 5, where the I-V characteristic of two Shunt-LDO regulators connected in parallel generating Vout1 = 1.5V and Vout2 = 1.2V can be seen. Thanks to these features, the eight Shunt-LDO regulators on the module can be operated in parallel, thus adding significant redundancy to the scheme: should one regulator fail, the current can still flow in the other regulators and the chain is not interrupted. The Shunt-LDO is in fact also designed to be able to cope with increased supply currents (up to the maximum allowed shunt current of 0.6A).

A crucial point for the SP scheme is the efficiency of the regulator. For the 2 Shunt-LDO regulators in FE-I4 operating in parallel, three sources of inefficency have to be considered: (1) the dropout voltage of the LDO (V_{drop}), (2) the extra shunt current (I_{shunt}), and (3) the difference in the output voltages of the two regulators (ΔV). As shown in table 1, the calculated nominal efficiency is 74%.

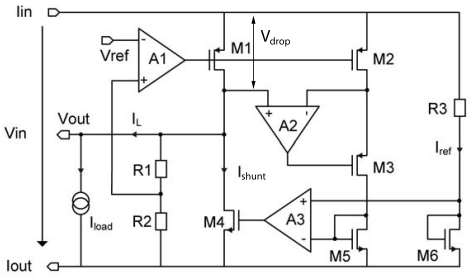

Figure 4. Simplified schematic of a Shunt-LDO regulator.

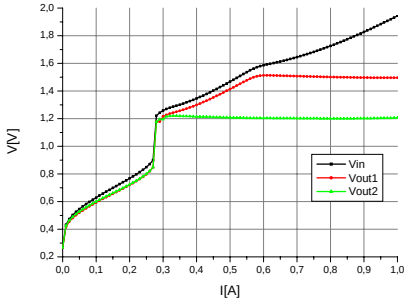

Figure 5. I-V characteristic of two shunt-LDO regulators placed in parallel, generating different output voltages. The output voltages settle at 1.5V and 1.2V, after saturation of all the transistors in the design [10].

Table 1. Power efficiency calculations for two Shunt-LDO regulators connected in parallel generating different output voltages.

	nominal	worst case	best case
Vout1	1.5V	1.5V	1.5V
Vout2	1.2V	1.2V	1.2V
I1	0.36A	0.40A	0.36A
I2	0.24A	0.27A	0.24A
V_{drop}	0.2V	0.2V	0.1V
I_{shunt}	0.03A	0.05A	0.01A
Eff	74%	71%	83%

Together with the regulator, the main component of the proposed SP scheme is the stave protection. One concern would be the injection of noise along the power line due to a mal-functioning module. This scenario has however been studied in great detail using artificial noise sources and has been found not to be critical [5]. As already explained, failures in the regulators are addressed by redundancy in the regulator connection at module level. Redundancy will be also added to the interconnection between modules and power lines, e.g. by making use of multiple wire bonds. Although these measures assure a very robust design, extra care has to be taken for possible worst case failures, in particular for the case of an open circuit fault in the current line which can cause overvoltage. A protection scheme featuring real time response is thus needed. Slow control is also desirable in order to have control over individual pixel modules.

The envisaged protection scheme embeds both features in a Module Protection Chip (MPC) (figure 6). The key element of the MPC is a bypass transistor (M_{bp}), which can be controlled independently by the DCS via an AC-coupled control line with rectifier (D1, D2, C), and by an over voltage protection circuit integrated in the chip itself (OV). In addition, the voltage across the

2010 JINST 5 C12002

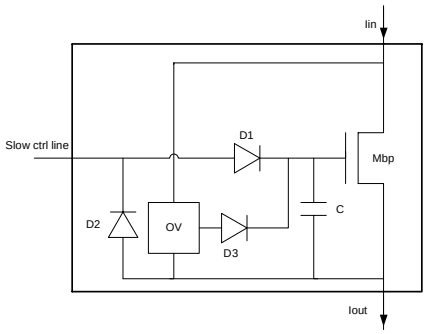

Figure 6. Simplified schematic of the MPC.

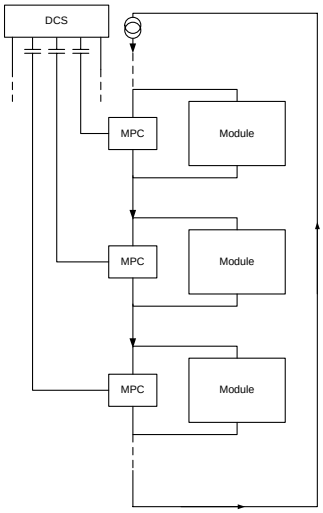

Figure 7. Schematical drawing of the protection scheme.

modules can be monitored by the DCS via the AC-coupled control line when idle. As shown in figure 7, each module will be equipped with its own MPC, so that the DCS can selectively turn the module on or off. In case of an open-circuit, the over voltage protection can react independently to protect the module, and the DCS can then switch off the module completely. As the MPC will be connected directly to the power lines on the module flex, a power on sequence can be defined in which the modules are powered one by one.

The MPC will be implemented in a commercial 130nm CMOS technology for radiation hardness. Simulations so far show that the bypass transistor should be a Dual Gate NMOS transistor with minimum length and width of 4.8mm, to withstand the maximum voltage across the module (2.5V),[4] and to shunt the maximum current (3.5A). For the slow control circuitry, the diodes D1 and D2 are implemented as PMOS transistors, and the capacitor C is the parasitic gate-source capacitor C_{GS} of the bypass transistor (33pF). On the DCS side, a 100nF capacitor is used. A signal of 2.6V in a frequency range from 100k to 1MHz from the DCS can effectively turn on the bypass transistor: the current flows in the bypass transistor and the module voltage is 60mV. For the over voltage protection a silicon controlled rectifier is envisaged.

System issues connected to the SP scheme are considered as well. For the module readout, AC-coupling at the receiver input is proposed. This solution requires receivers with self-biased inputs and DC-balanced data. A self-biasing circuitry was integrated in FE-I4 for the LVDS receiver, whilst an external one can be used for the SLVS (Scalable Low Voltage Signaling) receiver in the GBTX. The clock is inherently DC-balanced, and the standard FE-I4 output data are 8b10b encoded. Only the commands are not DC-balanced. However, their transmission speed is only 40Mbps and the FE-I4 LVDS receiver is a rail-to-rail receiver which could accomodate some common mode shift due to non DC-balanced data. An alternative/fallback solution could be a link with feedback as in [5].

[4]The maximum voltage across the module is defined by the maximum input voltage of the Shunt-LDO.

2010 JINST 5 C12002

Table 2. Material added in the active area of the detector by the serial powering scheme (SP) and by the independent powering scheme with DC-DC conversion (DC-DC) proposed for the upgraded ATLAS pixel detector. The material is expressed in percentage of radiation length, X_0, per pixel layer.

	SP	DC-DC
Current conversion factor	8	2
Power lines	0.056% x/X_0	0.138% x/X_0
AC-coupling	0.018% x/X_0	-
Protection scheme	0.010% x/X_0	-
External capacitors	-	0.015 x/X_0%
Total	**0.084% x/X_0**	**0.153% x/X_0**

The HV connection and distribution to the serial powered modules can either be done point-to-point or by grouping together all modules in a SP chain to one HV power supply. In this case the total potential difference of the modules in the chain has to be taken into account because the common HV is referenced locally to the potential of each module. It is however expected that this will not be a severe issue as the module voltage is of only a few V.[5]

To demonstrate the feasibility of the proposed SP scheme, an ATLAS pixel outer layer stave prototype will be built using dedicated stave cable and module flex for current routing in a SP fashion.

4 Material reduction

Table 2 shows a comparison between the material added in the active area of the detector by the proposed SP scheme and by the other powering scheme under investigation for the ATLAS pixel detector at sLHC, i.e. independent powering with DC-DC conversion[6] [12]. For a power dissipation on the power lines of about 6% of the total stave power, as fixed by design for the scheme with DC-DC conversion, and given the different current conversion factors, SP allows a reduction of 50% in material. However, as already mentioned, the voltage drop and thus the losses on the cables are not fixed in a SP scheme. As shown in figure 8, more material can be saved in the active area of the detector by allowing slightly higher power densities.

5 Conclusions

A serial powering scheme is being developed for the ATLAS pixel detector at sLHC. The Shunt-LDO, a new regulator concept targeting serial powering needs, has been largely prototyped and tested, showing good performances. For operation in the new ATLAS pixel front-end chip, FE-I4,

[5]Depending on the chosen powering scheme (section 4), the module voltage will be 1.7V (SP) or 3.5V (direct powering with DC-DC conversion).

[6]This scheme foresees the use of a charge pump DC-DC converter [11] with conversion factor two integrated in FE-I4. A voltage regulator/first stage conversion will be placed on a patch panel about 14m away from the detector. The maximum allowed voltage drop between converter and regulator is 1V, of which 0.2V are on the stave cable.

2010 JINST 5 C12002

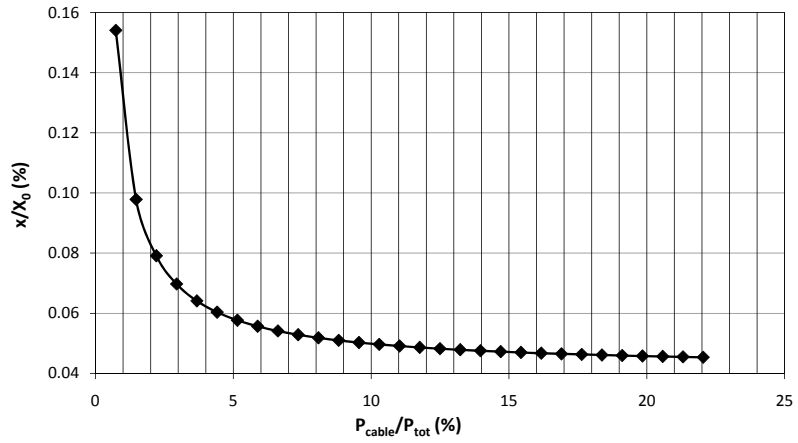

Figure 8. Material added in the active area of the detector by the power lines of the proposed SP scheme (in unit of percentage of radiation length) as a function of the power dissipation on the lines normalized to the total stave power.

where two Shunt-LDO regulators generating different output voltages are placed in parallel, the calculated power efficiency is 75%. A protection scheme featuring slow control and fast response is developed, whose main element is the Module Protection Chip. As shown, in the active area of the detector the proposed SP scheme requires 50% less material than the independent powering scheme with DC-DC conversion which is also considered for the upgrade of the ATLAS pixel detector at sLHC.

References

[1] M. Weber, *Power distribution for SLHC trackers: challenges and solutions*, *Nucl. Instrum. Meth.* **A 592** (2008) 44.

[2] L. Rossi, *ATLAS Upgrade Week*, November 2009, CERN, Geneva, unpublished.

[3] T. Stockmanns et al., *Serial powering of pixel modules*, *Nucl. Instrum. Meth.* **A 511** (2003) 174.

[4] T. Stockmanns, *Multi chip module development for the ATLAS pixel detector* (in German), PhD thesis, BONN-IR-2004-12 (2004).

[5] D.B. Ta et al., *Serial powering: proof of principle demonstration of a scheme for the operation of a large pixel detector at the LHC*, *Nucl. Instrum. Meth.* **A 557** (2006) 445.

[6] M. Gilchriese and M. Garcia-Sciveres, *ATLAS Upgrade Week*, November 2009, CERN, Geneva, unpublished.

[7] M. Barbero et al., *FE-I4 ATLAS Pixel Chip Design*, PoS(VERTEX 2009)027.

[8] P. Moreira et al., *The GBT project*, Twepp 2009 Conference, Paris, Proceedings of TWEPP 2009.

[9] M. Capeans et al., *ATLAS Insertable B-Layer Technical Design Report*, CERN-LHCC-2010-013, ATLAS-TDR-019.

2010 JINST 5 C12002

[10] M. Karagounis et al., *An integrated Shunt-LDO regulator for serial powered systems*, ESSCIRC '09 Conference, Athens, Proceedings of ESSCIRC '09, 276.

[11] P. Denes, R. Ely and M. Garcia-Sciveres, *A capacitor charge pump DC-DC converter for physics instrumentation*, *IEEE Trans. Nucl. Sci.* **56** (2009) 1507.

[12] L. Gonella et al., *Towards Minimum Material Trackers for High Energy Physics Experiments at Upgraded Luminosities*, Pixel 2010 Conference, Grindelwald, Proceedings of Pixel 2010, to be published.

2010 JINST 5 C12002