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A module concept for the upgrades of the ATLAS pixel system using the novel SLID-ICV vertical integration technology

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ABSTRACT: The presented R&D activity is focused on the development of a new pixel module concept for the foreseen upgrades of the ATLAS detector towards the Super LHC employing thin n-in-p silicon sensors together with a novel vertical integration technology. A first set of pixel sensors with active thicknesses of 75 μm and 150 μm has been produced using a thinning technique developed at the Max-Planck-Institut für Physik (MPP) and the MPI Semiconductor Laboratory (HLL). Charge Collection Efficiency (CCE) measurements of these sensors irradiated with 26 MeV protons up to a particle fluence of $10^{16}\,n_{eq}cm^{-2}$ have been performed, yielding higher values than expected from the present radiation damage models.

The novel integration technology, developed by the Fraunhofer Institut EMFT, consists of the Solid-Liquid InterDiffusion (SLID) interconnection, being an alternative to the standard solder bump-bonding, and Inter-Chip Vias (ICVs) for routing signals vertically through electronics. This allows for extracting the digitized signals from the back side of the readout chips, avoiding wire-bonding cantilevers at the edge of the devices and thus increases the active area fraction. First interconnections have been performed with wafers containing daisy chains to investigate the efficiency of SLID at wafer-to-wafer and chip-to-wafer level. In a second interconnection process the present ATLAS FE-I3 readout chips were connected to dummy sensor wafers at chip-to-wafer level. Preparations of ICV within the ATLAS readout chips for back side contacting and the future steps towards a full demonstrator module will be presented.

KEYWORDS: Detector design and construction technologies and materials; Radiation-hard detectors; Particle tracking detectors (Solid-state detectors)

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1 Introduction

While the nominal peak luminosity of the present LHC accelerator is intended to reach $10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, an upgrade to increase this value is planned to be carried out in a two phase process [1]. This poses new challenges especially to tracking detectors in terms of radiation tolerance and track discrimination power. They have to be more radiation tolerant and allow for a higher track discrimination power. For phase 1, foreseen to start in 2016, a new innermost pixel layer will be mounted on a new beam pipe and inserted into the present innermost layer of the ATLAS pixel detector. For the phase 2 upgrade (HL-LHC), expected to be realized beyond 2020 and reaching a maximum luminosity of $(5-10)\cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, a completely new ATLAS tracking detector with a reduced minimum radius is foreseen. The pixel modules for both upgrades have to be very compact, sustain integrated fluences of several $10^{15}\,\mathrm{n_{eq}cm^{-2}}$ (1 MeV neutron equiv.) after the phase 1 and up to $10^{16}\,\mathrm{n_{eq}cm^{-2}}$ after the phase 2 upgrade. Their material budget should be reduced to minimize multiple scattering. At the Max-Planck-Institut für Physik (MPP) an new module concept (figure 1) is developed that aims to fulfill all these requirements as explained in the following.

The defects in the semiconductor sensors resulting from the high integrated fluence cause higher leakage currents and reduce the charge collection distance to values smaller than standard sensor thicknesses of $(250-300)\,\mu$m. This leads to a higher noise contribution and a reduced charge collection efficiency (CCE). Adjusting the thickness of the sensors towards the final expected collection distance reduces the material budget and hence multiple scattering without losing CCE. Furthermore, thin sensors will have a modified electric field distribution which, at the same bias voltage, should increase the amount of charge collected after irradiation compared to standard thickness sensors.

To increase the fraction of active area of the pixel modules a design employing the novel vertical integration technology of the EMFT[1] is envisaged (see figure 1). This technology consists of the Solid-Liquid InterDiffusion (SLID) interconnection and Inter-Chip Vias (ICV) [2]. The SLID interconnection in comparison to the standard solder bump-bonding has a lower material

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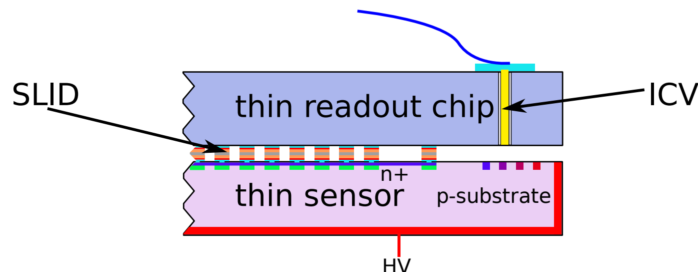

Figure 1. The MPP module concept using thin n-in-p sensors and the SLID-ICV vertical integration technology applied to the present ATLAS readout chip geometry. In order to contact the ICV from the chip back side, the readout electronics are thinned to $(50-60)\,\mu$m.

budget, higher flexibility of the contact pad geometries, and possably lower cost. The ICV that will be placed into the ATLAS readout electronics (figure 1) are produced by deep reactive ion etching of channels through the devices which are subsequently filled with tungsten. The signal transport to the readout pads on the back side of the chips gives a very compact four side buttable devices.

2 Thin pixel sensors

Using a new wafer thinning technology developed at the MPP and HLL the thickness of the pixel sensors can be adjusted freely [3]. A first production of eight n-in-p 6-inch float zone wafers with active thicknesses of $75\,\mu$m and $150\,\mu$m has been successfully completed on a $2\,\mathrm{k}\Omega$cm substrate. The n-in-p material only needs single sided structured processing (figure 1) and hence gives a reduction of the needed number of production masks and consequently the price. This can be done since the n-in-p sensors will not undergo type-inversion during irradiation and always develop the pn-junction starting from the readout side of the sensors.

On each of the wafers pixel-, strip-, and pad sensors are placed. The pixel sensors are compatible with the present ATLAS FE-I3 readout chip [4]. The strip implant length is 7 mm. With respect to the punch through biasing and the inter-implant isolation, the strip sensors are identical to the pixel sensors. However, next to strip sensors with a pitch of $50\,\mu$m also sensors with $80\,\mu$m pitch are implemented. The pad sensors are used to characterize the silicon bulk properties.

A first characterization of the n-in-p structures [5] was carried out before irradiation and showed a very high device yield (79/80 for pixel sensors). The measured full depletion voltage of pad sensors is around 20 V for the $75\,\mu$m and 80 V for the $150\,\mu$m thin sensors. These values are also expected from the known resistivity. The maximum full depletion voltage for pixel sensors is always below 120 V, i.e. far below the break down voltages of $(300-600)$ V. The leakage currents are less than $10\,\mathrm{nA/cm^2}$.

For strip sensors with an $80\,\mu$m pitch the CCE has been measured with the ALIBAVA readout system [6] after irradiation with 26 MeV protons up to a fluence of $10^{16}\,\mathrm{n_{eq}cm^{-2}}$. The CCE measurement set-up is based on a ^{90}Sr source in combination with a scintillator trigger system. The leakage current, increasing linearly with the fluence, contributes to the shot noise of the system and degrades the chip output signal linearity. Hence, to keep the leakage current $\leq 5\,\mu$A, the measure-

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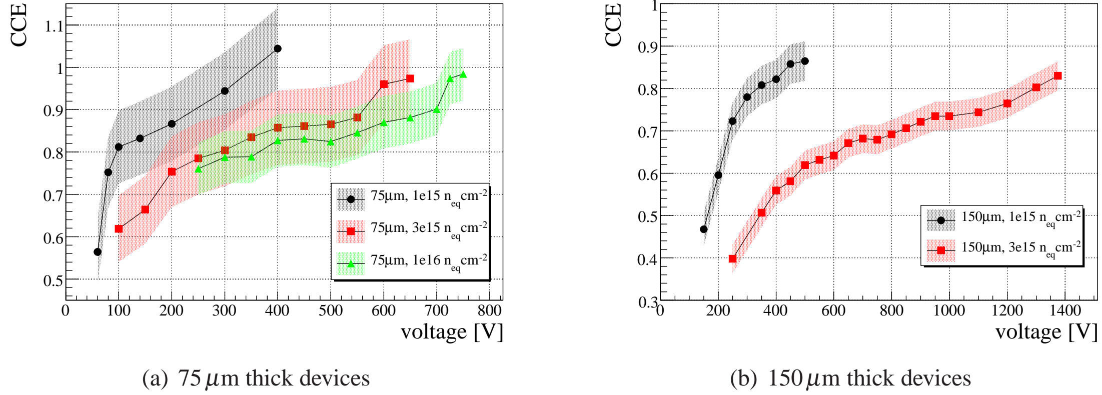

(a) 75 μm thick devices

(b) 150 μm thick devices

Figure 2. Charge collection efficiencies of irradiated strip sensors as a function of the bias voltage. Shown are the sensors with an active thickness of 75 μm (a) and 150 μm (b).

ments have been performed at -30 °C or at -46 °C. Two not irradiated sensors were used to obtain a calibration of the expected signal size before irradiation for 75 μm and 150 μm thick sensors.

The results of the CCE measurements are shown in figure 2. For each charge measurement the uncertainty was assumed to be 500 e^-. This value has been estimated by various repetitions of the same measurement using different input parameters for the analysis. Within uncertainties, the 75 μm thick sensors can recover the full charge measured before irradiation up to the maximum fluence of $10^{16}\,n_{eq}cm^{-2}$, when biased at voltages around 750V. The 150 μm thick sensors need voltages above 800V to achieve a CCE above 70% at a fluence of $3 \cdot 10^{15}\,n_{eq}cm^{-2}$. At 1400 V the measured CCE is (83±4)%. The measurements for the 150 μm thick sensors irradiated to a fluence of $10^{16}\,n_{eq}cm^{-2}$ are still ongoing.

The measurements for both active thicknesses at high applied bias voltages result in a CCE larger than expected from the calculations based on the current radiation damage models [5]. This effect has also been observed by other groups with devices irradiated to high fluences and it has been interpreted as an avalanche multiplication process taking place in the first microns below the n^+ electrodes, in the area of highest electric field of the detectors [7, 8]. Hence, this effect is observed to be more pronounced in thin sensors, i.e. [9].

3 SLID interconnection technology

The SLID interconnection technology representing an alternative to the standard bump-bonding, is characterized by a very thin eutectic Cu-Sn alloy. To prepare the sensor and the readout chip for SLID, a 100 nm thin TiW diffusion barrier is placed on the metallized contact pads. This has been shown to prevent atoms from the 5 μm copper layers electroplated on both devices to diffuse into the silicon [10]. In addition, on one of the two copper layers a 3 μm thin layer of tin is applied. To form the connection the two devices are aligned, brought in contact, and heated at an applied pressure of 5 bar to a temperature of around (240 – 320)°C. At this temperature the tin diffuses into the copper to form the Cu-Sn alloy. As the melting point of this alloy is around 600°C multiple layers can be stacked and connected without melting the SLID connections

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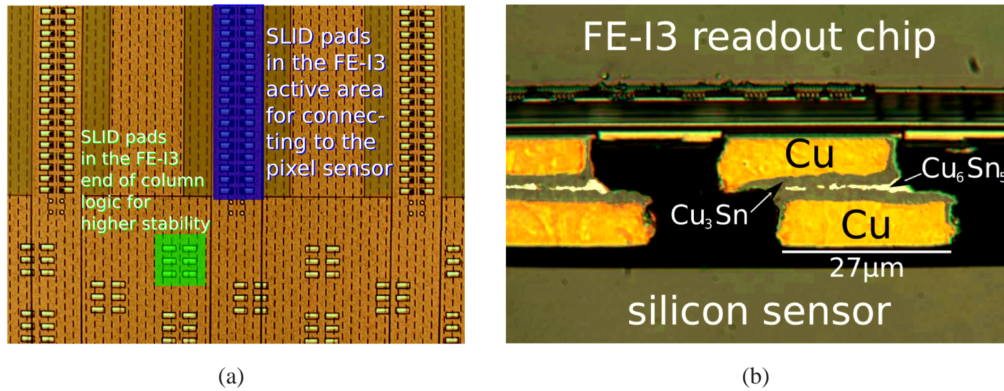

(a) (b)

Figure 3. The SLID interconnection applied to the ATLAS FE-I3 pixel readout chip. In (a) the blue rectangle marks the SLID pads that connect to the sensor pixel cells whereas the green rectangle denotes a group of SLID pads that are used in the area of the end of column logic to increase the mechanical stability of the module. A cross section of an FE-I3 chip connected to a dummy sensor is shown in (b). Clearly visible are the different phases of the Cu-Sn alloy. In this case a relative misalignment of around 10 μm is visible.

already present. Compared to the bump-bonding technology less process steps are needed for SLID supposably resulting in a cost reduction for the detector construction.

The devices can be connected either wafer-to-wafer or chip-to-wafer. A first production mainly containing daisy chains has been carried out on two pairs of wafers to study the applicability of the SLID interconnection between the sensor and readout electronics for an ATLAS pixel module. Different SLID pad sizes and pitches as well as deliberate imperfections in the wafer surfaces were implemented to explore the limits of the technology [11]. The imperfections of the silicon surface are realized by introducing steps in the SiO_2 (100 nm) or the aluminum (1 μm) layer below the SLID interconnection pad. For most of the chains all SLID connections were faultless, and the SLID measurements yielded overall inefficiencies of less than 10^{-3} for most of the tested chains. In particular, the efficiency for the SLID pad geometry implemented in the thin pixel production, with dimensions of 27 μm $\times$ 60 μm, has been estimated to be $(5\pm1)\times 10^{-4}$. Within the present uncertainties, neither the contact size nor the reduction of the surface planarity severely affect the performance of the SLID interconnection. Next to the daisy chains alignment structures to optically and electrically measure the pick and place precision were implemented. From these a relative misalignment of (5–10)μm was obtained for the connections at wafer-to-wafer level. At chip-to-wafer level unexpected problems lead to a worse misalignment and lower connection efficiencies. However, these problems are understood to originate from boundary conditions of this R&D investigation that will not be present in future productions.

In a second interconnection process the present ATLAS FE-I3 readout chips are planned to be connected to the thin sensors described above. The electroplating of the SLID pads has to be performed at the wafer level. As a first step for the assembly of the demonstrator pixel modules, this has already been completed on one FE-I3 wafer and four sensor wafers, two for each active thickness. Figure 3(a) shows the SLID pads created on the FE-I3 chip. In the active area of the chip the SLID connections establish the electrical contact to the sensor counterpart, whereas in

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the end-of-column logic SLID connection are implemented to increase the mechanical stability of the assembly. The FE-I3 chips have then been singularized and reconfigured onto a 6-inch handle wafer, according to the location of the pixels in the MPP-HLL thin sensor production. A test assembly has been obtained using one handle wafer populated with FE-I3 chips and one dummy sensor wafer, where only the first oxide and an aluminum layer have been deposited. Figure 3(b) shows the cross-section of SLID pads in a FE-I3 module of this wafer. Two different phases of the Cu-Sn alloy are visible, Cu_6Sn_5 and Cu_3Sn, with the latter being the more thermally stable one. The assembly is affected by a misalignment of about (10–15) μm, due to a rotation of the chips in the handle wafer with respect to their nominal position, measured to be in the range of (0.05–0.3) degrees. The SLID interconnection of the FE-I3 chips to the real thin pixel sensors is in preparation, with the chip to wafer technique employed in the test-assembly.

4 Inter-chip vias

The use of ICVs offers the possibility of extracting the signals from the back side of the readout chip. This technique will be applied to the FE-I3 readout chips connected to the thin pixel sensors. The foreseen ICV processing for the FE-I3 starts at wafer level with the etching of the vias on the chip pads originally designed for wire-bonding, after having removed the last aluminum layer. The positions of the ICVs on the pad are visible in figure 4(a) as defined by the mask needed for the first photolitographic step before the etching process. Around the ICVs a 3 μm wide trench is designed to provide an additional isolation of the vias belonging to different pads. The cross section of a via is $3 \times 10\,\mu\text{m}^2$, with an initial depth of 60 μm. They are passivated with tetraethyl orthosilicate and afterwards filled with tungsten in a chemical vapor deposition (CVD) process. As the FE-I3 wafers have an initial thickness of around 650 μm they have to be thinned down from the back side after the via filling until the vias are exposed. After the thinning, an additional process step is needed to form the metal contact pads on the back side. Etching trials have been performed on a test wafer to firstly determine the optimal dimensions of the vias and secondly the process sequence for etching through the different dielectrics layers of the FE-I3 chip. An SEM picture of one of these etching trials is shown in figure 4(b). The R&D activity will continue with the SLID interconnection of the FE-I3 chips with ICVs to the thin pixel sensors, also in this case adopting the chip to wafer technique.

5 Conclusion

A first production of thin pixel sensors with an active thickness of 75 μm and 150 μm has been completed in view of the ATLAS pixel detector upgrades. The electrical characterization before and after irradiation shows an excellent behavior in terms of leakage currents and operability at high bias voltages. CCE measurements performed after irradiation show that it is possible to get the full charge obtained before irradiation in the 75 μm thick sensors at a fluence of $10^{16}\,\text{n}_{\text{eq}}\text{cm}^{-2}$ and 83% of the charge in the 150 μm thick sensors at a fluence of $3 \cdot 10^{15}\,\text{n}_{\text{eq}}\text{cm}^{-2}$. Thin pixel sensors are being connected to FE-I3 chips using the SLID interconnection, a possible alternative to the bump bonding technique. A high interconnection efficiency was measured with daisy chain structures for different pad sizes and pitches. The pixel sensor- and chip wafers have been electroplated and a test assembly of real FE-I3 chips with a dummy sensor wafer has been completed.

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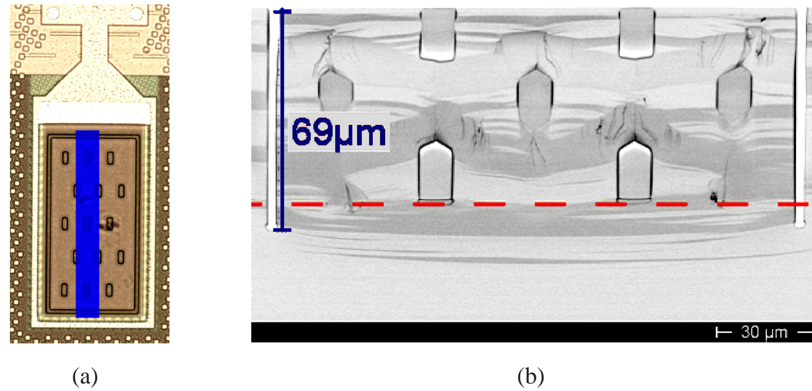

(a) (b)

Figure 4. The preparation of ICV in the wire-bonding pads of the FE-I3 readout chip. A single pad with the foreseen positions of the ICVs and the isolation trench around them is given in (a). A slanted cross-section in the area of the blue rectangle in (a) is shown in (b), exposing the long dimension of the holes for the vias and the isolating trenches. The etching reached to a depth of up to 69 μm, the red dashed line denotes the plane up to which the chip needs to be thinned in order to access the vias from the back side.

The post-processing of the ASIC wafers has started with etching trials to determine the optimal dimensions of the vias and the process sequence.

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