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Study for the LHCb upgrade read-out board

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ABSTRACT: The LHCb experiment envisages to upgrade its readout electronics in order to increase the readout rate from 1 MHz to 40 MHz. This electronics upgrade is very challenging, since readout boards will have to handle a higher number of serial links with an increased bandwidth. In addition, the new communication protocol (GBT) developed by the CERN micro-electronics group mixes data acquisition, slow control and clock distribution on the same link. To explore the feasibility of such a readout system, elementary building blocks have been studied. Their goals are multiple: understand signal integrity when using highly integrated high speed serial links running at 8 - 10 Gbits/s; test the implementation of the GBT protocol within FPGAs; understand advantages and limitations of commercial standard with a predefined interconnection topology; validate ideas on how to control easily such a system. We designed two boards compliant with the xTCA standard which meets an increasing interest in the physics community. The first one is a generic handling 32 high speed serial links. The second one is a communication switch allowing the generic boards to communicate together. In this paper, we present jitter measurements obtained at 8 Gbits/s on serial link. We describe the versatility of this architecture which can be tuned from basic acquisition systems to more high-end complex ones. Finally, we demonstrate the feasibility of a low cost scalable control system based on NIOS core embedded in FPGAs.

KEYWORDS: Modular electronics; Front-end electronics for detector readout; Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases); Data acquisition concepts

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1 LHCb upgrade

Studies of CP violation and more generally flavored changing neutral currents were essential in establishing the Standard Model, as the theory describing the CP violation observed in the laboratory. Today they appear as a powerful tool to reveal processes beyond the Standard Model and to understand their nature. In this context, the LHCb experiment running at LHC will play a major role.

The detector [1] is a single arm forward spectrometer covering the forward region of the proton-proton interaction. It is designed to run at an instantaneous luminosity of 2×10^{32} cm^{-2}s^{-1} and to accumulate an integrated luminosity of 2 fb^{-1} per year. LHCb will collect 5 to 6 fb^{-1} by end of 2015.

The LHCb collaboration envisages to upgrade its detector in 2016 in order to run with an instantaneous luminosity multiplied by a factor 5 (10^{33} cm^{-2}s^{-1}) and with an improved trigger [2]. The new trigger stategy is based on a software trigger running in CPU farm analysing every crossing. It requires to read-out the detector at a frequency of 40 MHz instead of 1 MHz as in the present system, and to re-design the readout architecture.

The new architecture is shown in figure 1.

It is based on the GBT (GigaBit Transceiver) chip [3] developped by CERN. This radhard component serializes the data at high speed and handles simultaneously the data acquisition, the slow control as well as the timing and fast control information.

Reading the detector at 40 MHz instead of 1 MHz, increases the number of optical links between the front-end boards and the common readout boards. In order to minize the cost, the data will be compressed at the front-end level.

The common readout board is the interface between the detector and the online network. On one side, it will be connected to the front-end electronics through serial optical link running at 4.8 Gbits/s and on the other side to the 10 Gigabit Ethernet network. The board mainly encapsulates front-end data into Ethernet frames. Its main characteristic is that the output dataflow is equivalent to the input dataflow. The number of optical links coming from the front-end electronics is estimated to 9500 while the number of 10 Gigabit Ethernet links is around 4800.

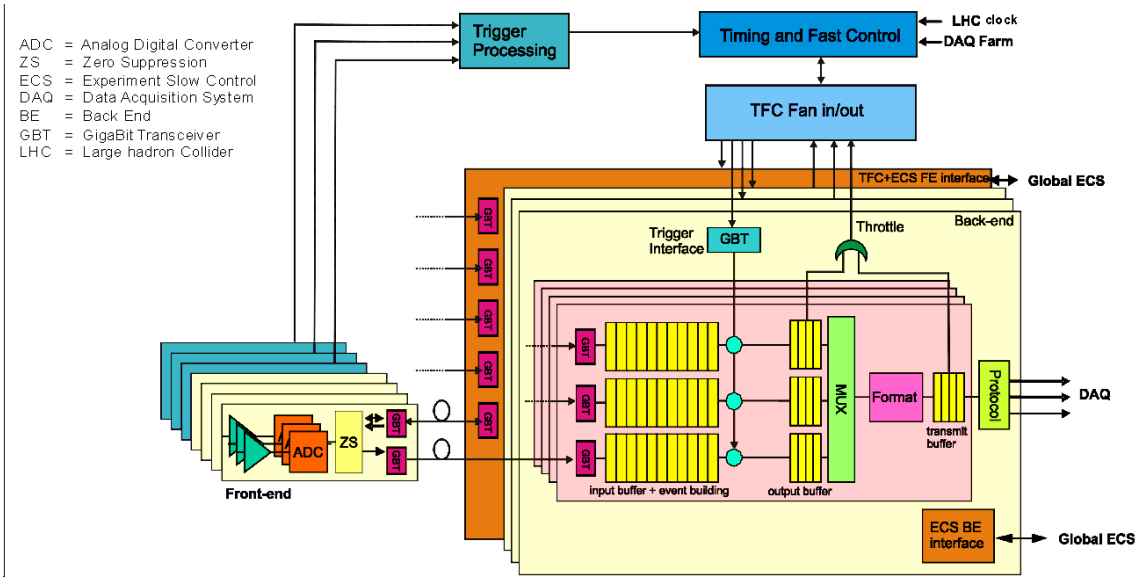

Figure 1. New LHCb read-out architecture.

2 Building blocks for a high speed read-out

In comparison with the current system, the amount of transferred data and the speed will be increased by an order of magnitude. When reaching 10 Gbits/s on serial link, the signal integrity becomes an issue. In order to control it, we designed a prototype able to operate at 4.8 Gbits/s with the GBT protocol [3] and at 10 Gbits/s with the Ethernet protocol.

The prototype is compliant to the xTCA standard (Micro Telecommunication Computer Architecture and Advanced Telecommunication Computer Architecture). Therefore, this architecture allows addressing very simple configurations useful for test, as well as very complex ones handling a large number of serial links, with the same hardware.

Many optical devices have been released in the last months with different form factors and capabilities. Due to this instability of the market, it appeared necessary to decorelate the input/output interface from the processing entity. This was obtained by placing the optical devices on mezzanines.

The slow control processor is embedded in the FPGA (Field Programmable Gate Array). It is close to the GBT interface since the latter merges data and slow control flows. The control processor is a NIOS core which is a RISC (Reduced Instruction Set Computer) processor routed in the FPGA logic array.

The architecture of the prototype is shown in figure 2. It is based on the AMC board (Advanced Mezzanine Card) and the MCH board (MicroTCA Controller Hub) which are compliant with the μTCA standard.

The AMC board is the main component of the system dealing with data acquisition and processing. Optical inputs and outputs are implemented on a mezzanine mechanically compliant with the VITA57 specification [4]. The processing of incoming data is assured by two Stratix IV GX FPGAs from Altera. Each FPGA is connected to the mezzanine by 16 bidirectional serial links.

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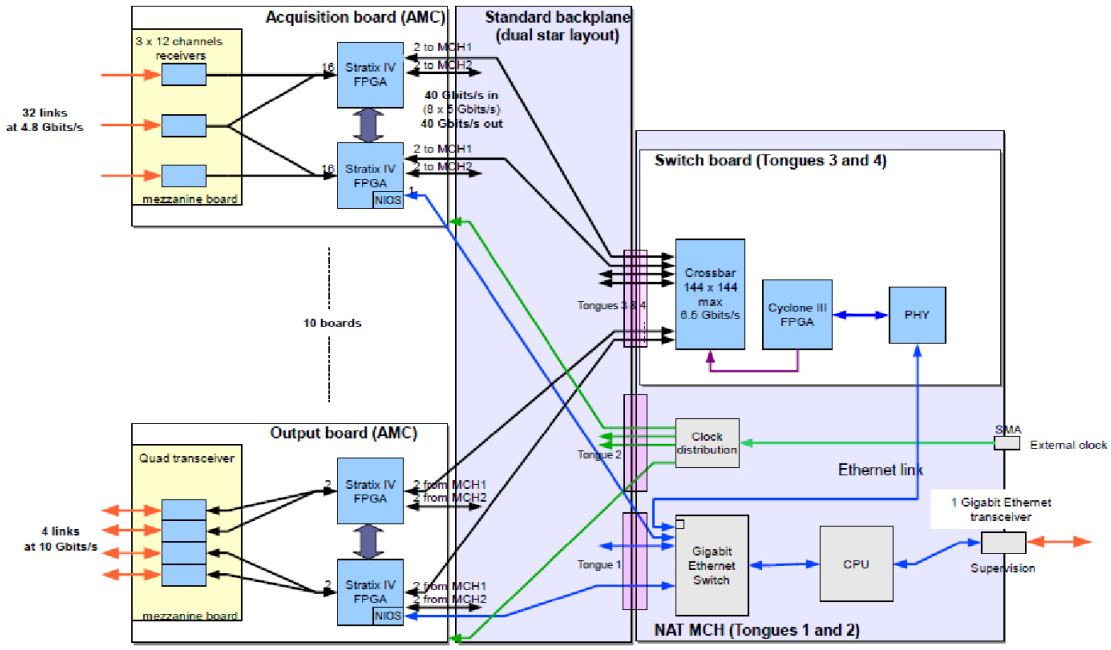

Figure 2. Overall architecture of the prototype.

The board is therefore able to handle 32 bidirectional channels. The maximum speed achievable by these FPGAs is 8.5 Gbits/s.

The board can be upgraded to Stratix IV GT operating to 10 Gbits/s. The board can be equipped with several kinds of mezzanines. Each mezzanine can receive a maximum of three SNAP12 devices (12 channels pluggable optical modules). They can be optical receivers, allowing the reception of 32 inputs, or optical transmitters, allowing the emission of 32 serial output links, or any combination of receiving/transmitting devices. For example, to avoid developing two mezzanines for the prototype, we have designed a single one with one SNAP12 receiver (12 channels in at 4.8 Gbits/s), one SNAP12 transmitter (12 channels out at 4.8 Gbits/s) and one SFP+ transceiver (1 channel in + 1 channel out at 8.5 Gbits/s).

The MCH board is in charge of the clock and slow control distribution. An analog crossbar allows to establish a programmable connection between any pair of FPGA wherever they are located in the crate. To avoid redeveloping a whole complicated MCH board, we designed only the crossbar part as a double mezzanine plugged on top of a commercial board.

The boards are inserted in a standard backplane with a classical redundant double star topology. The center of the star is the MCH board. Therefore, it can propagate an external clock to any AMC board. A Gigabit Ethernet switch located on the MCH allows the slow control to reach any AMC board in the crate from a single PC connected to the MCH board.

3 Performance

The AMC board can be tested alone by connecting its optical outputs on its optical inputs as described in figure 3.

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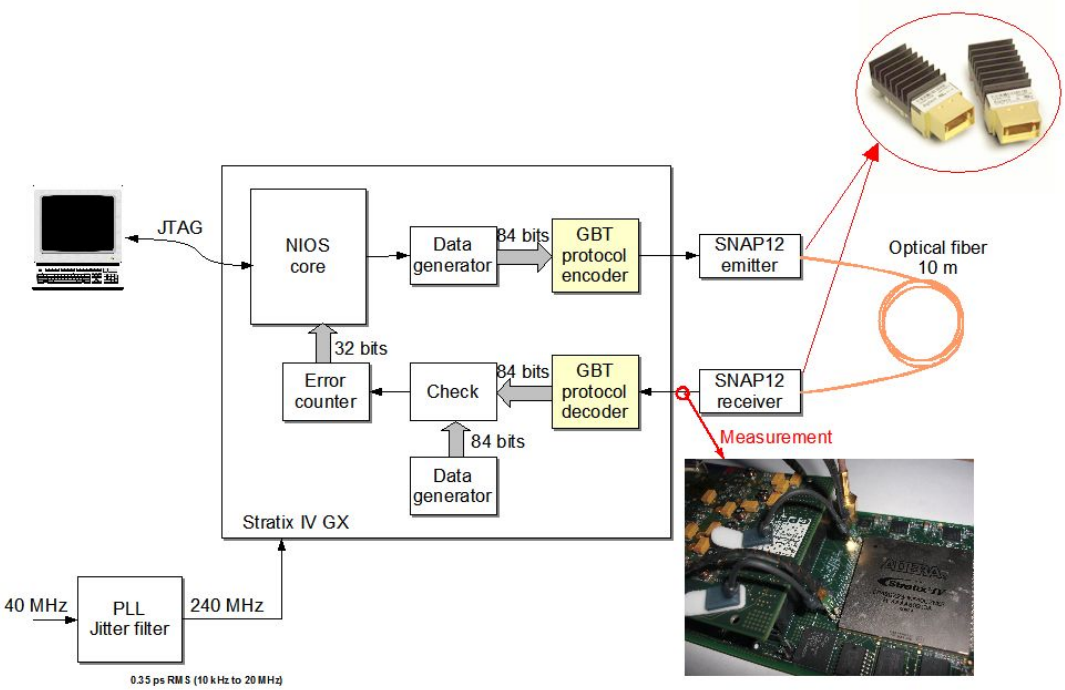

Figure 3. Test Setup to measure performance of high speed serial links.

The GBT protocol is used in all the tests for the transmission. A simple quad 21 bits counter generates known patterns on 84 bits, whereas the protecting code extend the data word to 120 bits as specified in the GBT protocol. On the receiving end the patterns are checked. The bit error rate (BER) and jitter are measured by a Lecroy Serial Data Analyser SDA i870 by soldering differential probes as close as possible of the FPGA input pins.

The GBT emulation showed a perfect eye diagram at 4.8 Gbits/s as shown in figure 4. The total jitter measured is 40 ps peak to peak. The Stratix IV GX requires a minimum eye aperture of 0.35 UI. Therefore, the BER (Bit Error Rate) derived from the bathtub curve is well below 10^{-16}.

At 8 Gbits/s the total jitter increases to 77 ps peak to peak. The closure of the eye diagram is mainly due to attenuation of high speed harmonics which produces inter symbol interference. The estimated BER remains below 10^{-16} for a required aperture of 0.35 UI.

4 Slow control

To study the feasibility of a low cost slow control system, we embed a NIOS core with a Triple Speed Ethernet interface inside the FPGA. The number of cells taken by this functionality is marginal, 4% of a EP1S230KFE FPGA.

We measured the number of transaction per second the NIOS core is able to sustain. A transaction is defined as writing and reading n consecutive words. The performances are summarized in table 1.

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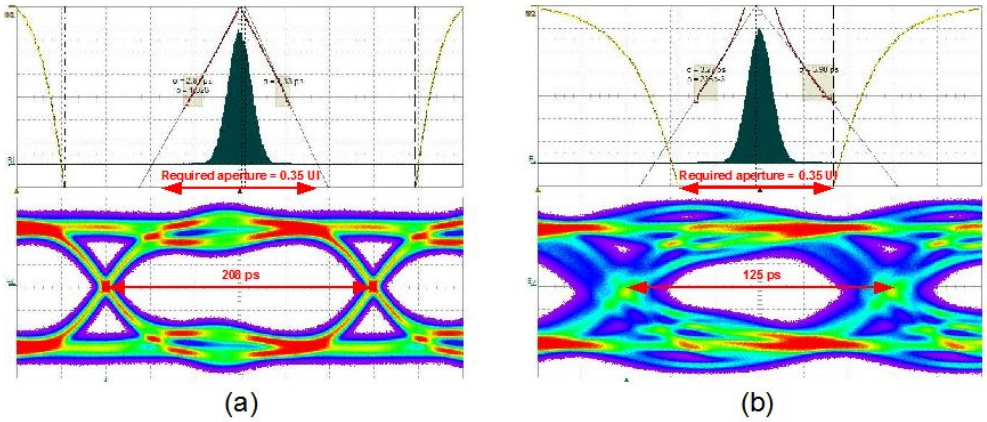

Figure 4. Jitter measurements at 4.8 Gbits (a) and 8 Gbits/s (b).

Table 1. : Number of transactions per second through Ethernet.

Packet size	Nb of transactions/s	Nb of tranfered bytes/s
1	943	1886
500	767	767000
1000	647	1294000
1458	568	1656288

The number of transactions decreases when the number of words increase, meaning that it will be more interesting to read or write a block of data. The overall performance is sufficient for controlling all the registers of a FPGA, but certainly not to control all the front-end electronics that can be attached to a single FPGA in a read-out board. Hardware acceleration is required to improve the performance, or maybe interface the GBT directly to a hardware Gigabit Ethernet IP interface. The advantage of mapping the slow control over a Gigabit Ethernet interface is that we can benefit of the embedded Gigabit Ethernet switch structure present in the xTCA specification.

5 Scalable read-out architectures

The proposed xTCA architecture is by nature scalable. It is possible to build a cheap *mini-readout* system with a couple of cards inserted in a *picoTCA* crate at a very low cost. The interest for the designers of Front-end electronics is to dispose very quickly of a system able to distribute a system clock, to provide a slow control interface and emulating the read-out functionality. The same AMC boards mounted on ATCA boards allow building the full scale system. These cards will serve as a pure data acquisition boards, as shown in figure 5, as well as a timing, fast control and slow control distribution, depending on the type of optical mezzanine used.

Conclusion. Operational serial links at 8 Gbits/s shows good performance without activating pre-emphasis and equalization. We still have margin to increase the speed of the links at 10 Gbits/s. Further measurements are ongoing to better understand signal integrity issues.

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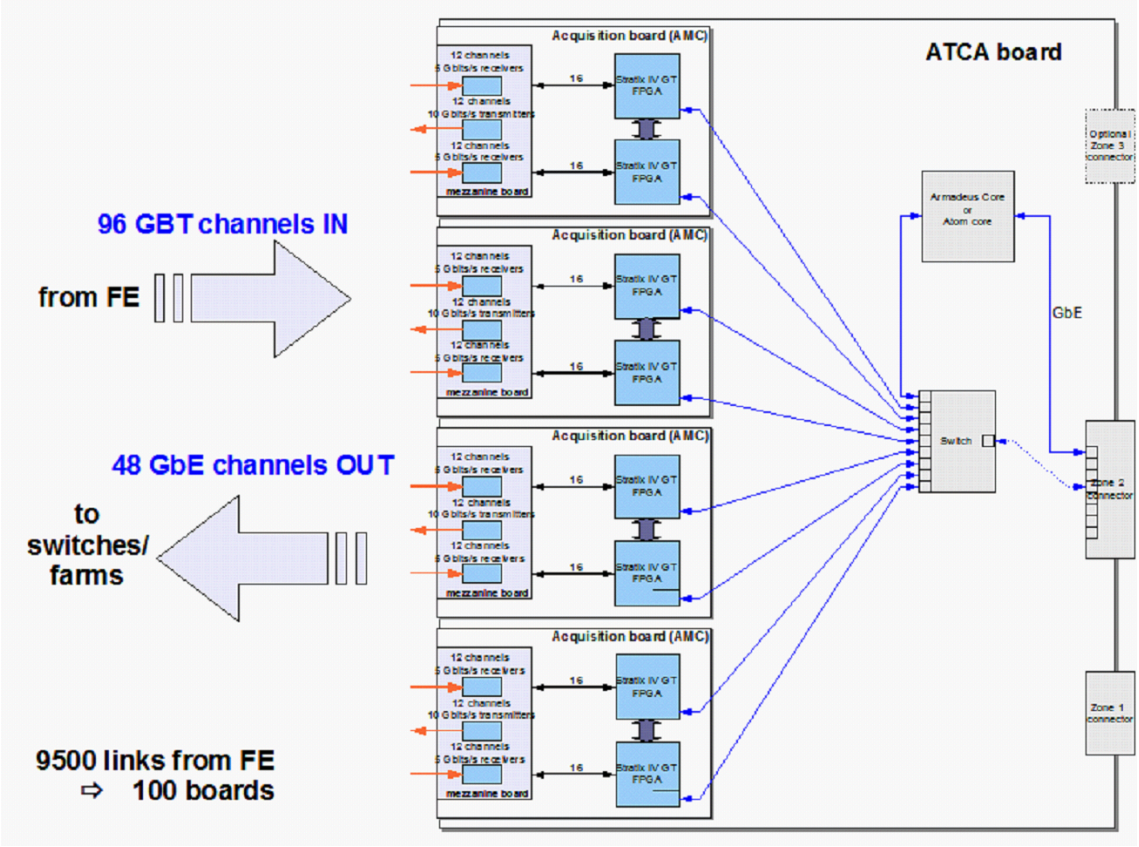

Figure 5. AMC cards mounted on larger ATCA card for data acquisition.

The xTCA architecture looks appropriate for achieving the full read-out functionality. At the same time, it is flexible enough to build cheap small test systems. Building the read-out over this standard can benefit also of the works of the *xTCA standard for Physics committee*.

The *optical mezzanine concept* allows building generic processing boards. This is a means to use the most recent optical devices without redesigning the boards. There is no specific signal integrity issue observed when passing high speed signals through the mezzanine connector.

At last, supervision system over NIOS cores embedded in FPGA looks promising even if performance needs to be improved for controlling the Front-end electronics.

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