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LVDS tester: a systematic test of cable signal transmission at the ALICE experiment

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ABSTRACT: In the ALICE experiment, the Low-Voltage Differential Signalling (LVDS) format is used for the transmission of trigger inputs from the detectors to the Central Trigger Processor (CTP), the L0 trigger outputs from Local Trigger Units (LTU) boards back to the detectors and the BUSY inputs from the sub-detectors to the CTP. ALICE has designed a set-up, called the LVDS transmission tester, that aims to measure various transmission quality parameters and the bit-error rate (BER) for long period runs in an automatic way. In this paper, this method is described and the conclusions from these tests for the ALICE LVDS cables are discussed.

KEYWORDS: Trigger concepts and systems (hardware and software); Trigger algorithms

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2010 JINST 5 C12041

Contents

1 Motivation **1**

2 Implementation **1**
2.1 Preparations for measurement 3

3 Bit-error rate (BER) measurements **3**

4 Uncertainties on the BER measurements **4**

5 Summary and conclusions **5**

2010 JINST 5 C12041

1 Motivation

The LVDS standard [1] sets the cable length to be 10 metres, while most of the ALICE trigger connections are in the maximum range of up to 60 metres. This could lead to distortions due to the longer cable length. Fortunately, it has been demonstrated that for a typical LHC transmission rate of 40 Mbit/s, transmission distortions can be successfully compensated with passive filters known as impedance equalisers [2]. It was found that signal transmission based on the LVDS provides a good signal integrity over distances of 100 metres and above, using passive filters [3–5]. Despite these promising results, a more systematic test was needed to verify the quality of signal transmission for ALICE applications. For this purpose, a set-up called the LVDS transmission tester was designed. These tests were carried out in the CTP Lab at CERN, Geneva.

2 Implementation

The implementation of the LVDS tester was carried out by modifying the standard ALICE Local Trigger Unit (LTU, see [6, 7]) using a different Field-Programmable Gate Array (FPGA) firmware configuration. It turned out that the ALICE LTU contains all the required elements needed to perform transmission bit-error rate measurements. Hence, the LVDS tester configuration re-uses several applications of the LTU such as control and monitoring functions (see [2, 8]).

The LVDS tester generates data patterns which it then propagates through the measured cable loop. The pattern output is simultaneously connected to three L0 connectors (as used for the LTU front panel) and each of them is driven by a differential driver. The instrument provides two identical channels that can be connected at the same time. A cable with no transmission problems can be connected in one of the channels to provide a measurement reference for another cable where errors in the signal transmission are expected to occur.

The principle of this device is shown in figure 1. The description of this diagram will be given for one channel only, say *cable 1* input, as the other channel works in the same way. The first

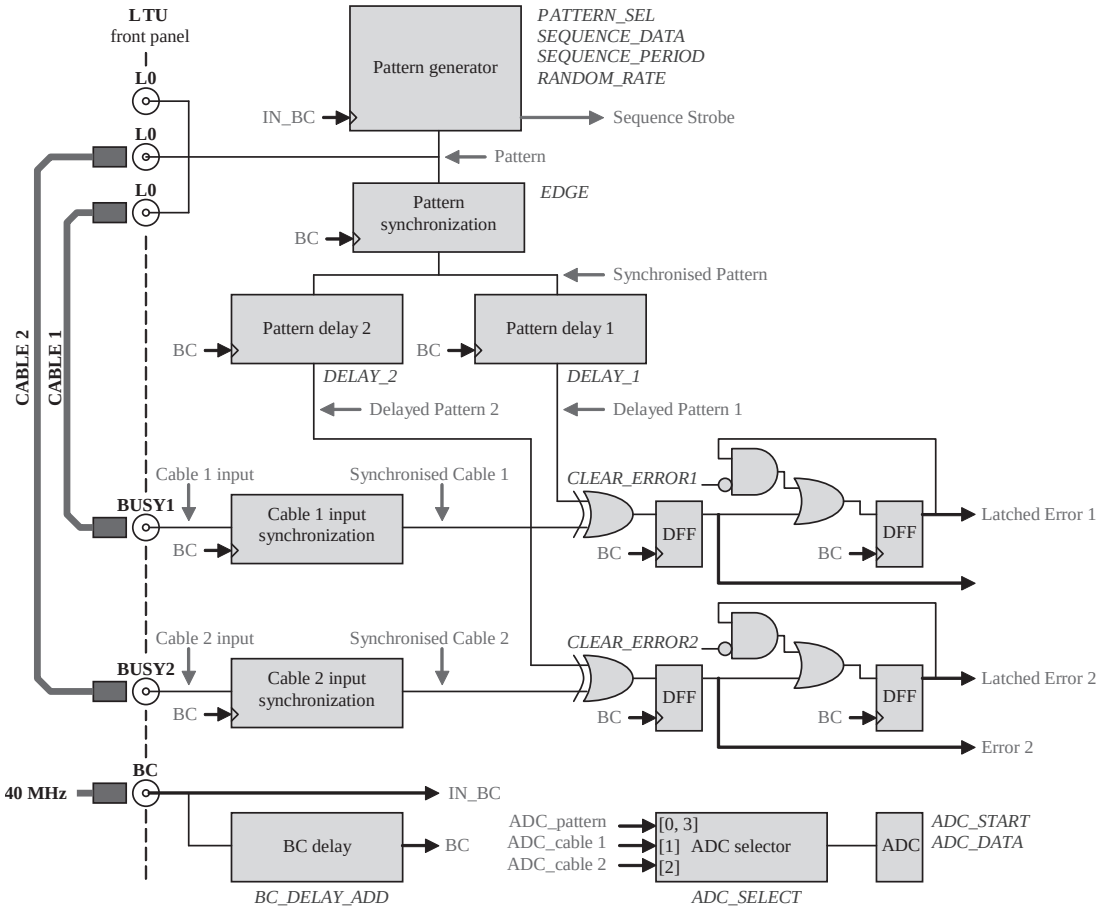

Figure 1. Block diagram of the LVDS tester.

block shown in this figure corresponds to the *pattern generator*, which can generate the following output patterns:

- A sequence of a 24-bit programmable data stream transmitted repeatedly at a programmable rate;
- A random signal of programmable rate. The pulse distribution is pseudo-random as the pattern repeats itself approximately every 53 s ($2^{31} - 1$ clock cycle or bunch crossing); and
- A toggling output (the bunch-crossing clock divided by two) that is required for phase measurements. The toggling is a waveform of 25 ns on and 25 ns off.

In order to activate the *pattern generator* block, the 40 MHz bunch-crossing (BC) clock is used. In figure 1 this is represented by *IN_BC*. The LVDS tester delays the *IN_BC* signal by changing the *BC_DELAY_ADD* "word" as shown in figure 1. This delayed signal is called BC delay.

The LVDS transmission tester also borrows all the elements used for the synchronisation of trigger inputs (see [9]) in order to synchronise the pattern output that it generates relative to its BC

2010 JINST 5 C12041

clock. In order to evaluate the quality of the pattern transmission, the *synchronised pattern* signal needs to be aligned in time with the *synchronised cable* input. Such an "alignment" procedure is achieved by delaying the *synchronised pattern* by a number of BC intervals (25 ns), as shown in figure 1.

In each BC clock interval, the transmitted *delayed pattern 1* is compared with the received pattern signal called *synchronised cable 1*. If their states are not the same, the corresponding error signal is asserted as shown in figure 1.

2.1 Preparations for measurement

The standard measurement carried out by the LVDS tester can be divided into three steps.

- *Step 1:* The synchronisation between the generated pattern and the BC clock is performed. It determines the BC delay at which the transition of the *synchronised pattern* occurs in the ADC measurement (arbitrary units) versus the BC delay. The value obtained from this measurement is called T_p and is used for the determination of the BC edge in step 3. The delay region given by $T_p \pm 3$ ns must be avoided in the final settings as it is where the set-up and hold time requirements can be violated.

- *Step 2:* The synchronisation between the *cable input* signal and the BC clock is performed. It determines the BC delay at which the transition of the *synchronised cable* signal occurs. The parameter obtained from this measurement depends upon the length of the used cable, and is called T_c. The value that is likely to return the least number of errors is called T_s and it is given by $T_s = T_c \pm 12$ ns, where the sign depends upon the shape of the phase measurement obtained from this measurement (see [9]).

- *Step 3:* The "alignment" between the *synchronised pattern* and the *synchronised cable* input is performed. The value T_s is set to be the BC delay (*BC_DELAY_ADD* word), and the edge of the BC clock is also taking into account. If T_s is inside the $T_p \pm 3$ ns interval, the *delayed pattern* is first sampled with the negative edge of the BC clock, otherwise it is sampled with the positive one; this is called the *edge rule*. The number of errors for the entire pattern delay (*DELAY_1*) of 0 to 31 BC is obtained. For each BC delay, the *edge rule* is applied. The value obtained from this measurement is called D, and it is the only delay of the *delayed pattern* at which the number of errors is zero. If there is not any delay value that returns no errors, the point with the smallest number of errors is selected by the LVDS tester software.

3 Bit-error rate (BER) measurements

Table 1 shows "transmission quality parameters" (T_c,T_s, and D) obtained by the LVDS tester for ten different cable length (5 to 60 metres). The T_p value was also obtained by the LVDS tester but, as it does not depends on the used cable, its value is always 17 ns as described in [8]. This table shows that for all the cable length tested an exact value for D was found, i.e. a BC delay when the *delayed pattern* does not give any errors. These measurements were obtained selecting the pseudo-random pattern in step 1 of the measurement procedure described in section 2.1. For a measurement that lasted about half an hour, these values are within the 10^9 level of accuracy (see below).

2010 JINST 5 C12041

Table 1. Measurement of the "transmission quality parameters" (T_c,T_s, and D) as performed by the LVDS tester for different cable length.

Cable length (m)	T_c (ns)	T_s (ns)	D (BC)
5	23	11	1
10	19	7	2
15	17	5	3
20	12	0	4
25	11	23	5
30	7	19	5
40	26	14	7
45	25	13	8
50	21	9	9
60	15	3	11

For a "realistic" bit-error rate (BER) measurement, the pseudo-random pattern should be selected in the step 1 of the measurement procedure. As mentioned earlier, the pseudo-random pattern repeats itself approximately every 53 s, which means that in order to test all the possible patterns, the error counting described in step 3 should take place during a time period of that length or multiple of it. Hence, with the clock frequency given by 40 MHz, there are approximately 2×10^9 bit transfers during the 53 s interval. This means that if N errors were counted, the corresponding bit-error rate will be approximately N divided by 2×10^9. Because the BC delay line has 31 steps, it would take approximately half an hour to complete the BER measurement for a given cable.

Notice that a measurement performed in such a way will corresponds to a "realistic" measurement because according to an accepted *rule of thumb* [2], if no error is detected at that level, the data link under test is considered reliable as the pseudo-random pattern will cover all the possible sequences that can occur. However, various tests were also carried out for a period of about 7 hours (BER at the standard 10^{12} level of accuracy) also concluding with the presence of no errors.

4 Uncertainties on the BER measurements

In the measurement procedure described in previous sections, the "alignment" between the *synchronised pattern* and the *synchronised cable* input was performed by setting the BC delay (*BC_DELAY_ADD*) equal to T_s. Sampling the BC clock at T_s should give the least number of transmission errors for a given cable as described in section [2]. However, one is likely to check the operation of the LVDS link at a set sampling point (BC delay) which is non-optimal and may violate the set-up and hold time requirements.[1]

Therefore, in addition to the step 3 described in section 2.1, the calculation of the "uncertainties" of the BER for a given cable requires another measurement to determine the so-called "sampling window" determination where a complete scan of the BC delay (*BC_DELAY_ADD*) is

[1]The worst possible working margin setting occurs at $T_c = \pm$ 6.25 ns (see appendix B in [8]) as it is left after the CTP trigger input synchronisation procedure.

2010 JINST 5 C12041

carried out. As before, the LVDS tester needs to carry out such a measurement in an automatic way, and this means the introduction of an addition "timing logic" table that deals with the automatic selection of the appropriate T_s parameter and the *DELAY_1* settings during the entire delay scan of the *BC_DELAY_ADD* word. This additional implementation turned out to be rather complicated and its technical details can be found in [2]. Essentially, the method to achieve this measurement consists on setting the *delayed pattern* (*DELAY_1*) to D $\pm$ 1 according to the different values of the BC delay (*BC_DELAY_ADD*) and observing the *edge rule*.

Contrary to what occurs in a standard measurement (i.e. when the BC delay is set to the T_s value), in the measurement of the BER uncertainties ("sampling window" determination) what matters is not the number of errors found but instead the number of consecutive BC delay bins with no error recorded; this number is called the *window* of the measurement, and for a good quality connection it should be 18 or higher as described in [2].

Figure 2 shows the "uncertainties" of the BER measurement for a 60 m LVDS cable for about 2×10^9 bit transfers. As found in the BER measurement, the delay at 15 ns (i.e. T_c) is the value with the largest number of errors. A Gaussian fit was performed to illustrate that error occurs around T_c. At the T_s value (3 ns as shown by the arrow in this plot), no error was found. This was also so between 0 to 11 ns, and between 20 to 31 ns in the BC delay line. Because the BC period is of 25 ns, this figure shows that there are only $T_s \pm 8$ ns BC delay bins with no errors in a 60 m cable, i.e. a window of 17 was obtained.

Furthermore, a systematic test was carried out for various cable lengths in a similar way to that described above for the 60 m cable. These measurements concluded that for cables larger or equal than 60 m, impedance equalisers must be used to correct their signal transmission; i.e. the *sampling window* of these measurements was found to be larger than 18.

5 Summary and conclusions

The LVDS tester measurements confirm the high quality of the ALICE standard LVDS cables. The tests have demonstrated the error-free transmission rate over the cable length of up to 60 m when the BC delay is set to its ideal value. Notice that these results were obtained even without an impedance equaliser circuit. The BER rate obtained for a cable length between 5 to 60 m is less than 1.5×10^{-12} using a 95% Poisson confidence level (upper limit).

A more sophisticated timing implementation was also developed in order to determine the "uncertainties" measurement of the obtained BER values (called "sampling window" determination). These measurements concluded that for LVDS cables longer than 60 metres, an impedance equaliser must be used in order to correct the error rate of the signal transmission. The LVDS tester has allowed ALICE to prepare the development, testing and correct tuning of the impedance equaliser circuit.

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2010 JINST 5 C12041

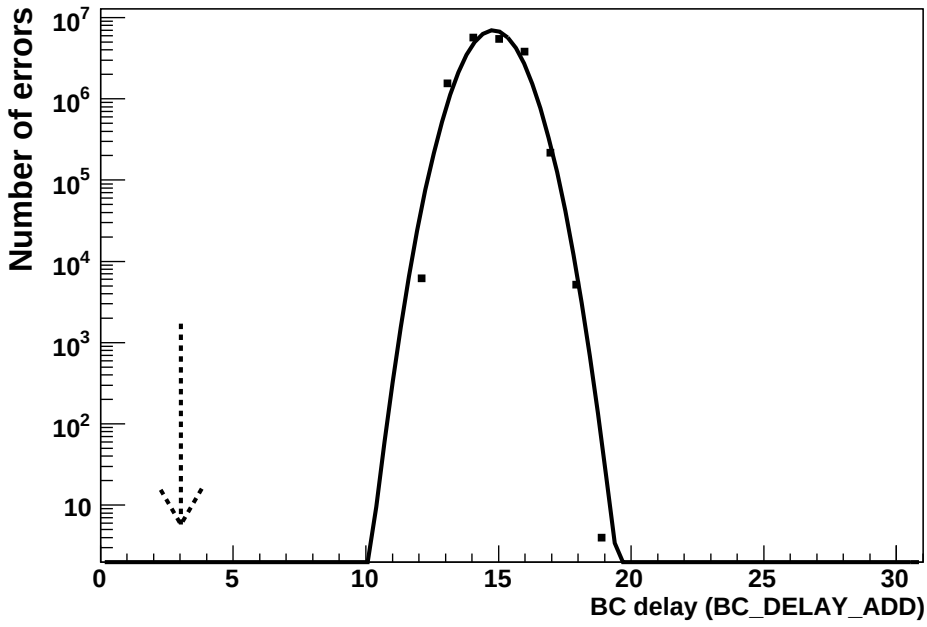

Figure 2. Error counting of the *delayed pattern* for the entire BC delay (*BC_DELAY_ADD*) called "sampling window", for a LVDS cable 60 m long. It shows the total recorded error for each consecutive BC delay bin. The arrow indicates that no error is found around T_s (see text for more details).

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2010 JINST 5 C12041