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ATLAS

Insertable B-Layer

Technical Design Report

TDR

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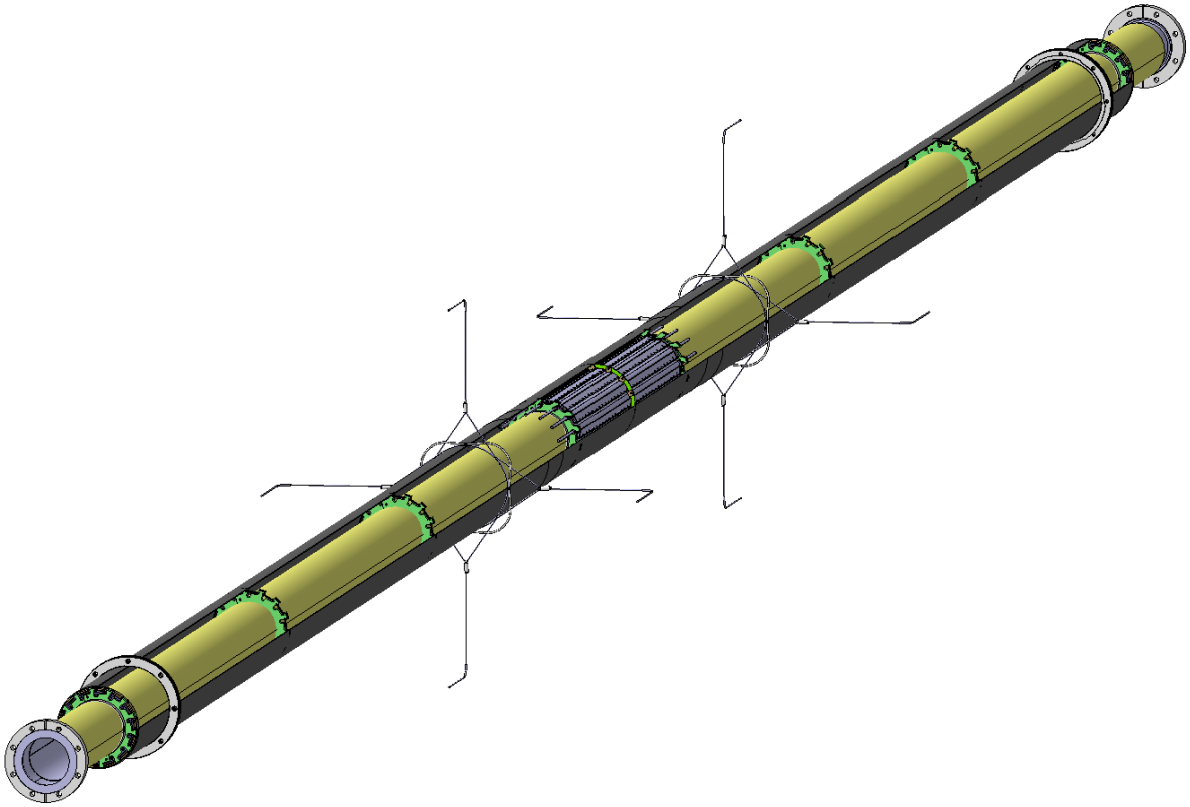

Technical Design Report

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ATLAS Insertable B-Layer Technical Design Report

ATLAS Collaboration

ABSTRACT: The ATLAS IBL detector activities are described in this paper.

KEYWORDS: ATLAS, LHC, sLHC, Upgrade, Pixel Detector, Insertable *B*-Layer, IBL, CERN.

Contents

Introduction

The Insertable B-Layer (IBL) is a fourth layer added to the present Pixel detector between a new beam pipe and the current inner Pixel layer (B-layer). The principal motivations of the project are:

1. Tracking robustness: Irreparable failures of modules in the B-layer, and in other Pixel layers, will appear with time. Although inefficiencies in the other layers can be partially compensated during reconstruction at the cost of an increased fake rate, a loss of data in the B-layer seriously deteriorates the impact parameter resolution, directly affecting the b tagging. The IBL restores the full b tagging efficiency even in case of a complete B-layer failure.

2. Luminosity effects: The current Pixel detector was designed for a peak luminosity of $1 \times 10^{34}\ cm^{-2}s^{-1}$. A luminosity at least twice that high is expected before the High Luminosity LHC (HL-LHC) is complete after 2020. With high luminosity the event pileup is increased, leading to high occupancy that can induce readout inefficiencies. Readout inefficiencies, particularly at higher luminosity, will affect the B-layer more than other layers and would thereby limit the b tagging efficiency. The presence of event pileup requires redundancy in the measurement of tracks in order to control the fake rate arising from random combinations of clusters in events with high pileup background. The addition of the IBL layer, with comparably low occupancy, helps to preserve tracking performance in face of luminosity effects.

3. Tracking precision: The IBL located close to the interaction point improves the quality of impact parameter reconstruction for tracks, and thereby improves vertexing and b tagging performance. As a result, sensitivity for signals in physics channels involving b jets is improved, for instance for a low mass Standard Model Higgs in the channel $WH \rightarrow b\bar{b}$.

4. Beam pipe replacement: Presently it would be very difficult to replace the central section of the LHC beam pipe in case of a vacuum failure. The present beryllium beam pipe was inserted into the Pixel Detector during its integration and installed together with the detector. This operation must be reversed in order to replace the beam pipe if mechanical problems appear with the pipe itself (*e.g.*, cracks, fatigue). *In situ* extraction of the beam pipe, including planning and all needed tooling, is considered part of the IBL project. The extraction process and tooling is being studied in great detail by testing the operation on an installation mock-up. Once the IBL is inserted, a smaller radius beam pipe is required, which can continue to be used for the HL-LHC upgrade unless an even smaller radius beam pipe becomes possible then.

5. Large radiation doses: As a result of current expectations for the evolution of the LHC luminosity profile, accumulated radiation dose is presently considered less of an issue than it was at the time that the Pixel detector was conceived, or later, in 2002, when the replacement of the B-layer became part of ATLAS planning and was put into the M&O budget. With the present prediction of integrated luminosity over the next five years, the dose that will be accumulated by the innermost Pixel layer will not represent a serious concern for its

efficiency. Nevertheless, other radiation-induced problems might appear (*e.g.*, large doses locally deposited as consequence of a beam loss) and should be considered in planning.

Strong constraints and project specifications have a substantial impact on the technologies required for the IBL:

1. The smaller radius of the IBL requires development of a more radiation hard technology for sensors and electronics.

2. The small radius between the new beam pipe and the existing Pixel detector does not allow for tilting of modules in the longitudinal direction (along the beam). Sensors with either an active edge or a slim guard ring must therefore be developed to reduce geometrical inefficiencies. Full coverage in phi is possible by constructing modules with the same active width, but with only one row of front-end chips. The new front-end chip has five times the area of the chip in the existing pixel detector and covers an active area that is 90% of the sensor. (The active fraction of the present pixel modules is 75%.)

3. Minimizing material is very important in the optimization of tracking and vertexing performance. The IBL radiation length will represent just 60% of the present Pixel *B*-layer. Low radiation length is achieved by considering more aggressive technology solutions, in addition to new module design, technologies such as: local support structures (staves) made of low density carbon foams; CO_2 evaporative cooling, which is more efficient in term of mass flow and pipe size; and electrical power services using aluminum conductors.

4. In general, on the mechanical side one expects tight tolerances and clearances, which require a re-design of supports and services and a complex engineering process to design the tooling required for the removal of the present beam pipe and the insertion of the new detector.

In addition to serving ATLAS until the HL-LHC upgrade in 2020, the IBL project will develop technologies and valuable experience for the subsequent high luminosity era.

The IBL schedule is a compromise between the drive to have the IBL ready as soon as possible, in order to benefit from its potential to anticipate and recover possible irreparable failures of the existing *B*-layer (and of the Pixel detector more generally), and the time demanded for the substantial technology developments and qualification tests required. The IBL is scheduled for installation early in 2015 in case of beam pipe failure or an unexpectedly large failure rate of the current Pixel detectors. In the absence of such problems, it will be installed in the long LHC shutdown foreseen for 2016.

Resources for the IBL appear to be available within the ATLAS collaboration. An Interim Memorandum of Understanding (iMoU) is in the process of being signed by the institutions who will commit to IBL construction. A final MoU will be signed following selection of the sensor technology, foreseen for 2011, and when the required resources become available. The total project cost, including the new beam pipe and installation, is 9.7 MCHF.

1. The IBL Detector within ATLAS during LHC Phase I

The ATLAS Inner Detector (ID) [1] provides charged particle tracking with high efficiency over the pseudorapidity range of $|\eta| < 2.5$. The Pixel detector [2], shown in Fig. 1, is the innermost part of the ID. It has approximatively 80 million channels: 67 million in its 3 cylindrical, barrel layers and 13 million in its 3 forward and backward endcap disk layers. The main parameters of the Pixel detector are given in Table 1.

The performance of the innermost layer (*B*-layer) of the Pixel detector is critical to the full realization of the physics capabilities of the ATLAS experiment. This performance must be maintained to ensure good vertexing and *b* tagging for the LHC Phase I upgrade physics program, despite increased event pileup and eventual problems in the present *B*-layer and other Pixel layers. Exploiting new technology, an additional layer inside the *B*-layer, the Insertable *B*-Layer (IBL), will maintain robust tracking despite effects arising from luminosity, hardware lifetime, and radiation. The IBL will also provide improved precision for vertexing and tagging. (Chapter 2 gives the results of a systematic study of the tracking performance with IBL). Installing the IBL in the 2016 LHC shutdown, the last shutdown preceding HL-LHC phase, will provide improved tracking and robustness before the LHC exceeds nominal peak luminosity and before the large LHC Phase I data set is collected.

Although regular replacement of the *B*-layer was foreseen by the original mechanical design for radiation reasons, engineering changes demanded by the exigencies of the overall ATLAS schedule led to a final design that does not permit *in situ* extraction of the *B*-layer from the rest of the Pixel detector. In 2008, an ATLAS task force defining the scenario for the first *B*-layer re-

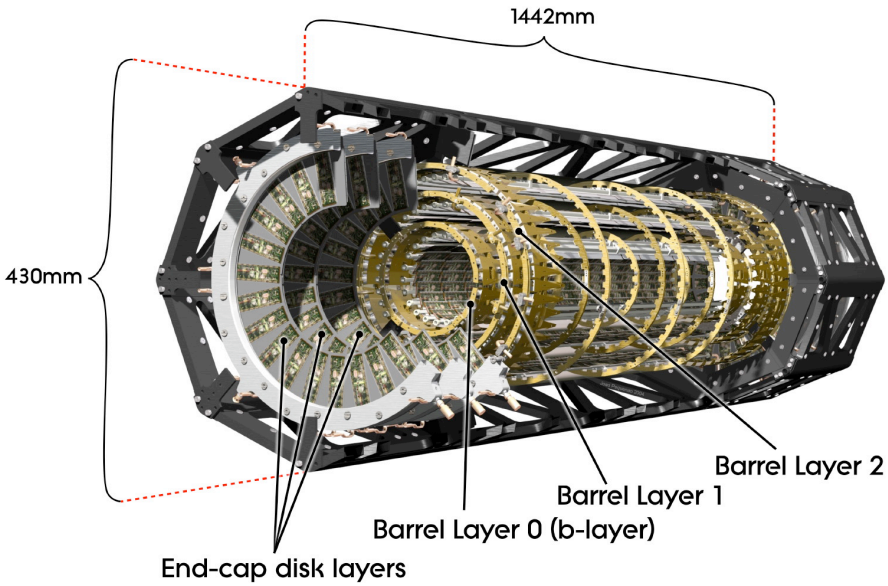


Figure 1. Schematic view of the active region of the Pixel detector consisting of barrel and endcap layers.

placement, including replacement of the section of beam pipe inside the detector, recommended, instead of replacement, insertion of a new innermost, fourth pixel layer with a smaller beam pipe as the best and only viable solution [3]. This recommendation formed the basis of the new Insertable *B*-Layer project described in this Technical Design Report (TDR). (Appendix A contains a short history of the changes of the Pixel layout, from the Pixel TDR to the constructed version, and of the B-Layer Task Force that resulted in the present technical solution.)

The LHC schedule and the environment for operating the IBL, including luminosity profile and radiation doses, are outlined in Section 1.1. Operation of the current Pixel detector, including limitations, are presented in Section 1.2. The impact of the IBL on ATLAS physics performance, for different scenarios of LHC luminosity and of behaviour for the present Pixel detector, is discussed in Chapter 2. The technical details of the IBL are described in Chapters 3 to 10.

1.1 The LHC Schedule and the Machine Environment for Operating the IBL

CERN has defined three future major LHC shutdowns for consolidation work and upgrades [4]. The first shutdown, in 2012, will focus on work on the superconducting magnet systems in order to enable operation at full design energy. The second and third shutdowns, in 2016 and 2020 respectively, will upgrade the accelerator system to enable operation at luminosity higher than "nominal". The running period between these two shutdowns is referred to as LHC Phase I. The IBL will be installed during the 2016 shutdown and will be active until the complete replacement of the ATLAS inner tracker, which will happen in the long shutdown of 2020 in preparation for the subsequent Phase, referred to as the High Luminosity LHC (HL-LHC).

The peak luminosity during LHC Phase I is expected to be approximately 2.2×10^{34} cm^{-2}s^{-1}. The total luminosities integrated before and during Phase I are difficult to forecast; however, predictions are around 35 fb^{-1} before the 2016 shutdown and 340 fb^{-1} at the end of the Phase I [4].

Item		**Radial Extension** [mm]	**Length** [mm]	**Staves / Sectors**	**Modules**	**Pixels** ($\times 10^6$)
Beam pipe (today)		$29 < R < 36$				
Beam pipe (with IBL)		$25 < R < 29$				
IBL	Envelope	$31.0 < R < 40.0$				
	Sensitive	$< R > = 25.7$	$\|Z\| < 332$	14	224	6.02
Pixel	Envelope	$45.5 < R < 241.0$	$\|Z\| < 3092$			
B-layer	Sensitive	$< R > = 50.5$	$\|Z\| < 400.5$	22	286	13.2
Layer 1	Sensitive	$< R > = 88.5$	$\|Z\| < 400.5$	38	494	22.8
Layer 2	Sensitive	$< R > = 122.5$	$\|Z\| < 400.5$	52	676	31.2
Disk 1	Sensitive	$88.8 < R < 149.6 = 88.5$	$< Z > = 495$	8×2	48×2	4.4
Disk 1	Sensitive	$88.8 < R < 149.6 = 88.5$	$< Z > = 580$	8×2	48×2	4.4
Disk 1	Sensitive	$88.8 < R < 149.6 = 88.5$	$< Z > = 650$	8×2	48×2	4.4
					Pixel Total	*80.4*

Table 1. Main parameters of the Pixel detector system including the foreseen IBL.

1.1.1 LHC machine backgrounds and radiation environment during LHC Phase I

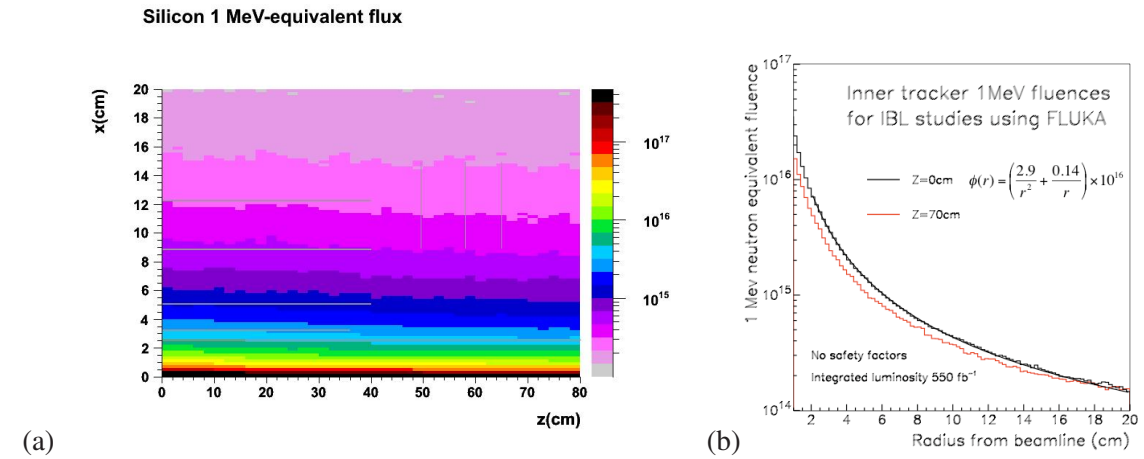
The design requirements for IBL have assumed an integrated luminosity of 550 fb^{-1} and a peak luminosity of 3×10^{34} cm^{-2}s^{-1} to evaluate the readout parameters. Recent LHC plans have reduced the expectations, but different evolution scenarios could happen in the years to come; keeping a larger safety factor has been considered appropriate. Furthermore, some developments for the IBL are considered to be used for the Pixel system at HL-LHC. The design specifications for IBL apply to that phase for a minimum radius of about 8 cm for the full life of the machine or for shorter time at a smaller radius (replaceable *B*-layer).

The requirements of radiation dose for the IBL have been studied simulating the fluences at IBL position from operation of LHC. In an older simulation made for Radiation Task Force [5], ID fluences for LHC operation were obtained using FLUKA for 2 cm radial binning. This is too coarse for *B*-layer studies so the simulations were repeated for 2 mm radial binning with an updated Pixel layout. In the simulations only a simple silicon cylindrical representation of the IBL has been implemented. This should still produce a reasonable estimate of IBL fluences and doses, though in longer term a more detailed geometry implementation, including services, should be considered.

Radiation background close to the interaction point is dominated by particles from pp collisions. Beyond a radius of 10 cm or so, albedo neutrons back-splashing from the calorimeters become important. Figure 2 shows simulation results obtained using the PHOJET pp event generator and FLUKA 2008 particle transport code.

Figure 2 (b) includes a simple parameterisation of the data for the case $z = 0$, obtained from a fit to the data for 2 cm $< r <$ 20 cm. The small z dependence suggests the $z = 0$ parameterization is useful for providing fluence estimates over the full Pixel region. The fluences are normalised to 550 fb^{-1}. For the case of $r = 3.1$ cm (minimum radius of the IBL sensors), the 1 MeV neutron fluence is estimated to be 3.3×10^{15} n$_{eq}$/cm^2.

The average dose in a 500 μm thick silicon cylinder of inner radius 3.2 cm from the beam line



(a) (b)

Figure 2. (a) 1 *MeV* neutron equivalent silicon damage fluences normalised to an integrated luminosity of 550 fb^{-1} and (b) corresponding 1 MeV neutron fluences versus radius r from beamline, for the cases of $z = 0$ and $z = 70$ *cm*.

is predicted to be 1.6 MGy (160 Mrad) for 550 fb^{-1}.

There are two main sources of systematic uncertainties:

- The proton-proton non-elastic cross section. At LHC energies event generator predictions differ by some 30%.
- The conversion of particle fluences into 1 MeV neutron fluences. Assumed in the Radiation Task Force Report is an uncertainty of 50% for the silicon damage factors used to convert the pion, proton and neutron fluences into 1 MeV neutron fluences.

There is no formal procedure for combining these uncertainties into safety factors. For IBL we chose to design for 5×10^{15} 1 MeV fluences, which corresponds to a 60% safety factor at $r =$ 3.2 cm, and 250 Mrad.

The peak luminosity does not affect the sensor design, but it affects the readout electronics from the front-end chip to the off-detector electronics. The FE-I4 front-end chip has a completely new internal architecture that fulfils the larger request of occupancies and bandwidths. Chapter 3 discusses the new FE-I4 architecture, whereas Chapter 6 describes the data links and the off-detector readout electronics.

1.1.2 Irradiation effects on the present *B*-layer

At the time of the design of the present *B*-layer, technology did not enable design of a small-radius layer with sufficient radiation tolerance to withstand the gradual degradation of performance of sensors and electronics for seven years of operation at the design luminosity. Based upon extensive measurements of components and modules during the qualification phase of the Pixel Detector, the estimated lifetime limit of the present *B*-layer due to radiation effects is about 300 fb^{-1}, with onset of reduced tracking efficiency at lower integrated luminosity. At the time of design, it was envisaged that the *B*-layer would be replaced during the lifetime of the experiment and before the remainder of the Inner Detector. This subsection describes the effects of irradiation, the expected doses at 300 fb^{-1}, and test results at comparable doses (that indicate that the lifetime is not longer).

The 0.25 μm CMOS front-end chips, module controller, and optical readout are most sensitive to the direct ionizing radiation, measured in terms of total ionizing dose (TID). Charge from ionization trapped in the gate oxide changes the transistor threshold voltage (V_T), which degrades both the analog and digital behaviour of the chips. Performance of the silicon sensors is more sensitive to the displacement damage induced by radiation in the silicon bulk, measured in terms of non-ionizing energy loss (NIEL). NIEL damage for sensors is conventionally quoted as the equivalent damage of a fluence of 1 MeV neutrons (n_{eq}/cm^2). Displacement damage of silicon sensors causes an increase in sensor leakage current (I_L), which results in an increase of noise in the analog front-end and of the detector bias voltage needed for full depletion (V_D). Increased noise requires a higher discriminator threshold to maintain system stability which, in conjunction with reduced collected charge, affects the detector performance. Increased full depletion voltage also affects detector performance if charge collection is reduced because the detector bias voltage cannot be set as high as needed for full depletion. (Detector bias voltage must be operated below V_D in order to avoid thermal runaway. Thermal runaway occurs when power dissipation in the detector reaches a critical value, because temperature depends on power dissipation, which depends upon I_L, which

in turn depends exponentially on temperature.) NIEL damage also reduces the mean free path of electrons and holes in the sensors, resulting in charge trapping and the reduction of collected charge.

Simulation (FLUKA AV16) has been used to estimate the TID and NIEL at the *B*-layer for 300 fb^{-1}. The TID estimate is 47 Mrad, with $< 10\%$ statistical uncertainty and 30% uncertainty in the pp cross section at 14 TeV energy. The corresponding 1 MeV equivalent fluence is 8.0×10^{14} n_{eq}/cm^2. The 1 MeV neutron equivalent fluence has an additional 50% uncertainty arising from silicon damage factors. If the above uncertainties are conservatively added to the central estimate, the TID and NIEL values should be considered to be 66 Mrad and 1.6×10^{15} n_{eq}/cm^2.

Extensive measurements of several Pixel detector modules up to a TID of 50 Mrad and a NIEL dose of 1×10^{15} n_{eq}/cm^2 were performed during the qualification phase of the Pixel detector. Limited additional experience is available from one module accidentally irradiated to 100 Mrad. While it was still possible to operate the FE-chips on this module at higher supply voltage, degraded performance was observed. Thus, a dose of 100 Mrad can be regarded as an upper limit for the radiation tolerance of the front-end chips [3].

The effects of irradiation upon the opto-boards and optical fibers, including effects on VCSEL light output, are expected to be at an acceptable level until the HI-LHC upgrade. These components are located at the largest practical radius in order to reduce their total radiation dose. The expected total dose for 300 fb^{-1} in this region is about 10 MRad.

Although both the radiation tolerance of the present *B*-layer and the total integrated luminosity for LHC Phase I are uncertain, the integrated luminosity could approach or exceed the radiation tolerance of the *B*-layer before the end of Phase I. The IBL will mitigate the effects of radiation-induced loss of efficiency.

1.2 Operating the Present Pixel Detector during LHC Phase I

1.2.1 Pixel detector readout architecture

The Pixel detector readout architecture was designed to be fully efficient at the "nominal" LHC peak luminosity of 10^{34} cm^{-2}s^{-1}, and for a LVL1 trigger rate of 100 kHz. Two bottlenecks arise in the architecture at luminosities greater than nominal, one in the FE-I3 (front-end chip) and one in the link between the MCC (Module Controller Chip) and the off-detector electronics. These bottlenecks can give rise to readout inefficiencies that would impact *b*-tagging efficiency in the absence of the IBL. A brief description of the readout data flow is provided as background to discussion of readout inefficiencies in Sections 1.2.2 and 1.2.3. The impact of readout inefficiencies on performance is presented in Chapter 2.

The readout architecture of the existing Pixel detector modules is implemented in two separate custom integrated circuits: the FE-I3 and the MCC. Sixteen FE-I3 chips and one MCC instrument each module. When deposition of charge is detected by the discriminator, the hit and its time stamp are briefly buffered in the pixel cell and transferred to circuitry at the end of the pixel column. Hit data is held there until a Level-1 trigger (LVL1) Accept signal arrives. Only then are hits associated with that LVL1 Accept moved to the MCC and subsequently transferred off detector through optical links. All hits in the pixel cells are sequentially transferred to the FE-I3 periphery using a shared bus for all the pixels in a double-column. The transfer happens in sequence: each pixel that raises

the “hit flag”, waits for the “token” and takes control of the bus when its turn comes. Only one hit can be transferred at a time for a double column of 320 pixels. The transfer bandwidth is 20 MHz/hit. Hits are buffered at the end of FE-I3 columns. If their time stamps match the one of the LVL1 trigger, they are transmitted to the MCC; otherwise, they are cleared once LVL1 latency has passed. Transmission from the FE-I3 is with fixed length packets (26 bits/hit) through 40 Mb/s serial links. Transfer happens in parallel for all 16 FE-I3 chips in a module. The MCC buffers all the data it gets from FE-I3s in "receiver" FIFOs. When an event is complete in the MCC, it is formatted and transmitted off-detector. The physical bandwidth from the MCC is 160 Mb/s for the *B*-layer (2 links at 80 Mb/s), 80 Mb/s for Layer-1 (1 link at 80 Mb/s) and 40 Mb/s Layer-2 and disks (1 link running at 40 Mb/s).

There are two critical bottlenecks in the system: the double-column bus in the FE-I3 and the link from MCC off detector. The first is sensitive to the pixel occupancy, which scales with the LHC luminosity. The second one is sensitive to the product of the hit occupancy and LVL1 rate.

1.2.2 Readout induced inefficiency due to Pixel detector occupancy

The readout inefficiency of the FE-I3 induced by pixel hit occupancy has been studied via a time-driven simulation of the FE-I3 architecture, with physics-generated events as input [6]. The inefficiency is plotted as a function of the FE-I3 double-column occupancy per bunch crossing in Fig. 3. The total inefficiency is shown by the solid black curve, which displays a very steep increase of the overall inefficiency at a certain threshold in occupancy.

The anticipated double-column occupancy as a function of luminosity is determined via physics simulation and corrected upwards by 20% in order to account for the observed charged particle track multiplicity in 900 GeV and 7 TeV collision data being about 20% higher than in the simulation used [7]. After correction, the estimated occupancy of the central module of the *B*-layer is 0.165 hits/DC/BC (double-column per bunch-crossing) at a luminosity of 10^{34} $\mathrm{cm}^{-2}\mathrm{s}^{-1}$. This value scales linearly with luminosities in this range.

Based upon the above simulations, the readout inefficiency arising from the FE-I3 in the *B*-layer central module is estimated to be 1.7% at 10^{34} $\mathrm{cm}^{-2}\mathrm{s}^{-1}$, 3% at twice the luminosity and 9% at three times. Considerable uncertainty, however, should be attached to these values, because of the strong dependence of the simulation upon the time structure of events.

Furthermore FE-I3 behaviour as function of occupancy has been studied in a high-intensity CERN test beam. The event structure and illumination of the FE-I3 were quite different from expected LHC conditions, but extrapolation of the measurements to LHC conditions results in more pessimistic estimates than the simulation: The estimated inefficiency is 5% for 0.27 hits/DC/BC, and 10% for 0.31 hits/DC/BC [8].

In light of the sharp threshold behaviour and these uncertainties, the overall Pixel system must have a margin of robustness against such occupancy-induced readout inefficiency. The addition of the IBL will provide the needed margin.

1.2.3 Bandwidth limits of the present Pixel detector

During LHC Phase I, at two or more times the nominal luminosity, the links between the MCC and the off-detector electronics will be bandwidth limited, causing loss of data. This loss can only

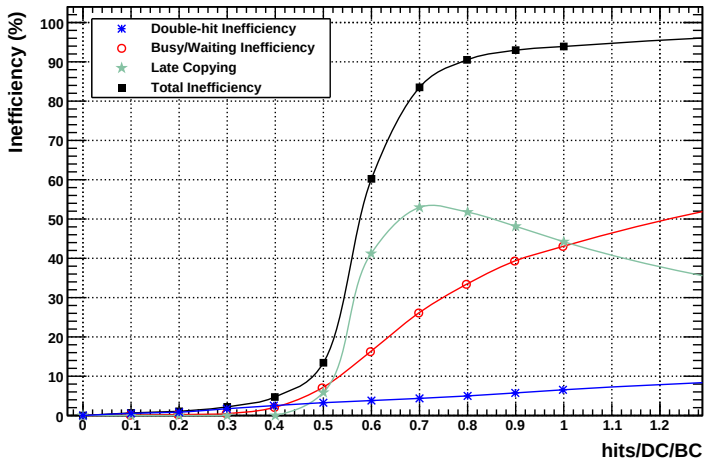


Figure 3. FE-I3 inefficiencies as function of the double-column occupancy per bunch crossing. The expected occupancy in the *B*-layer central module at 10^{34} cm^{-2}s^{-1} is 0.16 hits/DC/BC.

be avoided by reducing the trigger rate. Table 2 shows results of studies of the bandwidth limits for nominal luminosity and 100 kHz level 1 trigger rate. These studies used a simulation of the readout architecture of the MCC [9] (2002) with 23 minimum bias interactions plus *b*-jets from decay of a 120 GeV Higgs. For this study, the simulated FE-I3 front-end chip was considered "ideal", with infinite buffer size and internal bandwidth. The results in the column labeled *MCC bandwidth* show that at two or more times nominal luminosity, all Pixel layers will be vulnerable to data loss, as the usage of the MCC bandwidth becomes large. The *B*-layer is already equipped with two 80 Mb/s output links per MCC; consequently, no remedial action is possible to avoid data loss. (Note that data loss in Layer 2 could be avoided by increasing its MCC output rate to 80 Mb/s and doubling the number of ROD Bandwidth limitations at the output of the ROD lcan so be eliminated by increasing the number of RODs) The IBL is designed without this bandwidth limit, and it will provide additional hits that will substitute for lost *B*-layer hits when the *B*-layer output links saturate.

1.2.4 Status of the present Pixel detector

Irreparable failures in the Pixel detector inevitably appear over time and can impact tracking and vertexing performance. Failures can affect single channels, or they can impact larger portions of the detector, for instance entire modules or all of the modules on a failed cooling loop. Table 3 tracks the type and number of failures from installation (July 2007) to present. Failures are classified according to the affected component. Only failures within the detector volume are considered here. The five classes are, in order of size of impact:

- *Cooling loop*: a cooling loop hard failure that requires powering off a bi-stave. The two main failures that have been experienced during the integration of the current detector are corrosion of aluminum cooling pipes and leakage at the fittings. A cooling loop is considered to have a

high leak rate if, when pressurized at 4 bars with helium, its pressure drops more than 2 mbar per hour. This leak rate does not imply that the cooling circuit is powered off automatically, but it is considered problematic. Existing cooling loop leaks lead to the presence of 0.1% of C_3F_8 (cooling fluid) in the inner detector nitrogen volume.

- *Opto-board*: all modules serviced by a single opto-board not functional. In the case of a complete opto-board failure, either 6 or 7 modules cannot function properly, disabling approximately 300,000 channels. This class of failures does not include single opto-link failures, which are counted in the module class.

- *Module*: a complete module not functional. Reasons for this class of failures are missing bias on the sensor, problems with low-voltage power supply at the module level, non-functional MCC, and data/clock connection failure of a single channel Pin-diode/VCSEL (Vertical Surface Emitting Laser). A module failure disables 16 front-end chips, or 46,000 channels.

- *Front-end*: whole front-end chip not functional. The main causes of this class of failures is failure of the front-end chip or of wire-bond connections. In some cases, high power supply current prevents correct configuration. A front-end failure disables 2880 pixels.

- *Pixel*: single pixel affected. The main causes of this class of failures are disconnected bumps, electronic dead channels, and masked noisy channels. A channel is considered noisy and is masked if it has occupancy($> 10^{-5}$ hits/bunch-crossing. The number of masked noisy channels depends on the applied discriminator threshold, which has been lowered to 3000 e from the 4000 e of the initial commissioning of the detector.

The IBL project has adopted new solutions and tightened the qualification of components in response to experience gained with the present design and to analysis of failures. For instance, the IBL opto-boards will be placed on the ID endplate, which is accessible, although not easily,

Pixel System *$L = 10^{34}\ cm^{-2}s^{-1}$, LVL1 rate = 100 kHZ*	**Col. pair occ.** hits/BC	**MCC** bandwidth	**ROD** bandwidth
B-layer *160 Mb/s MCC out* *6/7 modules/ROD, 44 RODs*	0.18	47 ± 3 %	52 ± 3 %
Layer 1 / Disks *80 Mb/s MCC out* *13 modules/ROD, 38 + 24 RODs*	0.06	39 ± 3 %	35 ± 3 %
Layer 2 *40 Mb/s MCC out* *26 modules/ROD, 26 RODs*	0.04	53 ± 3 %	43 ± 3 %

Table 2. Column pair occupancies and fraction of output bandwidth used for single MCC and ROD for different Pixel subsystems. Values reported in the table have been simulated for nominal LHC luminosity of 10^{34} cm^{-2}s^{-1} and maximum design first level trigger (LVL1) rate of 100 kHz.

Affected System (failure class)	No. of parts in the system	*Number of Pixel detector Failures* Jul 2007	Dec 2008	Dec 2009	Aug 2010
Pixel	80 363 520	n/a	n/a	n/a	161 040
Front-end	27 904	3	26	37	42
Module	1 744	3	28	39	40
Opto-board	272	0	0	1	1
Cooling loop (high leak) (**)	88	0	3	3	3
Total fraction of dead pixels		0.18 %	1.70 %	2.74 %	3.01 %

Affected System (failure class)	No. of parts in the system	*B-layer Only Failures* Jul 2007	Dec 2008	Dec 2009	Aug 2010
Pixel	13 178 880	n/a	n/a	n/a	15 080
Front-end	4 576	0	8	9	9
Module	286	0	4	6	6
Opto-board	44	0	0	0	0
Cooling loop (high leak)	11	0	0	0	0
Total fraction of dead pixels		0 %	1.57 %	2.29 %	2.41 %

Table 3. Development of failures in the Pixel detector over time.

without disconnecting, extracting, and opening the full Pixel detector. Thus, the IBL will provide a more robust tracking layer while compensating for irreparable failures in the *B*-layer. The impact of Pixel detector failures on performance, with and without the IBL, is described in Chapter 2.

1.3 The IBL Layout and Strategy for Insertion into the Pixel Detector

The envelopes of the existing Pixel detector and of the beam pipe leave today a radial free space of 8.5 mm. The reduction of 4 mm in the beam pipe radius brings it to 12.5 mm, which makes possible to fit in the new IBL detector design. Figure 4 shows in (a) a picture where the empty space between the *B*-layer and the beam pipe is visible, and in (b) the rendering of the future insertion of a smaller beam pipe with the IBL.

1.3.1 Layout

The IBL layout is shown in Fig. 5. A fully hermetic coverage in ϕ for high p_T tracks is possible with 14 staves. The tilt angle in ϕ is almost fixed by the space constraints, while the sign will be the same as for the other pixel layers and it is selected to compensate (reduce) the Lorentz angle. Due to the small radius of the IBL, the angle of the sensor to the radial direction is between 0 and 27°.

It is not possible to obtain the full geometrical coverage in z as the Pixel detector does, where modules are tilted in z and are partially overlapped, because there is not enough space. However the gap between modules is minimized using a sensor design with active or slim edges. Additionally,

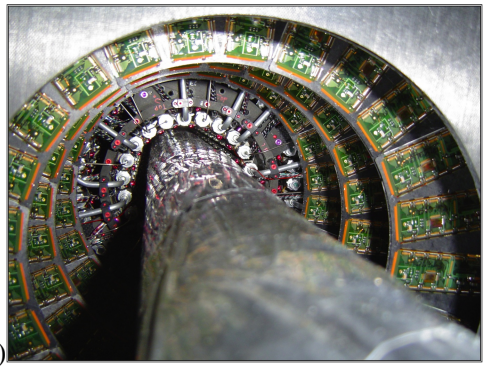
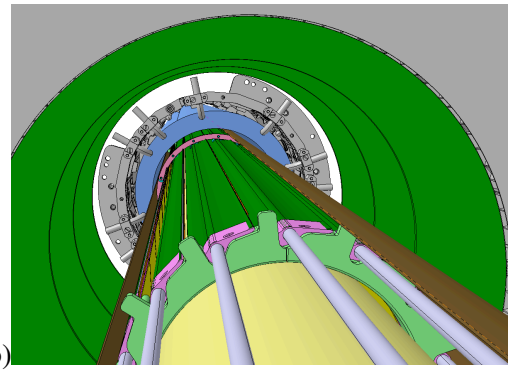
(a)  (b) 

Figure 4. (a) Photo of the Pixel detector with the inserted beam pipe during the integration in SR1 building, and (b) rendering of the insertion of the IBL with the smaller beam pipe.

a big effort is made to reduce the material budget; the goal is to almost halve the X_0 of the existing Pixel *B*-layer. Table 4 summarizes the main layout parameters.

1.3.2 Removal of existing beam pipe

Before inserting the IBL with the new beam pipe, it is necessary to extract the VI section of the current beam pipe. The VI section is a 7.3 m long pipe made in beryllium with two aluminium flanges at its extremities; they support the beam pipe together with two other intermediate support points at $\pm$ 0.85 m from $z = 0$. The intermediate supports use two collars attached to a wire

	Value	**Unit**
Number of staves	14	
Number of modules per stave (single/double FE-I4)	32 / 16	
Pixel size (ϕ, z)	50, 250	μm
Module active size W$\times$L (single/double FE-I4)	16.8$\times$40.8 / 20.4	mm^2
Coverage in η, no vertex spread	$\lvert\eta\rvert < 3.0$	
Coverage in η, 2σ (=112 mm) vertex spread	$\lvert\eta\rvert < 2.58$	
Active z extent	330.15	mm
Geometrical acceptance in z (min, max)	97.4, 98.8	%
Stave tilt angle in ϕ (center of sensor, min, max)	14.00, -0.23, 27.77	degree
Overlap in ϕ	1.82	degree
Center of the sensor radius	33.25	mm
Sensor thickness:		
Planar silicon	150 $\div$ 250	μm
3D silicon	230$\pm$15	μm
Diamond	400 $\div$ 600	μm
Radiation length at $z = 0$	1.54	% of X_0

Table 4. Main IBL layout parameters.

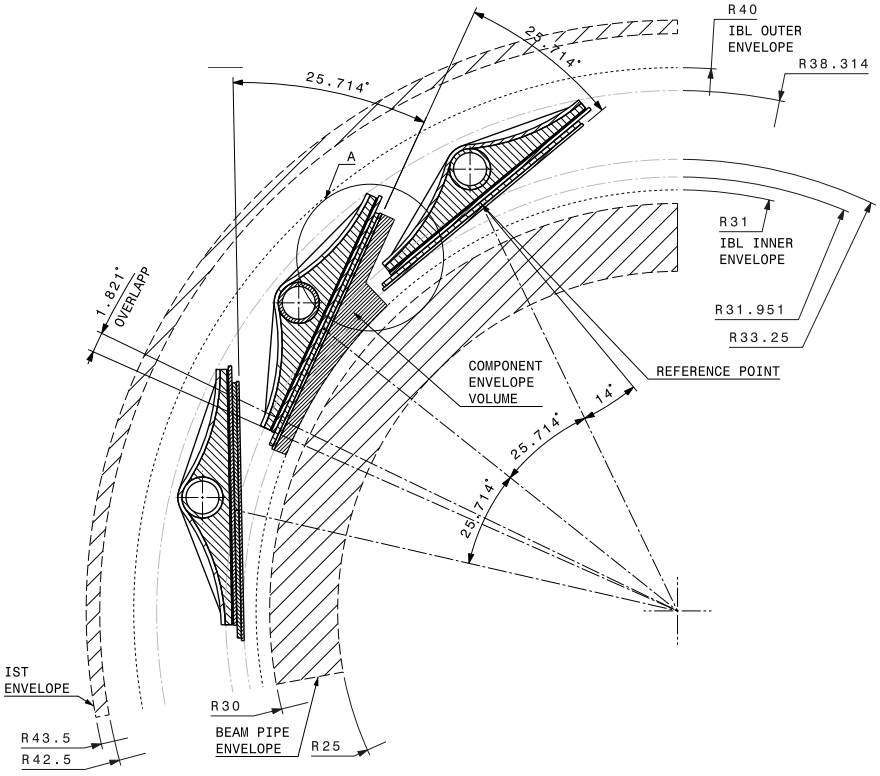


Figure 5. IBL layout: $r\phi$ view.

suspension/alignment system. There are two main critical issues to extract the beam pipe: the remote position of the collars that must be disconnected from the supporting wires and the cutting, at one extremity, of the beam pipe for removing one of the flanges; this is needed to pass through the Pixel disks. Wires have to be kept in place, because they will be used for the support of the new detectors and beam pipe. The collars need to be dismounted with remotely operated tools from outside the pixel package and the suspension wires have to be engaged and recuperated to be used for supporting the IBL. The position where the beam pipe is cut to remove the flange on C-side is made of aluminium, avoiding the toxic issue of cutting beryllium. Additional issues that have to be considered in the extraction are the control the bow of the beam pipe when it is disconnected from its supports, and the radiation issues due to activated material. Fig. 6 shows the beam pipe with its supports.

Extraction of the beam pipe and the insertion of the new detector (described in Chapter 7) are the most risky operations of the entire project and are being carefully planned. A full scale mock-up of the present inner detector is in construction to test, step by step, all the phases with final components and tooling.

1.3.3 New beam pipe concept

To make possible an IBL layout, the beam pipe needs to be reduced by 4 mm in radius (from inner radius of 29 mm to 25 mm). In the definition of the inner diameter of the existing beam pipe there

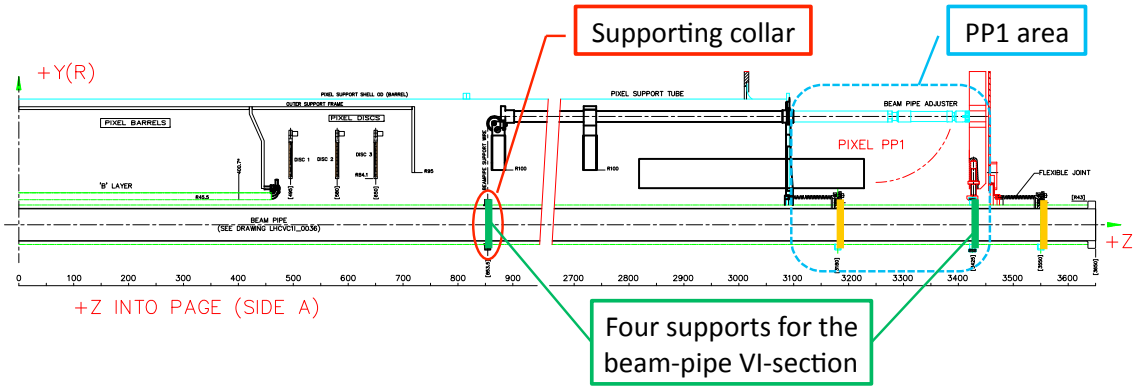


Figure 6. Drawing of the existing beam pipe showing the supports inside the Pixel detector volume.

were several tolerances taken into consideration, as shown in Table 5. One of those tolerances allowed for instability of the cavern floor. The movement has been measured and is much less than was allowed for. Figure 7 shows the survey of the ATLAS cavern made from 2003 to 2007, where the maximum displacement is of ~ 1 mm and has stabilised. Due to that stability, the related tolerance on the new beam pipe radius can be relaxed from 9.8 to 5.8 mm and consequently gain the 4 mm needed for the IBL. To make possible the insertion of the beam pipe, the new flanges must also be reduced in diameter. The new design will have "split" flanges of 58 mm diameter; the dimension is small enough to insert the beam pipe with the envelope of internal services inside the IBL Insertion Tube (IST). The new beam pipe inner diameter has been reviewed from the point of view of aperture and considered acceptable; the formal approval from the LHC machine is pending.

1.3.4 Insertion constraints for IBL

The small clearance between the envelopes of the Pixel *B*-layer and IBL together with a total IBL length larger than 7 m, strongly constrains the insertion of the new detector package. To simplify the insertion and support of the IBL with the beam pipe, an IBL Support Tube (IST) will be used in a similar way to the Pixel Support Tube (PST) of the current Pixel detector. The IST will be put

	Current Design [mm]	**IBL Design** [mm]
Beam aperture ($10\times\sigma$)	14.0	14.0
Alignment	2.6	2.6
Construction and deflection	2.6	2.6
Stability during run, and between alignments	9.8	5.8
Physical inner radius of pipe	29.0	25.0

Table 5. Beam pipe tolerances for the present design and for the IBL design. The stability of the position of the beam pipe is 4 mm better than foreseen and can be gained for IBL.

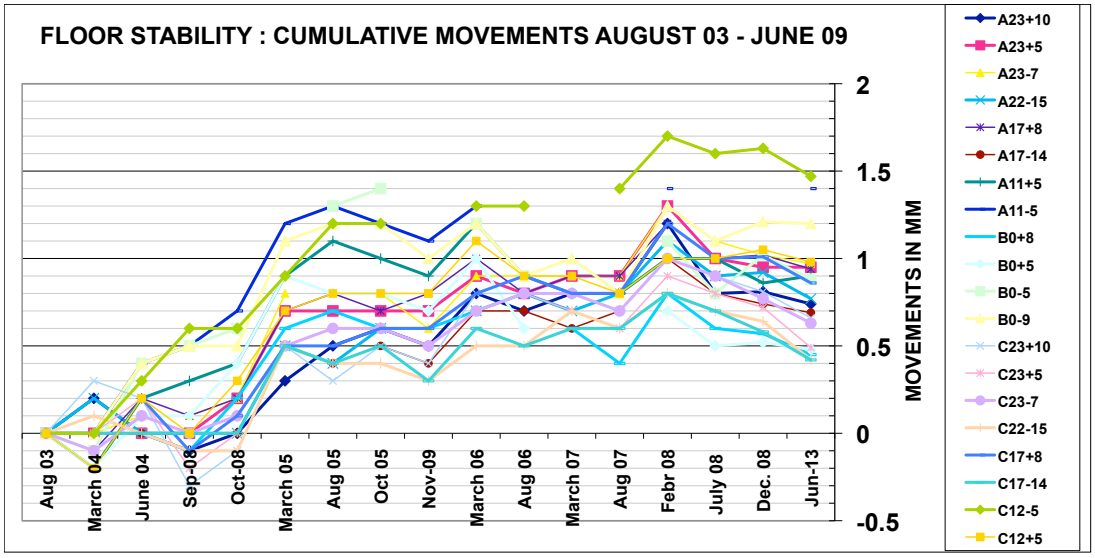


Figure 7. Cavern survey made between years 2003 and 2007 showing that the maximum displacement is of the order of 1 mm and has stabilised.

in place without the IBL using the same tooling designed for the beam pipe extraction. The tooling has to precisely control the positioning and alignment, to correct for the bow due to the weight during the insertion of the IST. The tooling has to remotely anchor the IST to the wire suspension system of the present beam pipe. Once the IST is in place, the beam pipe with the IBL will be more easily inserted.

The radial clearance between Pixel *B*-layer and IST envelopes is 2 mm (45.5 mm - 43.5 mm). The tooling designed for insertion of the IBL will use remote visual inspection and active system to control the bow and will need precise alignment. A full scale mock-up is in construction to extensively test all these operations.

1.3.5 Integration and commissioning with the existing Pixel detector

The IBL acts as a fourth pixel layer of the Pixel detector unit, rather than being a new sub-detector on its own; this irrespective of using substantial different technologies in many of its parts. The design of the off-detector readout, DCS, interlock and TDAQ software are developed and coordinated in tight connection with the Pixel Collaboration. In particular, the TDAQ and Software working groups of IBL and Pixel will be common, with unique coordinators. The IBL Collaboration and its management structure (Chapter 11) is intended to be in place only for the IBL construction and commissioning phases, the latter being the last step carried on as a joint effort. After this point, the IBL management structure will end its mandate and the IBL will be absorbed in the Pixel Collaboration. This organization of the project, defined in the IBL Memorandum of Understanding (MoU), will help in the tight connection needed for the integration and commissioning.

2. Physics and Performance

In this Chapter the implications of the IBL detector on the performance of the ATLAS experiment and thereby on its physics program during LHC Phase I are discussed. The improvements in track and vertex reconstruction and on the b tagging performance in the presence of high luminosity pileup have been studied using *Geant4* [10] based simulation and the ATLAS full reconstruction chain.

2.1 The Physics Goals of ATLAS during Phase I

There is no division in the physics program of ATLAS before and after the upgrades. The IBL installation will occur after the experiment has accumulated sufficient luminosity at 7 to 14 TeV, such that explorations of a new energy regime will have progressed considerably, but the full power of the LHC will not have been exploited. Tracking and vertex performance will be critical to this full exploitation.

The physics program of ATLAS will evolve as discoveries are made, however some physics signatures are so generic that they will be important whatever the discoveries are. One of these is the ability to distinguish jets arising from the production of different quark flavors. While jets from light quarks cannot be distinguished, those from bottom (and to a lesser extent charm) can be identified by exploiting the lifetime of the B-mesons and baryons present in the jets. A precision vertex system capable of tagging b jets with high efficiency and excellent rejection of jets from light quarks is essential. A low mass Higgs boson is expected to couple preferentially to b quarks and while the discovery of a Higgs via the decay to b quarks is difficult, confirming observations requiring less statistical significance will be powerful in constraining the Higgs couplings and determining whether its properties are consistent with those expected for a standard model Higgs boson. Observation of Higgs bosons at low mass might be improved by using the WH final state and selecting events where the Higgs has large transverse momentum and the two b quarks emerge as a single jet. In this case event rates are lower and integrated luminosity in excess of 30 fb^{-1} will be needed for a discovery in the challenging mass region below 130 GeV. In some extensions to the standard model the Higgs may be produced in the decay of other new particles. In these cases the production rates can be low but the signal to background ratio high due to the presence of other particles produced in the same event. The low rate would therefore restrict detection of the Higgs to final states with a large branching ratio: $b\bar{b}$ where the Higgs would appear as a resonance in the di-jet mass distribution where both jets are tagged as coming from b quarks. Supersymmetric models could have decays of this type. If models based on supersymmetry or extra space-time dimensions prove to be correct, there are expected to be many new particles produced and the LHC will explore their properties. Distinguishing these particles from one another will require identification of the decay products.

The identification of τ leptons proceeds primarily via their hadronic decays: unless the electron or muon from the leptonic decay can be proved not to have arisen from the interaction vertex, it cannot be distinguished from a directly produced electron or muon which will likely have a larger rate. The primary features of a hadronic τ decay are the narrow jet with low invariant mass and low track multiplicity and the dominant source of fakes is the much higher rate of QCD jets. Vertex information can be used to improve the rejection of this background. The validity or otherwise of

$e/\mu/\tau$ universality is a powerful tool in determining the nature of new physics: decays of known standard model particles respect this symmetry, provided that the particle is heavy enough. The decay of a Higgs boson is proportional to the lepton mass and tau final states dominate over e and μ. Supersymmetric models often have result in the partner of the τ being lighter than that of the e or μ, and consequently having a larger production rate.

After the IBL is installed, and before the next major shutdown in 2020, the LHC luminosity will reach twice the nominal value, 2×10^{34} cm^{-2}s^{-1}, with around 50 interactions per bunch crossing. These will produce large backgrounds, including additional jets from QCD or other background processes like $t\bar{t}$ production. Careful event selection will be required to select signal events and reject backgrounds. For example, should supersymmetry have been discovered the direct production of the super-partners of the electroweak gauge bosons will be searched for. These have a small production cross-section and their signatures will be obscured by other larger rate processes such as the production of top quarks or heavier strongly interacting superpartners such as gluinos. The electro-weak production processes are accompanied by less additional jets from QCD radiation: the requirement that these jets are absent can be used to reject background. However these jets are soft and at high luminosity could arise from a different pp interaction in the same bunch crossing. The longitudinal information from the ATLAS tracker can then be used to assign these jets to individual primary vertices in order to only veto events where there are additional soft jets from the same pp interaction as the decay products of the electro-weak superpartners. The absence of such jets can also be used to distinguish the two dominant mechanisms for the production of Higgs bosons: $gg \to H$ and $qq \to qqH$, as the former has more jets in the central region of the detector than the latter. Distinguishing these production process provides detailed information on the Higgs couplings. As the number of pile-up interactions increases, better vertex resolution is needed to to distinguish the primary vertex from nearby secondaries.

2.2 Performance of the Present Inner Detector at Phase I Luminosities

The ATLAS ID [11] has been designed to operate at a nominal luminosity of 10^{34} cm^{-2}s^{-1}. Emphasis has been given as well to physics accessible at initial luminosity running at 10^{33} cm^{-2}s^{-1}

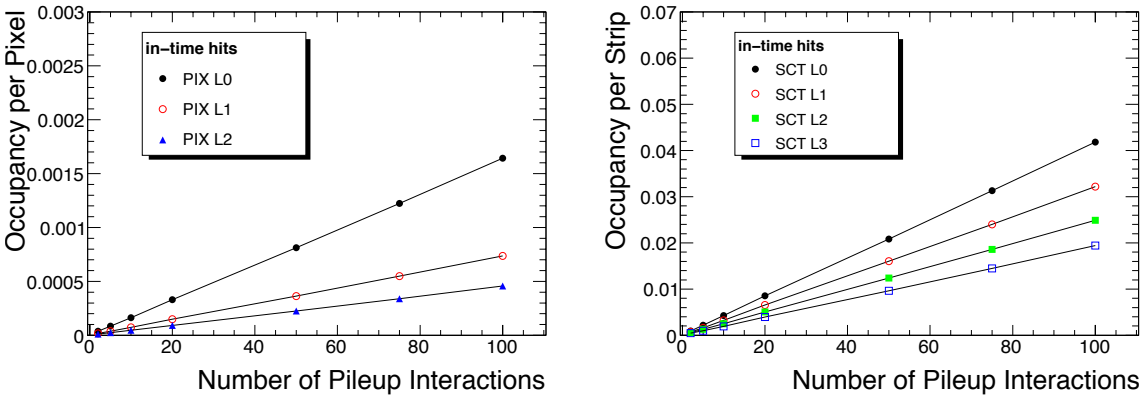


Figure 8. Expected occupancies as a function of the average number of pileup interactions for (left) the Pixel barrel layers and (right) the SCT barrel layers for the present ATLAS detector.

where more complex signatures such as τ lepton tagging and heavy flavor reconstruction are a key issue. Provided the current ID continues to be fully functional it will perform well even somewhat above nominal luminosity. However the IBL is required for an excellent performance for Phase I luminosities that preserves good sensitivity for physics channels with signatures including b jets, as well as for a robust reconstruction in the case of a significant fraction ($> 10\%$) of Pixel modules not working.

The very successful commissioning of the present ID started with cosmics data taking [12] prior to the LHC pilot run at 900 GeV. In the 2010 run, ATLAS is routinely taking data at 7 TeV centre of mass energy. The ID is performing as expected and fast progress was made in the understanding of the data, as can be seen e.g. in [13]. The LHC has delivered instantaneous luminosities above 10^{31} cm^{-2}s^{-1} with a small number of bunches, already leading to significant pileup in the detector. The extrapolation from those initial running conditions to LHC Phase I luminosities at 14 TeV has to rely on Monte Carlo simulation, while measurements of the charge particle multiplicities at 900 GeV, 2.36 TeV and 7 TeV [14, 15] can be used to constrain the predicted occupancies. The Monte Carlo models underestimate the multiplicity by 15% - 20% and the p_T spectrum in data is softer than predicted. At the same time the energy dependence seems correctly described by the models.

The predicted Monte Carlo [16] hit occupancy as a function of the average number of in-time pileup events is shown in Fig. 8 for the different barrel layers of the present Pixel and SCT detector. It increases linearly as expected for these low occupancies. At 50 pileup events, corresponding to a luminosity of 2×10^{34} cm^{-2}s^{-1}, the occupancies in the Pixel detector range from 0.08% in the present B-layer to 0.02% in layer 2. This is much lower compared to the SCT, which ranges from 2% for layer 0 to 1% in layer 3, because of the higher granularity of the Pixel detector. For this reason the ATLAS ID track reconstruction (*NewTracking* [17]) starts track finding in the Pixel layers. With high luminosity pileup the increasing occupancy in the Transition Radiation Tracker (TRT) leads to a reduced number of precision measurements usable to determine the momentum in the track fit and therefore to a degradation in the momentum resolution for muons, as can be seen

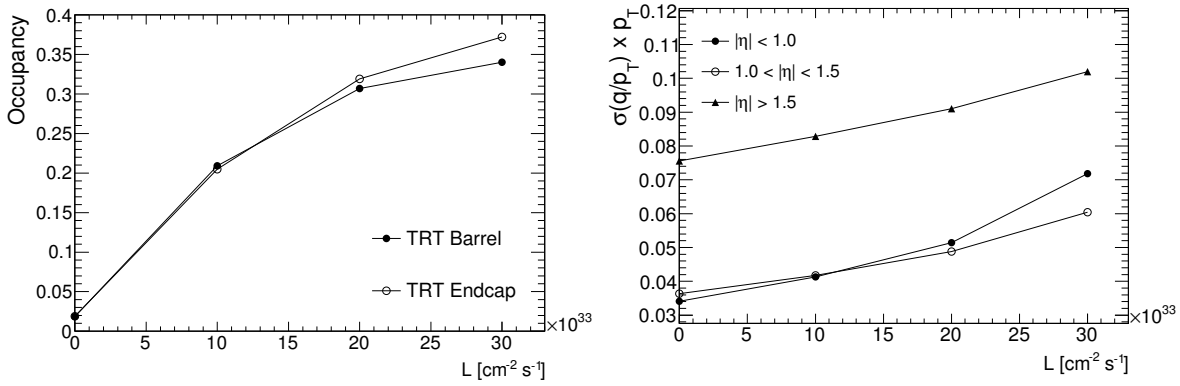


Figure 9. Expected occupancy of valid hits with a leading edge in the TRT barrel and endcaps (left), as well as the momentum resolution for single 100 GeV muons in different η regions (right) as a function of the instantaneous luminosity.

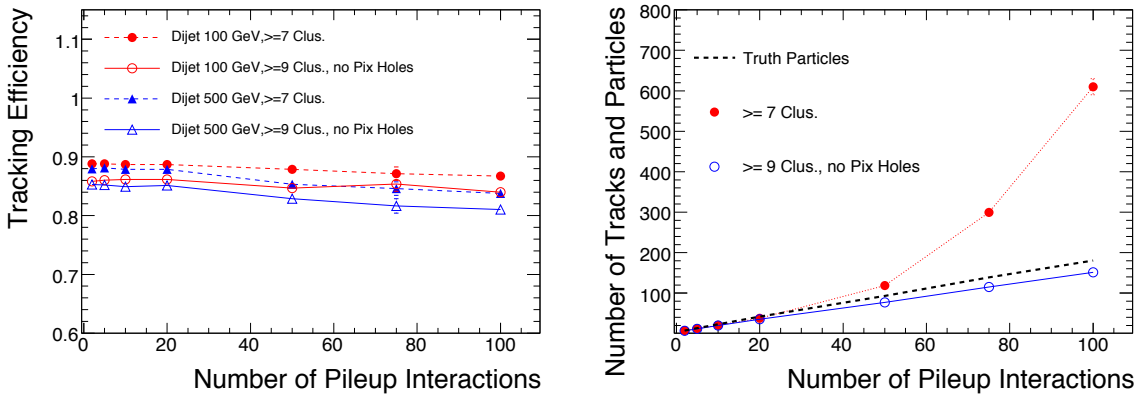


Figure 10. (left) Efficiency for reconstructing tracks in 100 GeV and 500 GeV di-jet events and (right) rate of reconstructed tracks as a function of the average number of pileup interactions. Shown are the results for different track selections for track candidates with $p_T > 1$ GeV and $\eta < 1.0$ accepted by the pattern recognition.

in Fig. 9. However, the ID momentum resolution is not a limiting factor for most of the physics channels accessible during Phase I.

Figure 10 shows the efficiency to reconstruct a track at $\eta < 1.0$ in 100 GeV and 500 GeV dijet events. The efficiency to reconstruct a track in the ID is limited by the rate of hadronic interactions of the pions with the detector material and is therefore nearly independent from the level of pileup. In the more collimated 500 GeV jet events a small reduction is visible at high pileup which is due to increased cluster density in those jet cores with pileup. For reference the results are shown with the nominal track selection, requiring at least 7 silicon (Pixel and SCT) clusters on the track out of the nominal 11 silicon layers, and a more tight selection, requiring at least 9 clusters and no Pixel module crossed by the track without an associated cluster (a so called *Pixel hole*). With a fully functioning detector, as used for this figure, the effect of tightening the track cuts is a 3% reduction in the tracking efficiency, which is mainly because requiring 2 additional clusters implicitly increases the required track length and hence increases the chance of loosing the track due to a hadronic interaction. In the same Fig. 10 the number of reconstructed tracks in the event is shown as a function of the average number of pileup events. For the nominal track selection a steep rise due to fake tracks is observed for luminosities exceeding 10^{34} cm^{-2}s^{-1}. Tightening the requirement on the number of clusters from 7 to 9 and adding the cut on Pixel holes removes most of those additional track candidates. While with a fully functional and highly efficient detector simulation those cut settings are rather safe, they leave little margin for a robust reconstruction using a realistic detector with inefficiencies and inactive modules.

The impact parameter resolution for tracks in 500 GeV di-jet events is affected very little by pileup, as is shown in Fig. 11 for different bins in η. Such degradation would result from cluster merging due to the limited double track resolution, but only at luminosities above 2×10^{34} cm^{-2}s^{-1} does the track density give rise to a significant rate of shared clusters in the Pixel detector. The dominant effect is confusion in the pattern recognition that leads to wrong associations of clusters to tracks and therefore gives rise to higher non-gaussian tails in the impact parameter distribution.

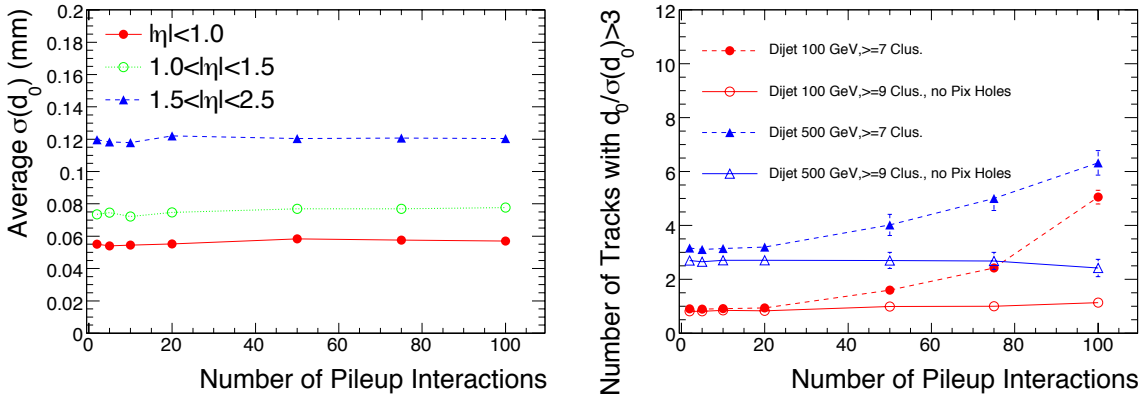


Figure 11. (left) Impact parameter resolution for tracks in 500 GeV di-jets events in bins of η as a function of the average number of pileup interactions. (right) Rate of tracks at $\eta < 1.0$ with d_0 offsets (with more than 3σ) in 100 GeV and 500 GeV di-jets events as a function of pileup events. Shown are the results for different track selections for track candidates accepted in the pattern recognition.

Fig. 11 shows as well the rate of tracks in the barrel ($\eta < 1.0$) with an impact parameter significance larger than 3σ w.r.t. the primary vertex, which is sensitive to such non-gaussian tails. The difference in jet energy scale between 100 GeV and 500 GeV jets as well as the collimation of those jets defines the rate of significant impact parameters at low luminosity. For nominal tracking cuts, requiring 7 Pixel plus SCT clusters, a fast rise in the rate of such tracks is seen for both jet energy scales. Such offsets directly affect the primary vertex reconstruction as well as the b tagging performance. Cutting hard on the number of Pixel plus SCT clusters and Pixel holes again mitigates the problem.

The integration of the IBL in the ID not only improves the impact parameter resolution, but as an additional low occupancy layer it helps the robustness of the tracking against detector problems and pileup. It therefore improves the primary vertex reconstruction and b tagging at Phase I luminosities, as will be demonstrated in the following.

2.3 IBL in the ATLAS Full Simulation and Reconstruction

The IBL detector has been fully integrated in the ATLAS ID software chain in order to facilitate performance studies. In the ATLAS software framework a central geometry model, the *GeoModel* [18] description, is used to implement the IBL as part of the full detector. This implementation in GeoModel provides a very detailed description of the actual detector geometry, including support and cooling structures and correct material properties. The detailed simulation geometry is derived from GeoModel for the full detector simulation using the *Geant4* [10] toolkit. A reconstruction geometry description (*TrackingGeometry* [19]) is the second model derived from GeoModel, which provides an abstract detector model built from layers and surfaces. It is optimized for an accurate overall material description and CPU performance. The detector response is modelled in a digitization package, which in the case of the IBL is based on the existing Pixel digitization algorithm. Similarly, the Pixel clustering package has been used to reconstruct the IBL. Tracks are reconstructed using the standard ATLAS track reconstruction *NewTracking*, taking full benefit from the

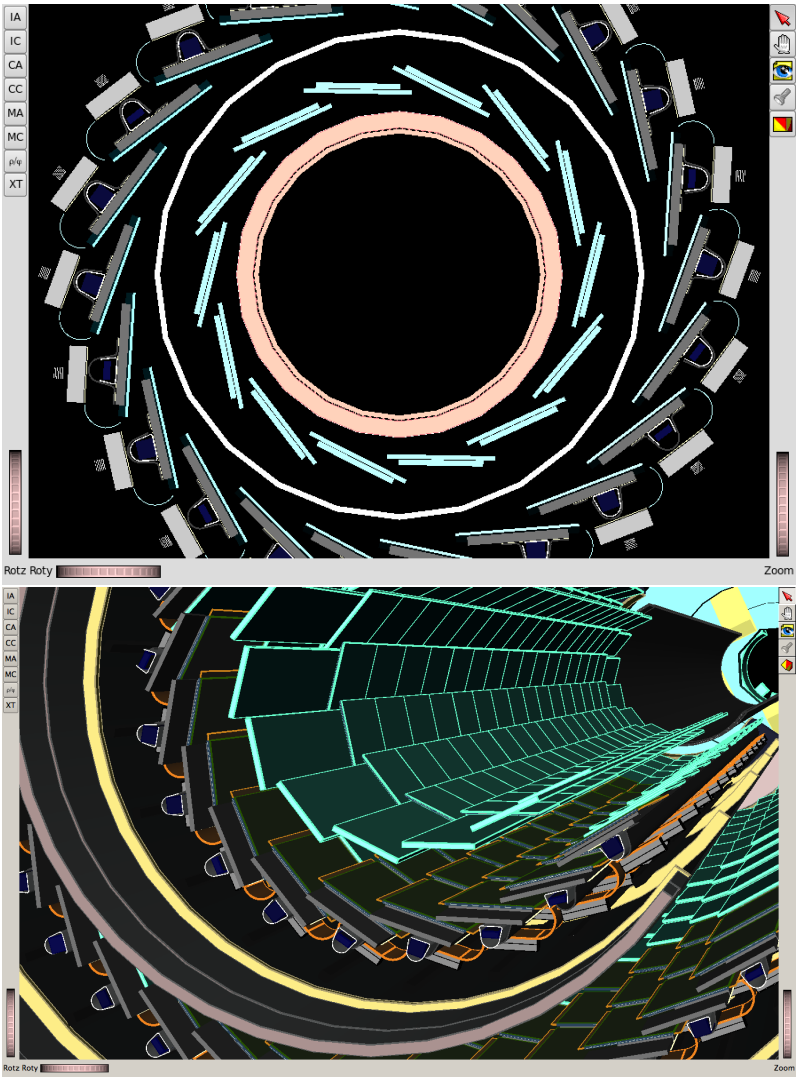


Figure 12. (top) XY view showing the new (smaller) beam pipe, the IBL with modules, staves and support tube and the Pixel *B*-layer all implemented in the ATLAS geometry model; (bottom) 3D view of the IBL inside the Pixel detector illustrating the geometrical arrangement.

additional track measurements from the IBL. The default ATLAS reconstruction is used for vertexing, *b* tagging and to reconstruct objects like jets and leptons. The analysis then proceeds using ATLAS analysis data formats and as much as possible standard performance analysis software to derive the results presented hereafter.

2.3.1 IBL geometry and material budget

The IBL geometry description required the insertion of another layer envelope into the current Pixel detector description. In parallel, the beam pipe radius was decreased to the proposed design values. The IBL modules are described in full detail, but support and cooling structures are smeared out over the full module surface, as can be seen in Fig. 12. The services outside the tracking volume

were omitted as they were not relevant for the studies discussed in the following.

A correct description of the detector material is crucial for simulation and reconstruction. For the simulation geometry, this is done by translating the very detailed GeoModel description and associated material properties into a corresponding Geant4 detector model. Figure 13 illustrates the contributions of the different parts of the IBL to the overall material budget of the ID, following the material budget corresponding to the layout described in Section 1.3.1. At normal incident angle the IBL, as implemented in GeoModel, accounts for 1.5% X_0 including the support tube. The interaction of the particles with the detector material during simulation is then carried out by the Geant4 library.

In track reconstruction, the detector material has to be taken into account as stochastic noise terms in track fitting and energy loss corrections in track propagation. As these processes are very frequent the access to the material model needs to be optimized in speed, while a small decrease in the accuracy of the material description is acceptable. The TrackingGeometry material description is kept in synchronization with the simulation geometry by an automated procedure that maps the Geant4 material description onto the layer frame of the TrackingGeometry. An overall relative agreement to the 1% level is reached with this procedure [19].

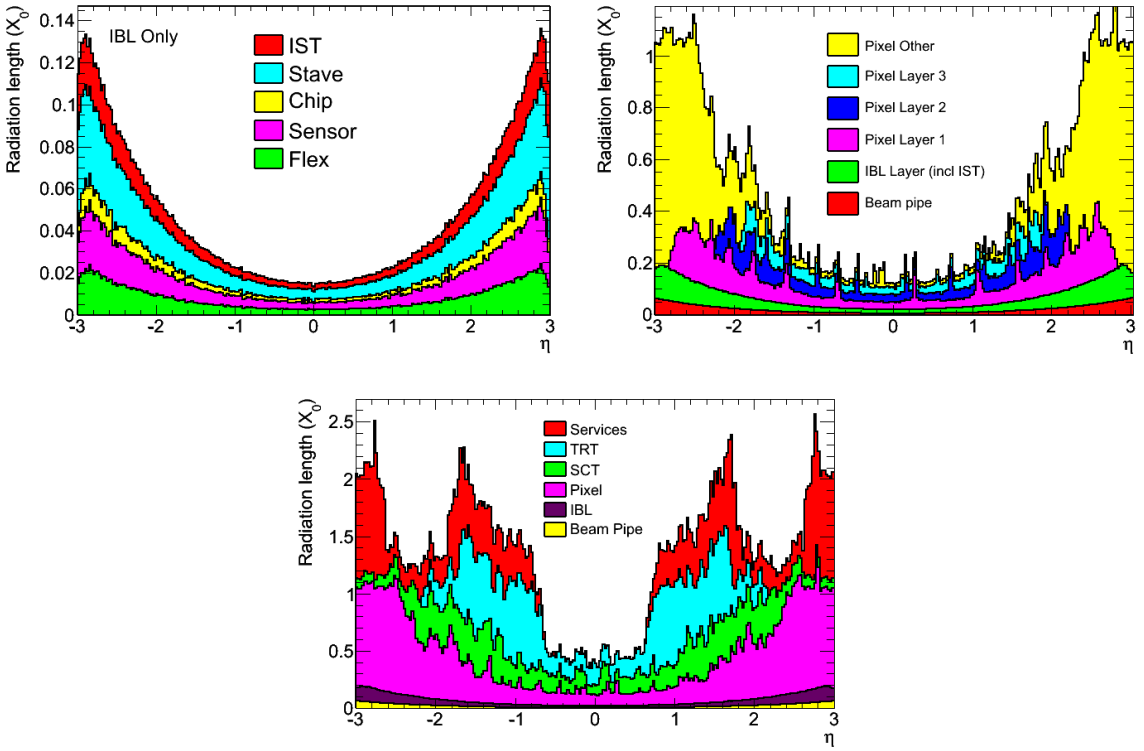


Figure 13. Radiation length as a function of η for the different ID components as implemented in the ATLAS geometry model. Shown are the IBL components (top, left), the IBL as part of the Pixel system (top, right) and the IBL as part of the overall ID (bottom). External IBL supports and services outside the active tracking volume are not included in the description yet.

2.3.2 Modeling the IBL detector response

The Pixel detector provides measurements of clusters, which are defined as linked set of fired Pixel cells. The resolution is determined by the accuracy to which the crossing point of an incident particle can be reconstructed from the cluster shape and deposited charge. With the present Pixel detector the *digital* clustering algorithm gives equal weight to all pixels in a cluster and provides a X_{local} resolution of about 10 μm, depending on the particle incident angle. Using the pulse height measurement (*analog* algorithm), improves the resolution in certain angular regions down to 4–6 μm [2, 20, 21].

With respect to the current Pixel detector, the IBL has three main differences affecting the reconstruction of cluster position: wider range of particle incident angles in the $R\phi$ plane, wider clusters in the z direction, due to the smaller segmentation, and lower ToT resolution due to 4-bit ToT dynamic range in FE-I4 with respect to the 8-bit range of FE-I3 (see Section 3.3).

There are three sensor-technology candidates for IBL: silicon planar sensors, silicon 3D sensors, and SVD diamond. The properties of these different technologies and the status of the qualification procedure are described in Section 3.2. The detector intrinsic resolution observed in test beams is similar and the detector choice is not expected to be critical from the point of view of tracking performances. The main difference in track reconstruction will be the effect of the Lorentz angle on the cluster size (see Fig. 14) for silicon planar and CVD diamond sensors, which does not affect 3D sensors. After radiation damage, when the detector will be operated at high field, drift velocity will be near to saturation. In this situation, the Lorentz angle will be much reduced [22], and no practical difference between the technologies is expected.

A comparison between the ToT measurement in individual pixels between the FE-I3 electronics of *B*-layer and the FE-I4 electronics of IBL is shown in Fig. 15. Since for most clusters the generated charge is shared across several pixels, the distributions are dominated by low ToT hits. The shoulder at ToT = 20 for *B*-layer and ToT = 9 for IBL correspond to single-hit clusters in which all the charge is collected in an individual pixel cell. Due to the limited bits available to store ToT information in FE-I4, all hits with ToT $\geq$ 13 are put in the same bin. This choice is taken because high ToT signal corresponds to energy loss fluctuations from delta ray generation in silicon and

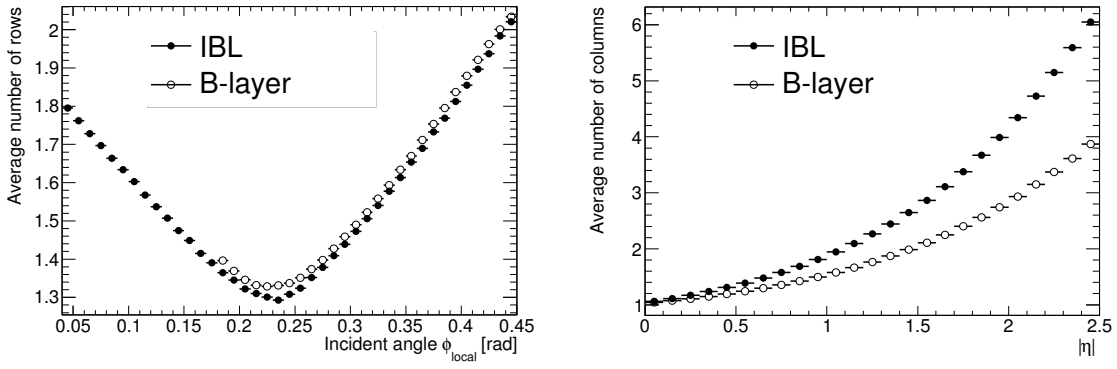


Figure 14. Average cluster size as function of particle incident angle projected in the $R\Phi$ (left) and Rz (right) planes, for IBL and *B*-layer.

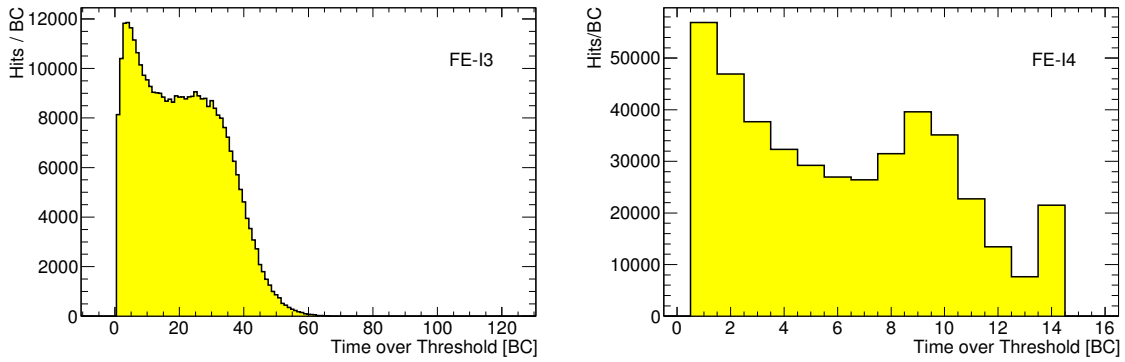


Figure 15. Individual pixels ToT distribution for FE-I3 *B*-layer (left) and FE-I4 IBL (right).

therefore do not carry position information. It allows instead to expand the low ToT region where charge sharing is relevant for improving the cluster reconstruction.

The intrinsic detector resolution, computed by comparing the cluster reconstructed position with the particle crossing point is shown in Fig. 16, comparing the *digital* and *analog* algorithms

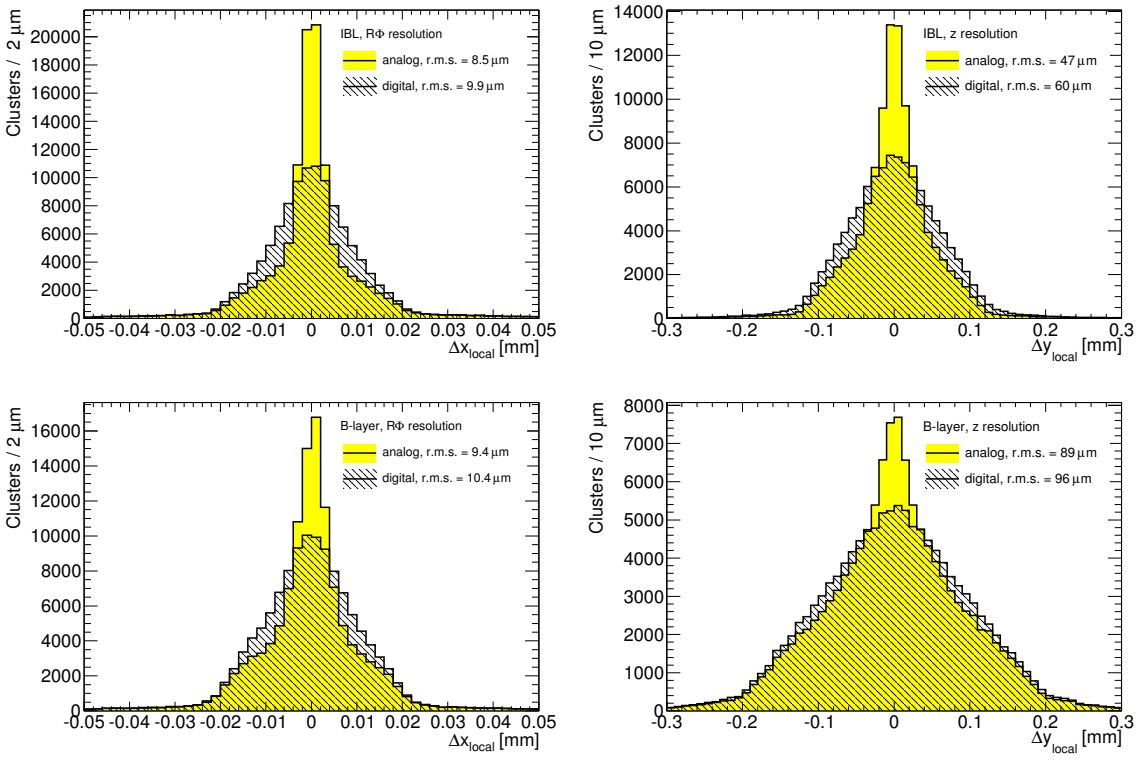


Figure 16. Residues distribution between reconstructed and true particle crossing point for IBL (top) and *B*-layer (bottom). The detector intrinsic resolution is estimated from the r.m.s. of the residues.

for *B*-layer and IBL. The resolution is strongly improved using the analog algorithm. In the $R\phi$ projection most of the improvement is from 2-pixel clusters, while 1-pixel clusters are the source of the remaining broader distribution in the ± 25 μm region. Compared to the present *B*-layer, the wider range of rate incident angles of tracks crossing the IBL result in more 2 Pixel clusters in *R Phi* and therefore in a slightly improved resolution. The tails at higher residuals comes from 3-pixel cluster, which contain a big fraction of events with δ-rays.

The detector performance studies presented in the following use benchmark non-irradiated planar silicon sensors for the IBL, and for practical reasons an *8 bit analog* algorithm for cluster position reconstruction. This approximation is justified as the difference in cluster resolution between the calibrated FE-I3 and FE-I4 output is small, especially in view of the effects of multiple scattering.

2.3.3 Adapting the ATLAS track reconstruction to the IBL

The next step, after the cluster reconstruction in the IBL, Pixel and SCT and after the TRT drift circle creation, is the formation of three-dimensional space points from the silicon hits. Pixel clusters provide local two-dimensional positions on a fixed module surface and therefore map directly into space points. On the contrary, SCT clusters do not transform directly into space points because a single strip provides a precise measurement in only one direction. Instead, space points are formed by combining the information from pairs of clusters from a SCT module, which consists of two pairs of sensors glued back-to-back at a stereo angle of 40 mrad.

The purpose of this study is to evaluate the performance improvements of the ATLAS ID with IBL at Phase I luminosities. Therefore only the primary track reconstruction package *NewTracking* [17] is used, which aims to reconstruct the tracks originating from the primary interaction(s) starting the pattern recognition in the Silicon detectors. The reconstruction algorithms starting from the TRT information (*BackTracking* [23]) to find secondaries are not used, because they are not tuned for an environment with Phase I pileup. Because of the modular design of the ATLAS track reconstruction NewTracking, the IBL was included into the pattern recognition simply as a 4th Pixel layer at smaller radius.

Seeds are formed from sets of three space points with each space point originating from a unique layer of one of the silicon detectors. The seeding algorithm allows for four possible combinations of space points: all space points in the IBL and Pixel detectors, all in the SCT, two space points in the IBL and Pixel detectors and one in the SCT, or one in the IBL or Pixel detectors and two in the SCT. The fourth category is not used by default in NewTracking. Seeds are preselected by imposing a minimum requirement on the momentum or maximum requirement on the impact parameters. The requirements differ between the categories. For each seed a crude estimate of the perigee parameters can be obtained based on a perfect helical track model. Those parameters define a search road with all IBL, Pixel and SCT modules that are near the estimated trajectory. A (combinatorial) Kalman filter is used to reconstruct track candidates in those roads. The final selection of tracks from the sample of candidates uses an ambiguity processor. The task of the ambiguity processor is to resolve the hit association to tracks and to select the genuine tracks, while suppressing as much as possible fake combinations. All candidates passing a crude preselection are refitted using the full fledged *GlobalChi2* track fit with precise material corrections and sophisticated outlier removal. Successfully fitted track candidates compete against each other for the best *score* defined

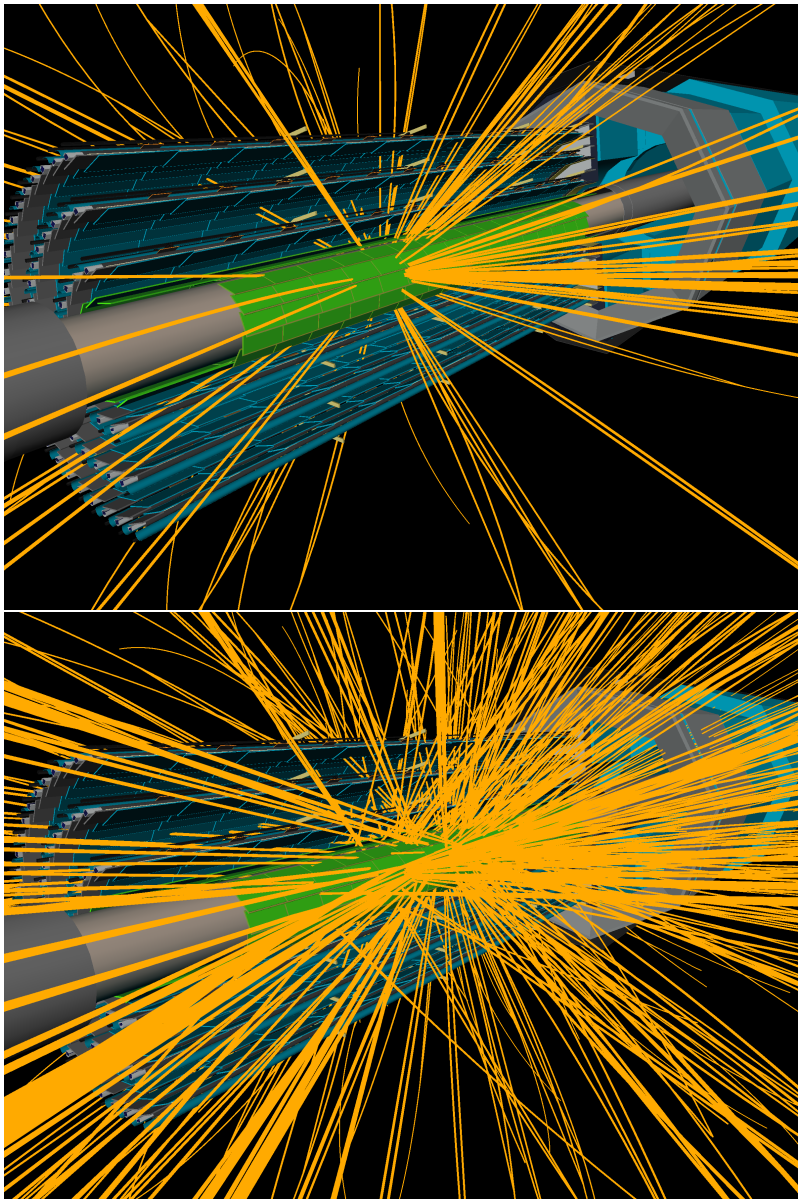


Figure 17. 3D displays of a Geant4 simulated event containing 2 jets of 500 GeV reconstructed using the IBL. Shown is the IBL, the beam pipe, the 3 Pixel barrel layers opened from the front, as well as the Pixel barrel supports and endcap structures in the background: (top) all tracks in the event with $p_T > 0.5$ GeV and more than 1 Pixel+IBL clusters while (bottom) shows the same event adding 2×10^{34} cm^{-2}s^{-1} pileup and applying the same track selection.

by the cluster content, the number of holes, the fit quality, etc. The score is chosen such that a track with a cluster in the IBL (or in the *B*-Layer for a nominal detector) is preferred above track candidates without. The best tracks are selected and remaining candidates sharing too many clusters with those selected tracks are refitted, removing those clusters, and the score is recomputed. The result of the ambiguity processing is a final set of silicon tracks, which are then extended into the

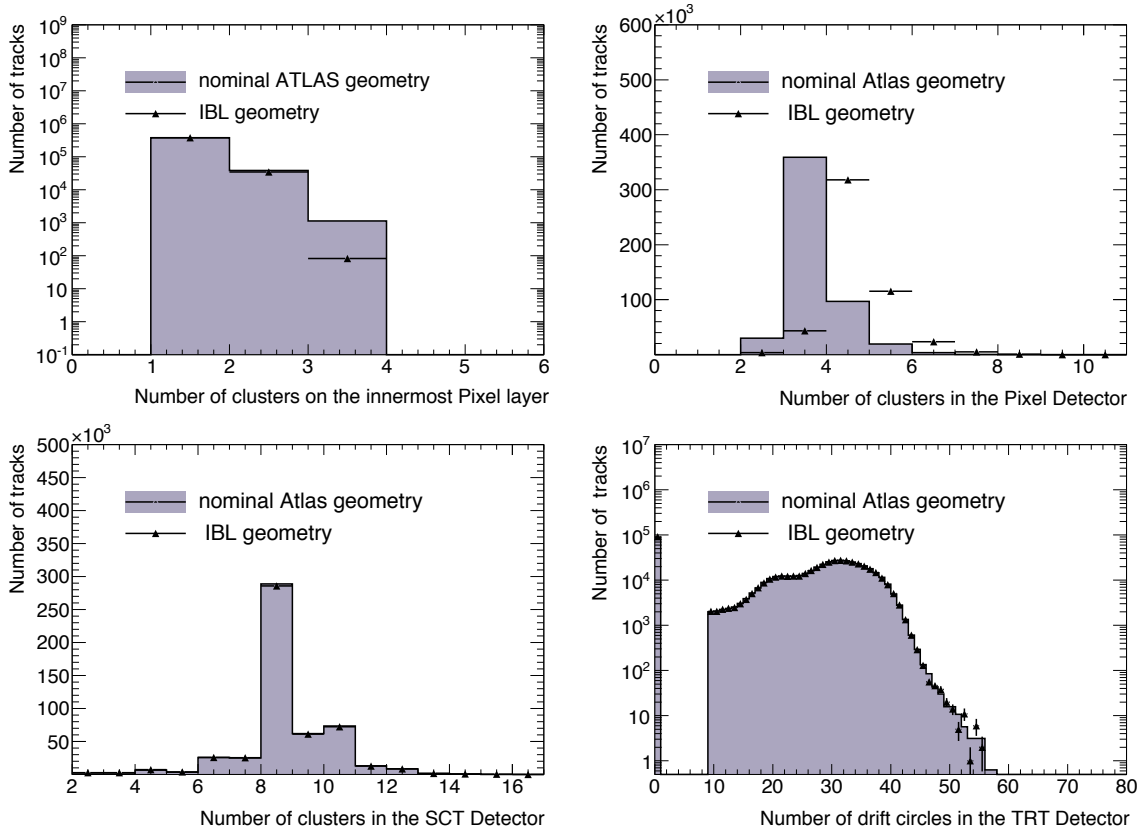


Figure 18. Cluster and drift circle association to reconstructed tracks in $t\bar{t}$ events without pileup. (top-left) Number of associated clusters in the innermost later; (top-right) total number of Pixel clusters; (bottom-left) total number of SCT clusters; and (bottom-right) number of associated TRT drift circles.

TRT. For each track the drift circles in a helical road around the trajectory are selected and a (combinatorial) Kalman filter is used to select the list of TRT drift circles and to resolve the left-right ambiguity. Each combination of a silicon only track and a list of TRT drift circles is refitted using the full track fit. Successfully refitted tracks are scored again and reevaluated against the silicon only track in terms of hit content, fit quality, etc. The final set of reconstructed tracks then contains the list of successfully extended tracks plus the list of remaining silicon only tracks.

Figure 17 shows a reconstructed 500 GeV di-jet event with the IBL. Shown are all tracks that pass the cut $p_T > 0.5$ GeV and have at least 7 IBL, Pixel and SCT clusters, as used in the pattern recognition. Tracks with less than 2 Pixel or IBL clusters are not shown to simplify the picture. In the same figure the event is shown as well with 2×10^{34} cm^{-2}s^{-1} pileup. No z vertex constraint has been used, such that tracks from all interactions passing the p_T and other quality cuts are reconstructed. Figure 18 shows the cluster and drift circle association to tracks in $t\bar{t}$ events without pileup. Compared are the results for events with and without IBL for tracks that pass the b tagging track selection, which requires at least one associated cluster on the track in the innermost layer (Pixel or IBL, respectively) and $p_T > 1$ GeV. While the total number of Pixel (plus IBL) clusters is increasing by 1 with the IBL, the number of clusters in the innermost layer remains basically

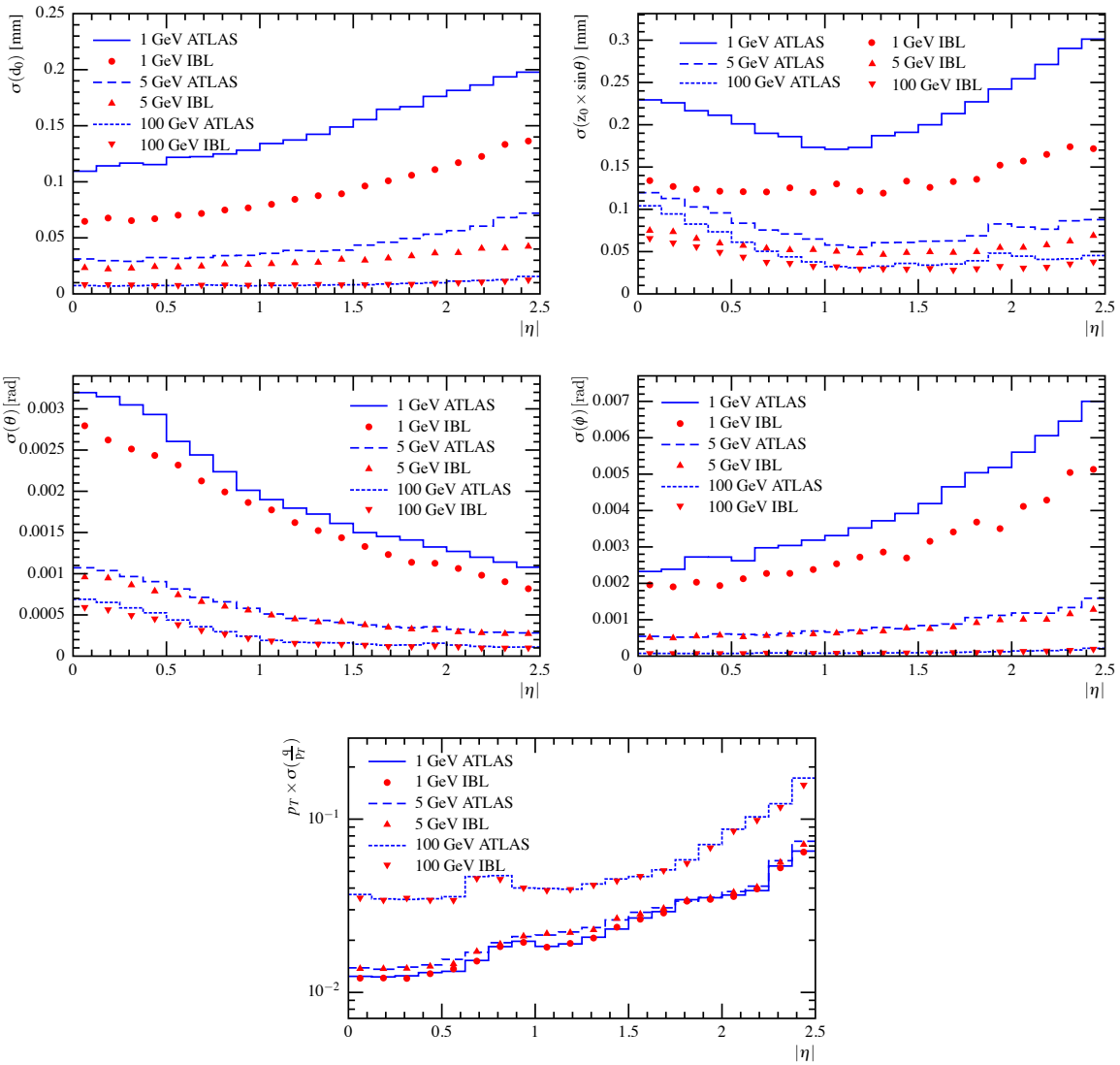


Figure 19. Track parameter resolutions for single muons at 1, 5 and 100 GeV as a function of η. Compared are the expected resolutions: (top-left) transverse impact parameter d_0; (top-right) longitudial impact parameter $z_0 \sin\theta$; (middle-left) angle θ; (middle-right) angle ϕ; (bottom) relative error on the curvature $p_T/\sigma(q/p_T)$ for the current ID and for the ID with IBL. No pileup was added to the events.

unchanged. The reduction in the number of 3 associated clusters in the innermost layer with IBL reflects the missing z overlap of the modules in a stave, leading only to occasional splitting of clusters across 2 adjacent modules in z in the very forward region. The number of associated SCT clusters and TRT drift circles is unchanged, as expected.

2.3.4 Improvements in tracking for single particles and particles in jets

The gain in the precision of the reconstructed tracks from the IBL is demonstrated using single 1, 5 and 100 GeV single muon events. Figure 19 shows the resolution as a function of η for the fitted

transverse (d_0) and longitudinal impact parameter ($z_0 \times \sin\theta$), the angles θ and ϕ as well as for the relative error on the measured curvature ($p_T \times \sigma(q/p_T)$. The results show the expected behavior that the biggest contribution of the IBL to the measurement precision is to the impact parameter resolution. The significant gains are thanks to the additional layer at smaller radius, to the smaller z pitch of the IBL compared to the present Pixel detector. The contribution from the IBL to the measurement of the track curvature is small as the overall track length is nearly unchanged.

The impact parameter resolution is the crucial parameter that affects the b tagging performance. Fig. 20 shows the measured d_0 and $z \times \sin\theta$ impact parameter distribution with respect to the Monte Carlo truth for tracks in $t\bar{t}$ events without pileup. Compared are tracks that pass the track quality selection for the b tagging, which requires at least one associated cluster in the innermost layer and $p_T > 1.0$ GeV. A clear improvement is seen in both distributions by the addition of the IBL. Figure 21 illustrates the gain for tracks at different η for tracks in $t\bar{t}$ events with 2 GeV $< p_T <$ 4 GeV. The shape of the distributions is induced by the η dependence of the multiple scattering effects in the material of the innermost layers and the beam pipe, as well as by the effect of the increasing z cluster size as a function of η. Figure 22 shows the p_T dependence of the d_0 and $z_0 \times \sin\theta$ impact parameter resolution. The observed p_T dependence can be described by the $A \bigoplus B/p_T$ model, for which the A term describes the intrinsic resolution of the detector visible at high p_T, while the B term describes the effect of multiple scattering in the detector material dominant at low p_T. For the slice between 0.2 and 0.4 in η, the IBL leads to an improvement in A by a factor 1.2 in d_0 and a factor 1.7 in $z_0 \times \sin\theta$, as shown in the figure. This illustrates the change in the z pitch between IBL and current Pixel detectors. The multiple scattering term improves by a factor 1.8 in d_0 and as well a factor 1.8 in $z_0 \times \sin\theta$.

2.3.5 Improvements in primary vertex reconstruction

The task of the primary vertex reconstruction is to reconstruct the vertex position of the signal and of additional pileup interactions. For this study the default ATLAS primary vertex algorithm [24] is

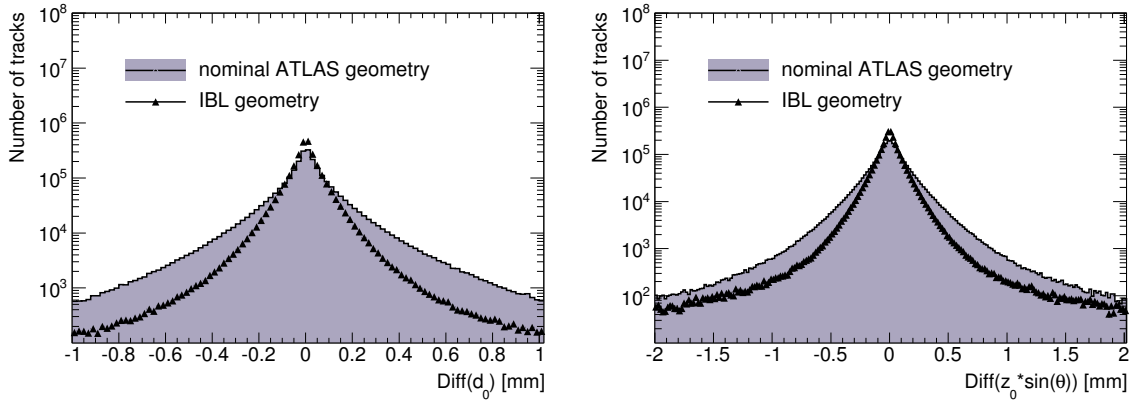


Figure 20. Impact parameter distributions of reconstructed tracks with and without IBL for $t\bar{t}$ events without pileup; (right) transverse impact parameter distribution d_0 and (left) longitudinal impact parameter distribution $z_0 \times \sin\theta$ with respect to true d_0 and $z_0 \times \sin\theta$.

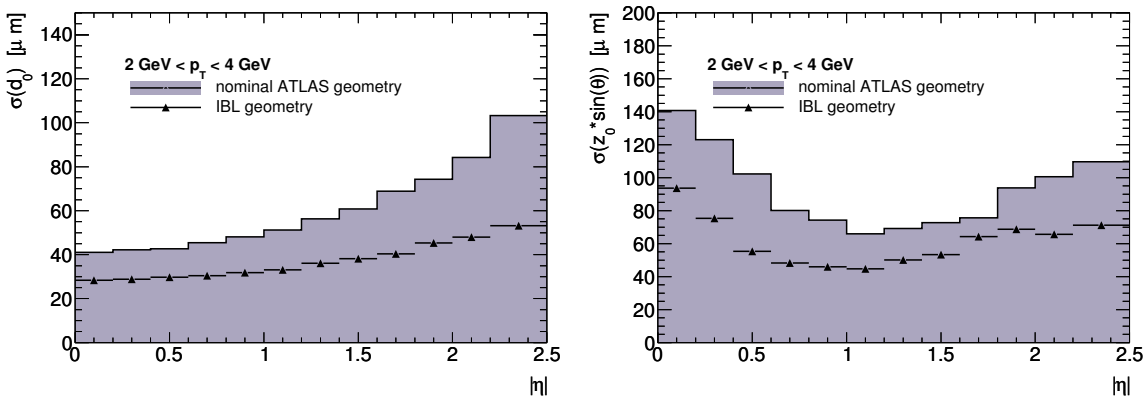


Figure 21. Impact parameter resolution as a function of η for tracks in $t\bar{t}$ events without pileup. Results with and without IBL are compared; (right) transverse impact parameter distribution d_0 and (left) longitudinal impact parameter distribution $z_0 \times \sin\theta$ with respect to the true primary vertex position of the event. Results from tracks between 2 and 4 GeV are shown.

used, which is based on the *Iterative Vertex Finder* in combination with the *Adaptive Vertex Fitter*. The task of the Iterative Vertex Finder is to find the best seed candidate scanning the z positions of all tracks ($p_T > 0.5$ GeV). The vertex position is then determined starting from that seed using the Adaptive Vertex Fitter, which is a robust vertex fitting technique as described in Reference [25]. This fitter uses an iterative scheme of *deterministic annealing* to determine the weight of individual tracks in the vertex fit, assigning small weights to outliers. Tracks incompatible with the vertex by more than 7σ are used to seed a new vertex. This procedure is repeated until no unassociated tracks are left in the event or no additional vertex can be found.

Figure 23 shows the resolution obtained for the reconstructed primary vertex in high multi-

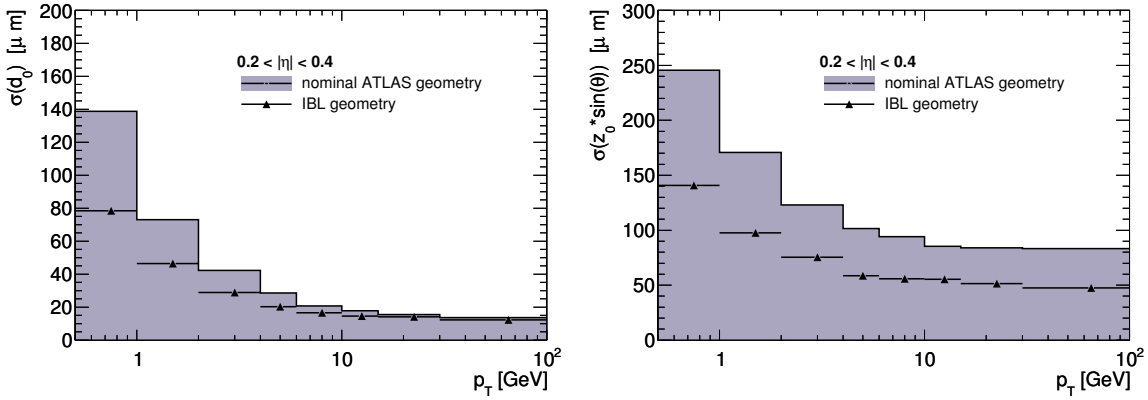


Figure 22. Impact parameter resolution as a function of p_T for tracks in $t\bar{t}$ events without pileup. Compared are the results with and without IBL. (right) transverse impact parameter distribution d_0 and (left) longitudinal impact parameter distribution $z_0 \times \sin\theta$ with respect to the reconstructed primary vertex of the event. Results for tracks with $0.2 < \eta < 0.4$ are shown.

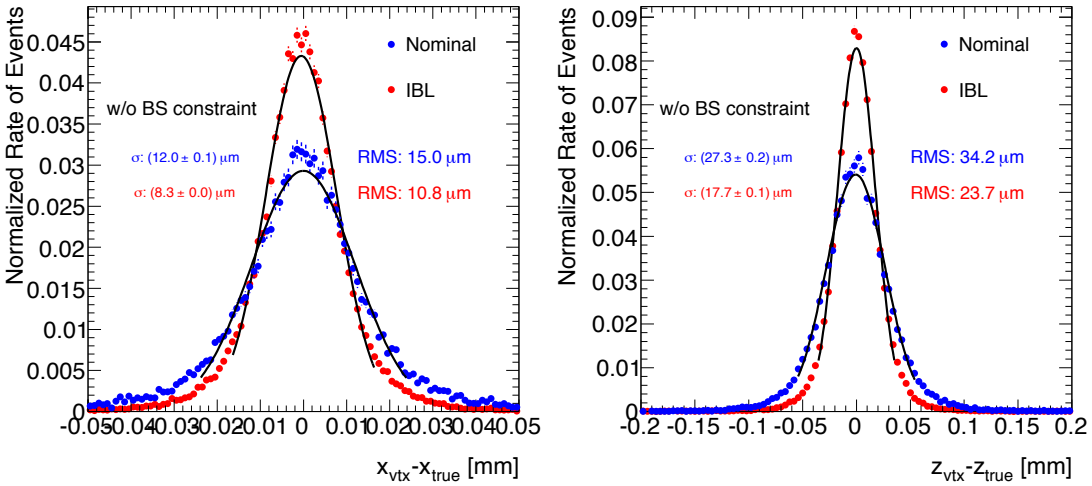


Figure 23. Resolution in x and z of the reconstructed primary vertex without beam spot constraint for $t\bar{t}$ events with and without the IBL. No pileup was added to the events.

plicity $t\bar{t}$ events without pileup and without beam spot constraint. With the IBL the resolution in x (and y) improves from 15 μm to 11 μm (RMS), the resolution in z improves from 34 μm to 24 μm. Adding the beam spot as a constraint to the vertex reconstruction leads to the results shown in Fig. 24. The beam spot is simulated with a size of 12 μm in $R\phi$, while the size in z is 45 mm corresponding to the assumed beam parameters during LHC Phase I [4]. The beam spot constraint reduces the gain in resolution with IBL in x and y, which now leads to an RMS of 8 μm compared to

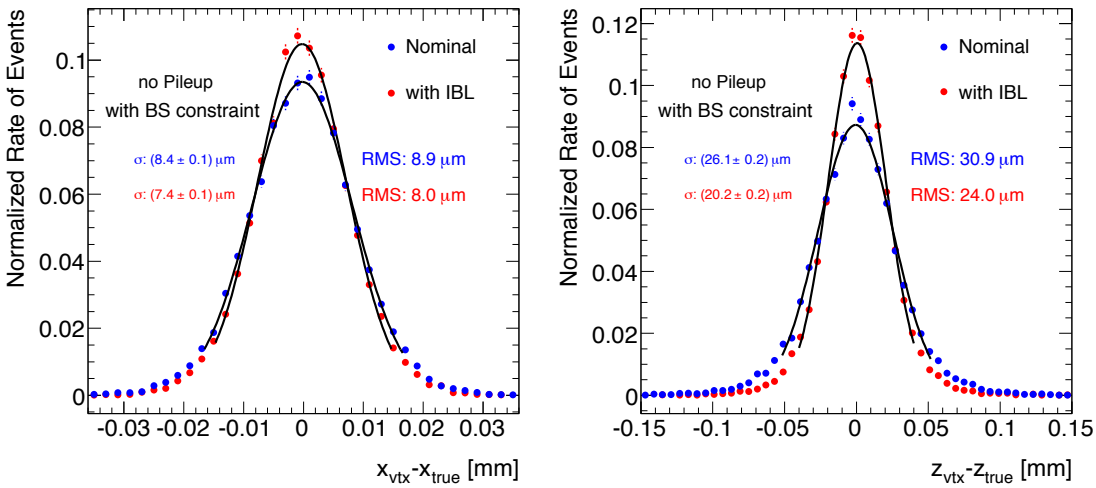


Figure 24. Resolution in x and z of the reconstructed primary vertex with beam spot constraint for $t\bar{t}$ events with and without the IBL. The simulated beam spot width is 12 μm, the beam spot length is 45 mm. No pileup was added to the events.

9 μm without IBL. In z beam-spot constraint does not help much and the resolution improvement with IBL is basically unchanged – the values are 24 μm with IBL compared to 31 μm without. The improvements in the reconstructed primary vertex resolution as well as the improved impact parameter resolution leads to a significant gain in b tagging performance, as is illustrated in the next section.

2.3.6 Impact of IBL on b tagging performance

The ability to identify jets stemming from the fragmentation and hadronization of b quarks is important for the high-p_T physics program of ATLAS for Phase I. The b jet tagging techniques used in ATLAS [26] take advantage of the relatively long lifetime ($c\tau \simeq 450\ \mu m$) of hadrons containing b quarks, as well as of the hard fragmentation and the high mass of the b hadrons. These properties lead to tracks with large impact parameters w.r.t the primary vertex and to secondary vertices with large invariant masses. Additional tagging algorithms use semi-leptonic b decays to identify b jets. For the studies discussed in the following the default ATLAS impact parameter based b tagging algorithm (*IP3D*) and secondary vertex based algorithm (*SV1*) are used.

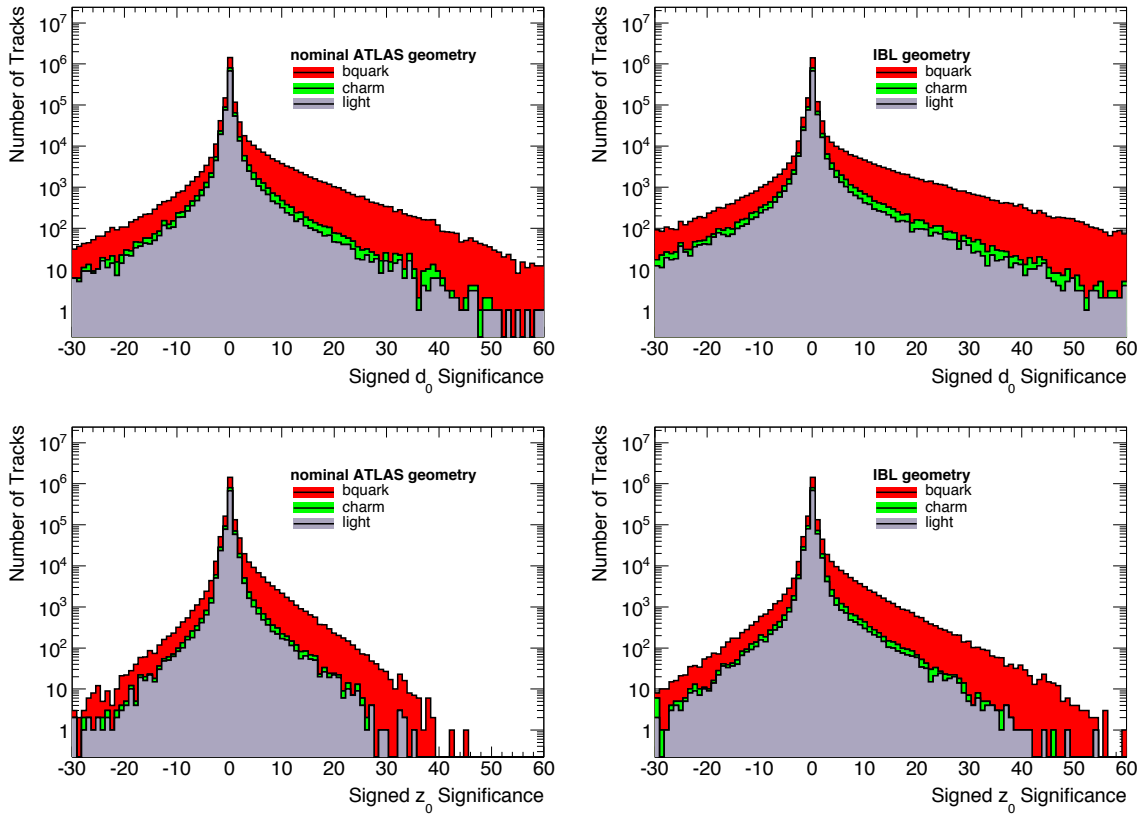


Figure 25. Transverse (top row) and longitudinal (bottom row) impact parameter significance distributions, signed w.r.t. the jet axis, for b, c and *light* jets from $t\bar{t}$ events without pileup. Compared are results with the present ID (left) and with the IBL added (right).

The *IP3D* algorithm uses the 2 dimensional distribution of the transverse ($d_0/\sigma(d_0)$) and longitudinal ($z_0/\sigma(z_0)$) impact parameter significance, taking advantage of the correlation between the two. Each impact parameter is signed on the basis that the b hadron direction should coincide with the jet direction to further discriminate tracks from b decays from tracks from the primary vertex. The b direction is estimated from the jet axis as measured in the calorimeters. Figure 25 shows the resulting d_0 and z_0 impact parameter significance distributions for b, c and *light* jets in $t\bar{t}$ events reconstructed with and without the IBL. Clear excess of tracks from b (and c) hadrons is shown in the tail at positive significance, while experimental resolution generates tracks with randomly positive and negative signed significance.

The vertex tagging algorithm *SV1* is based on an inclusive secondary vertex search, which starts from all possible 2 track combinations that lead to a vertex that is at least 2σ from the primary vertex. Vertices compatible with a V^0, conversions or hadronic interaction in the detector material are rejected before all remaining vertices in a jet are combined into one inclusive secondary vertex. For those vertices *SV*1 uses a 2 dimensional distribution of the *invariant mass* of all tracks at the vertex and the *ratio of energies* of the tracks at the vertex to all tracks in the jet to discriminate b jets. In addition, the number of candidate *2 track vertices* and the ΔR between the jet axis and the direction of the secondary vertex w.r.t. the primary vertex are used in this tagging algorithm. In $t\bar{t}$ events reconstructed with the IBL the *SV*1 algorithm finds in total 10% more vertex candidates.

For both tagging algorithms, *IP3D* and *SV1*, a likelihood ratio formalism is used to calculate a jet weight. The measured value of a discriminating variable is compared to pre-defined smoothed and normalized distributions for both the b and light jet hypotheses. Probability density functions are used for one dimensional distributions. The ratio of the b over light jet probabilities defines the track or vertex weight. The final jet weight is obtained from the sum of the logarithms of the individual track and vertex weights. In order to optimize the performance of both tagging algorithms for events reconstructed with the IBL the smoothed probability functions have been

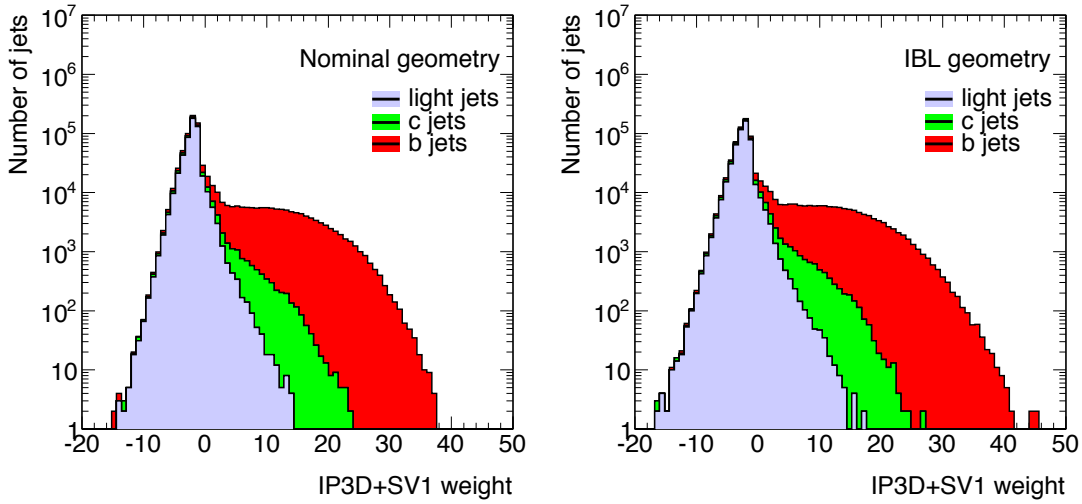


Figure 26. The distributions for the weight for the combined *IP3D+SV1* tagger for the current (left) and the detector with IBL (right) for b, c and *light* jets from $t\bar{t}$ events without pileup.

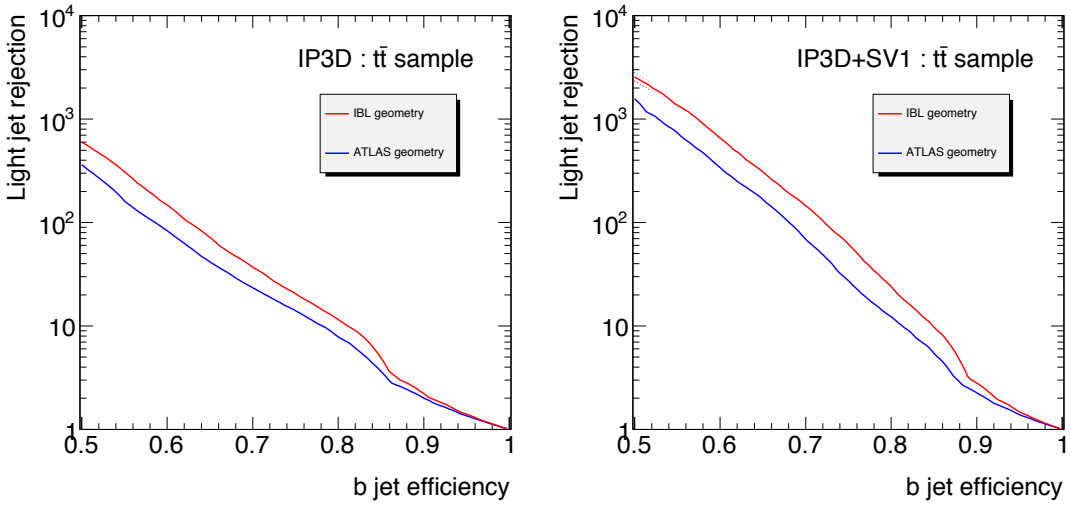


Figure 27. Rejection factor against light jets as a function of b jet efficiency for the *IP3D* tagger (right) and for the combined *IP3D+SV1* tagger (left). Compared are the results with and without IBL, using b and *light* jets from $t\bar{t}$ events without pilep.

recomputed using $t\bar{t}$ events. Figure 26 shows the weight for the combination of the *IP3D* and *SV1* tagging variables (*IP3D+SV1*). This tagger combines the rather independent information from the impact parameter measurements with information about secondary vertex properties in the jet.

Figure 27 shows the rejection factor for light jets as a function of the efficiency for b jets, obtained by varying the cut on the jet weight obtained from *IP3D* alone and from the combination of *IP3D+SV1*. The results are obtained using $t\bar{t}$ events without pileup. Jets used for this study have $p_T > 15$ GeV, $\eta < 2.5$ and at least one track associated to the vertex satisfying the b-tagging-quality criteria. As expected from the improved impact parameter resolution with IBL, a significant improvement in the rejection of light jets at fixed b efficiency is observed. Table 6 summarizes the very significant improvements in light jet rejection for the benchmark b efficiency of 60%. The c jet rejection factors using *IP3D* or *IP3D+SV1* are nearly unchanged as those taggers are tuned to reject light jets. Specialized taggers need to be developed exploring the differences in b and c hadron lifetimes and decay properties to fully benefit from the improved resolution with IBL.

2.4 Tracking, Vertexing and b Tagging Performance with IBL at Phase I Luminosities

The instantaneous luminosity during Phase I is expected to exceed 2×10^{34} cm^{-2}s^{-1}. In-time and out-of-time pileup influence the detector response in many ways as the LHC luminosity increases.

b tagger	Without IBL	With IBL	Ratio
IP3D	83 ± 1.5	147 ± 3.4	1.8
IP3D+SV1	339 ± 12	655 ± 32	1.9

Table 6. Rejection of light jets in $t\bar{t}$ events without pileup for b efficiency of 60%.

The large background from hits from pileup affects the track reconstruction (as it was discussed in Section 2.2), which consequently leads to problems for the vertex reconstruction. Additional minimum bias interactions contribute comparatively fewer jets than a high-p_T event such as $t\bar{t}$, but particles produced by the minimum bias interactions can overlay noise and other soft particles thus raising a low energy deposition above the jet reconstruction threshold or altering the reconstructed jet direction. As a consequence the analysis of high-p_T physics events is affected by the increased jet multiplicity from pileup. A detailed study of jet reconstruction in ATLAS at Phase I luminosities is beyond the scope of this document. Instead, the focus will be on the improvements from the IBL on the track and vertex reconstruction, as well as on its effects on the b tagging performance in the presence of high luminosity pileup. The latter is one of the key elements to reach the ATLAS physics goals during Phase I.

2.4.1 Stability of track reconstruction with IBL against pileup

The track reconstruction of events with high luminosity pileup suffers from the increased combinatorial background at all levels, from seeding to track finding and selection of good tracks, up to the reconstruction in the TRT at high occupancy. At the same time the number of shared clusters increases as hits from neighboring tracks merge into single larger clusters. The track reconstruction needs as well to be robust against possible detector defects (see Section 2.5) that may develop in time. An optimal working point for the track reconstruction needs to be found that limits the rate of fakes from pileup while preserving the tracking performance for b tagging and high p_T jets.

For the present detector tighter track-selection cuts in the reconstruction, requiring 9 instead of 7 silicon (Pixel, SCT) clusters and removing tracks with a hole in the Pixels, reduce the rate of additional fake tracks in events with high luminosity pileup (see Fig. 10). At the same time this induces only a modest loss in efficiency if one assumes a fully functioning detector. For a small rate of failed modules the tracking efficiency can be mostly recovered provided such inactive modules are known to the reconstruction.

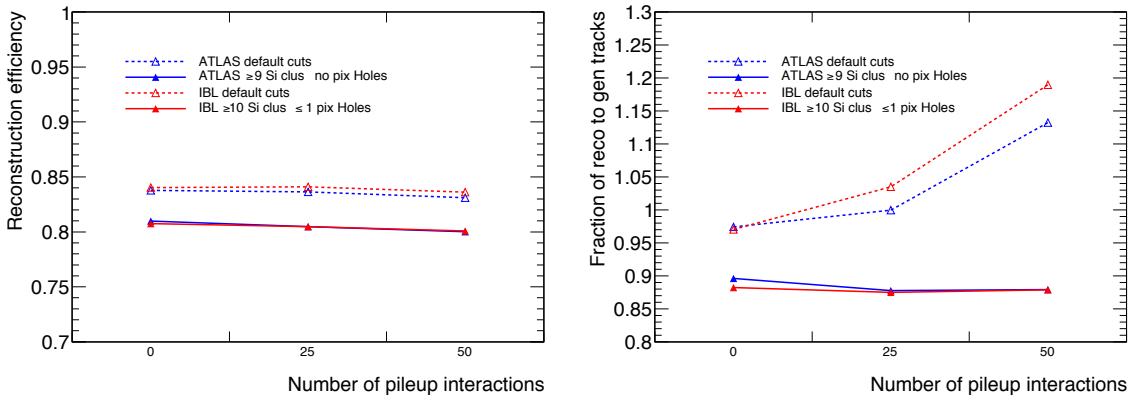


Figure 28. (left) Efficiency for reconstructing primary tracks ($p_T > 1$ GeV) with and without IBL in $t\bar{t}$ events and (right) the ratio of reconstructed tracks to generated primary particles as a function of the average number pileup events. Shown are the results for the nominal track selection and for the track selection optimized for high luminosity.

As shown in Fig. 28, using the same cut of 7 silicon clusters for events with pileup leads for the IBL to a higher rate of the reconstructed tracks, compared to the present detector. The extra track candidates are fakes due to an increased combinatorial background from the enlarged number of measurement layers and the presence of pileup. Like for the current detector, a more appropriate tighter track selection can be used for the IBL to remove the surplus in the rate of track-candidates in events with high luminosity pileup. In addition one can take advantage of the additional layer to introduce robustness in the reconstruction against e.g. FE-I3 inefficiencies in the *B*-layer at high luminosity. Figure 28 shows as well a comparison of the track reconstruction efficiency with tighter cuts for the present detector and for the detector with the IBL. For the latter a requirement of 10 silicon (IBL, Pixel, SCT) clusters on the track is used, while allowing for up to 1 Pixel hole. In addition, for both geometries with and without IBL, the p_T cut is raised from 500 MeV to 900 MeV to reduce the combinatorics from soft tracks from pileup interactions. In both cases the tighter track selection results in very similar track reconstruction efficiencies and low rates of additional tracks, almost independently of the level of pileup.

It was shown in Fig. 11 that the extra tracks accepted without the tighter track selection would lead to a larger rate of tracks with significant offsets and thus can affect the primary vertex reconstruction and *b* tagging. Therefore both track selections will be used in the following, the normal selection and the tighter selection tuned for high luminosity. The effect of detector defects on the track reconstruction performance for events with pileup is discussed in Section 2.5.2.

2.4.2 Performance of primary vertex reconstruction using IBL with pileup

The task of the primary vertex reconstruction for events with high luminosity pileup is to reliably reconstruct the interaction vertex of the physics event of interest on top of the background from soft minimum bias interactions. The working point of the *Iterative Vertex Finder* is chosen con-

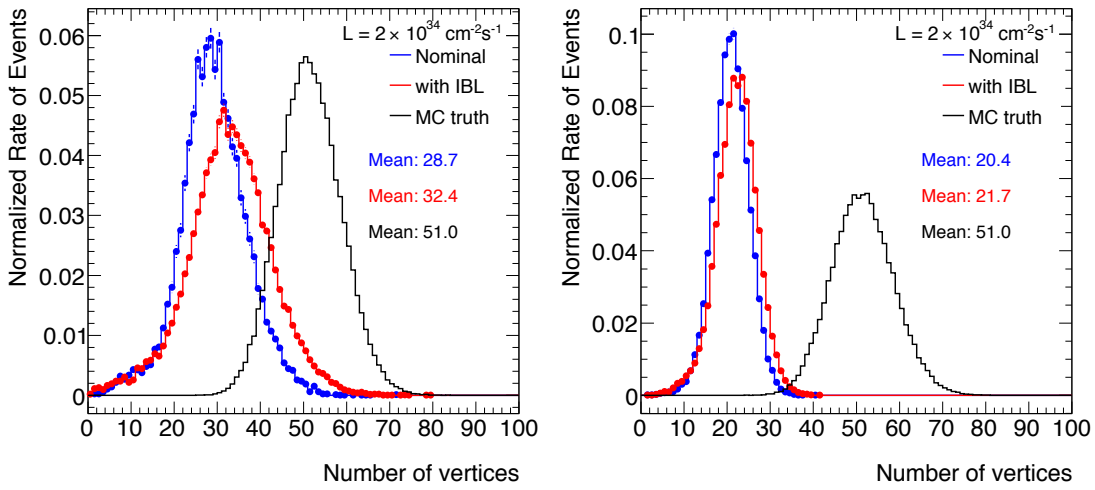


Figure 29. Number of reconstructed primary vertices for $t\bar{t}$ events with high luminosity pileup for the current ATLAS geometry and with the IBL. Shown are the results with nominal track selection (left) and with high luminosity track selection (right).

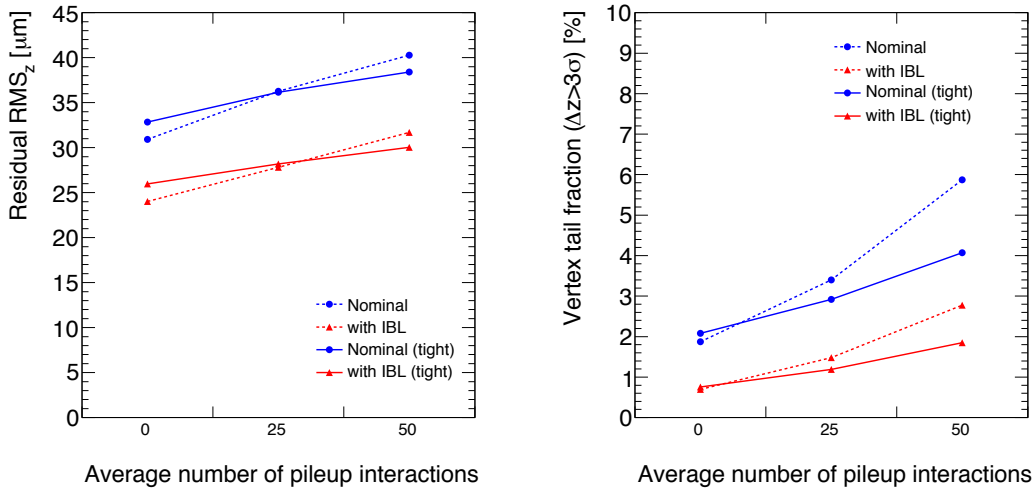


Figure 30. Primary Vertex resolution (RMS) in z for the $t\bar{t}$ interaction vertex as a function of the average number of pileup events, with and without IBL (left). Shown are the results for the nominal and high luminosity track selections. (right) shows the tail fraction of reconstructed vertices which are more than 3σ away in z from the true primary vertex.

servatively, applying a 7σ cut on a track w.r.t. an existing vertex before seeding a new vertex. This choice minimizes the rate of fake and split vertices. Figure 29 shows the rate of reconstructed primary vertices for events with $2 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$ pileup, using the normal and the high luminosity selections. In both cases the *Iterative Vertex Finder* finds more well separated primary vertices with IBL than without it, which is a direct consequence of the improved z resolution due to the IBL. Applying the high luminosity track selection significantly reduces the number of vertices found, primarily because the higher p_T cut removes soft tracks from pileup.

The primary vertex resolution for signal $t\bar{t}$ vertices in x and y depends on the rate of pileup interactions, as is shown in Fig. 30 for both track selections with beam spot constraint. The resolution in z (RMS) worsens significantly with pileup, especially for the case of the nominal track selection, while with the high luminosity track selection the dependence is reduced. This is a consequence of a rapid increase in the rate of non-gaussian tails with the nominal track selection at high rates of pileup interactions, which is shown as well in Fig. 30. Those tails are due to merging of the signal vertex with close-by vertices from pileup. With the high luminosity track selection the size of the non-gaussian tails is reduced significantly for both, with and without IBL. The improvement in resolution with IBL does not degrade with pileup and the IBL helps to reduce the tail fraction significantly.

The primary vertex position of a $t\bar{t}$ interaction, which represents a very high Q^2 process, is found by the *Iterative Vertex Finder* with very high efficiency, as shown in Fig. 31. With IBL the inefficiency for events with $2 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$ luminosity pileup is about halved, a benefit of the improved vertex resolution. With the high luminosity track selection both efficiencies are improved, because the rate of tails is reduced. The correct identification of the interesting primary interaction vertex from the set of reconstructed vertices is equally important for the physics performance.

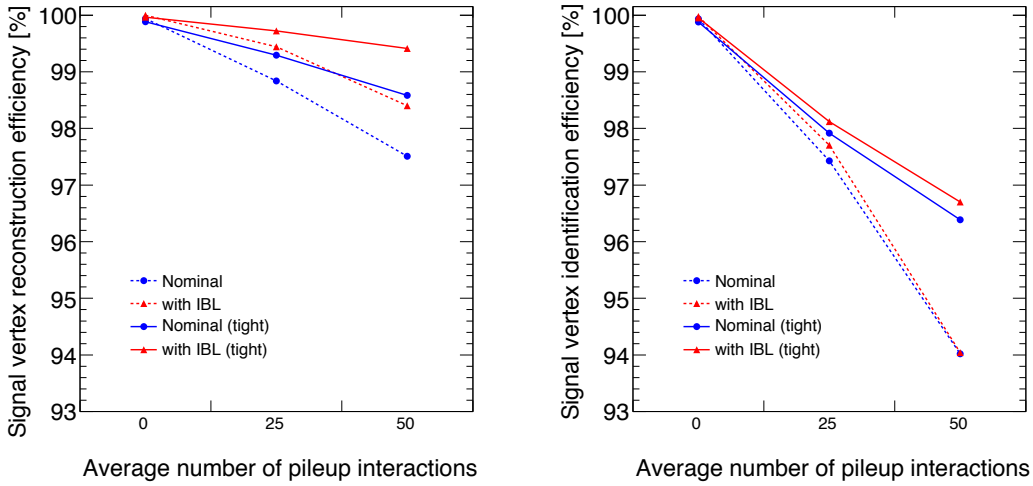


Figure 31. Efficiency for reconstructing the primary vertex (right) in $t\bar{t}$ events as a function of the average number of pileup events for $t\bar{t}$ events. Shown are the results with and without IBL for $t\bar{t}$ events with the nominal and the high luminosity track selection. (left) efficiency to identify correctly the true primary vertex using the $\sum p_T^2$ algorithm.

At low luminosity a simple $\sum p_T^2$ algorithm, based on the tracks associated to a vertex, leads to very satisfactory results (see Fig. 31). Based on this criteria the rate of misidentified vertices increases significantly with the rate of pileup interactions when applying the nominal track selection, independently of the detector layout with or without IBL. Using the high luminosity track selection reduces the rate of misidentification at a high average number of pileup events, because badly measured tracks (and fake tracks) are removed from the event.

In a physics analysis one can use other means of identifying the correct primary vertex from the set of vertices, like the identified lepton or the tracks associated to the jets from the $t\bar{t}$ decay, further increasing the vertex reconstruction efficiency. Using a Monte Carlo truth-based algorithm to identify the reconstructed primary vertex is therefore justified for the following studies, and is much simpler. It also allows the effects of the vertex reconstruction and resolution on the b tagging performance to be studied independently from the inefficiency induced by the vertex identification.

2.4.3 Performance of b tagging using IBL at Phase I luminosities

The b tagging algorithm combines the information from the track, the primary vertex and the jet reconstruction to identify b jets. The effects from pileup on track and vertex reconstruction have been discussed in the previous sections, and directly deteriorate b tagging. In addition, high-p_T physics events are affected by the increased jet multiplicity due to pileup. Additional tracks and jets from pileup interactions enter the b tagging algorithm.

Figure 32 shows for $t\bar{t}$ events with pileup the increase in the number of b-tagging-quality tracks (hence tracks with a cluster in the innermost layer and compatible with the signal primary vertex) that can be associated to any reconstructed jet. The extra tracks are either from a nearby pileup interaction close to the signal primary vertex or tracks from the signal event matching a pileup jet.

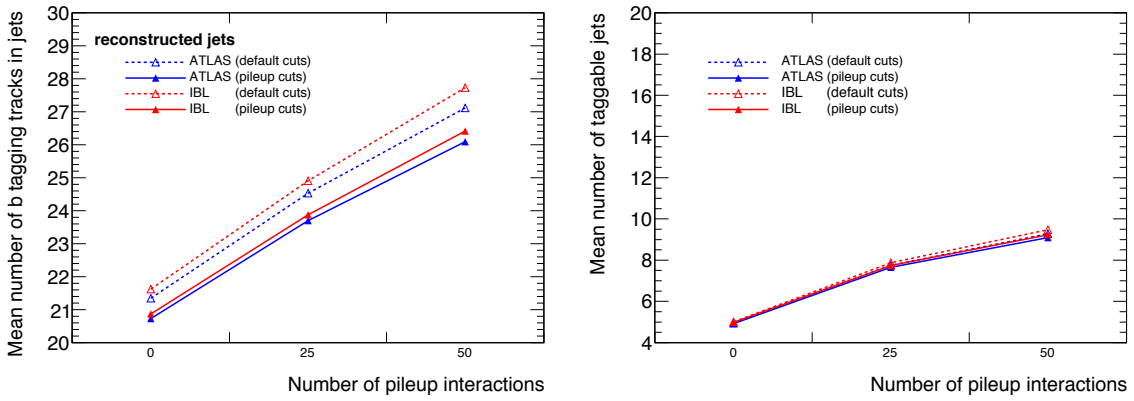


Figure 32. (left) Rate of b-tagging-quality tracks as a function of the average number of pileup events for different track selections and detector layouts. (right) Rate of jets with $p_T > 15$ GeV in $t\bar{t}$ events and jets that have at least one b-tagging-quality track and therefore are considered by the b tagging algorithm.

Figure 32 also shows the increase in the rate of reconstructed anti-Kt4 jets with $\eta < 2.5$ and at least one associated b-tagging-quality track.

Pileup jets entering the b tagging algorithm often have different properties that can be used to discriminate against them. The so called *Jet Vertex Fraction* (JVF) [27] is defined as the momentum sum of all tracks associated to the jet that match the primary vertex over the total momentum sum of all tracks in the jet. Figure 33 shows the JVF for all jets entering the b tagging algorithm in $t\bar{t}$ events with 2×10^{34} cm^{-2}s^{-1} pileup and only for those jets that are from the signal interaction. Jets from pileup have the tendency towards small values in JVF. Figure 33 shows as well the rate of b-tagging-quality tracks in jets made from Monte Carlo truth of the signal $t\bar{t}$ event. It illustrates

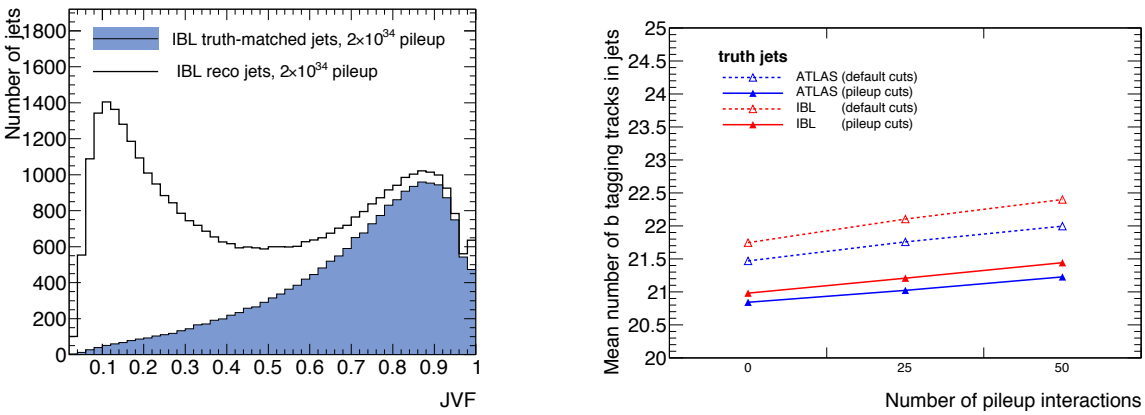


Figure 33. (left) Jet vertex fraction with IBL for all reconstructed jets (with $\eta < 2.5$, $p_T > 15$ GeV, at least one b tag quality track) in $t\bar{t}$ events with 2×10^{34}cm^{-2}s^{-1} pileup and for the jets from the $t\bar{t}$ interaction itself, selected using Monte Carlo truth. (right) Rate of b-tagging-quality tracks in jets from $t\bar{t}$ events from Monte Carlo truth as a function of the average number of pileup interactions.

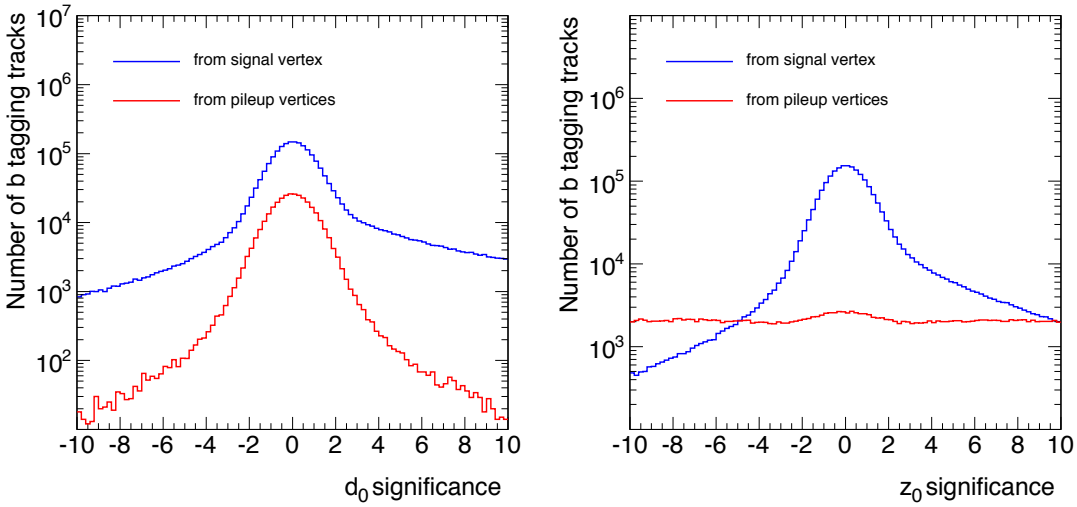


Figure 34. Impact parameter significance for b-tag-quality tracks from signal and pileup interactions, (left) for d_0 and (right) for z_0. Shown are the results for tracks with the high luminosity track selection with the IBL.

that most of the additional b-tagging-quality tracks are due to jets from pileup. Only those truth level jets are used in the following studies in order to disentangle the effects of jet production in events with pileup from the influence of the IBL on the b tagging performance.

The beam spot describes the envelope of all signal and pileup primary vertices in an event. The shape of the LHC beam spot (very narrow in the x-y plane and 4.5 cm wide in z) determines

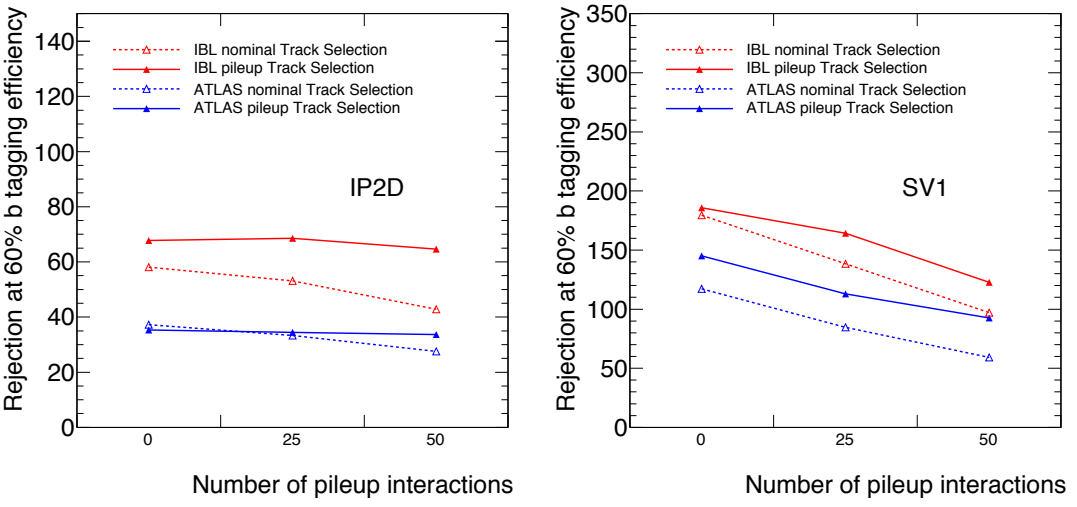


Figure 35. Light jet rejection in $t\bar{t}$ events for 60% b efficiency as a function of the average number of pileup events, on the (left) for *IP2D* and on the (right) for the vertex tagger *SV*1. Compared are the results with and without IBL. See text for details.

that pileup is likely to affect predominantly the z impact parameter significance, while leaving $R\phi$ nearly unchanged. Nearby pileup vertices in z do lead to tails in the primary vertex reconstruction, as was shown in the previous section, and are a source of additional b-tagging-quality tracks with significant z offsets. Figure 34 shows this effect in the impact parameter significance for b tag quality tracks from signal and pileup interactions, for $t\bar{t}$ events reconstructed with the IBL and using the high luminosity track selection. The d_0 significance from pileup interactions is symmetric and has the expected shape for tracks in light jets, while the z_0 significance is rather flat as expected for tracks from nearby interactions in z. A cut is added to the b tagging software to remove tracks with $|z_0/\sigma(z_0)| > 3.8$ and $|d_0/\sigma(d_0)| < 3$ that are compatible with being from a nearby pileup vertex and would otherwise affect the performance.

As is shown in Fig. 35, the tagging algorithm $IP2D$ (which contrary to $IP3D$ uses only the $R\phi$ impact parameter information) is rather stable and the performance improvement with the IBL is almost independent of the level of pileup. Shown as well is the performance of the secondary vertex based tagger $SV1$, which degrades very little with pileup and leads to an improved performance with IBL at all luminosities. In both cases, the high luminosity track selection leads to much improved results as additional fake track candidates are removed from the event.

Figure 36 shows the b tagging performance as a function of the average number of pileup interactions for $IP3D$ and $IP3D+SV1$, comparing the results with and without IBL as well as for different track selections. In all cases $IP3D$ does show some remaining degradation with an increasing level of pileup due to the effects in z from nearby pileup vertices discussed before. Still, the results with IBL are much improved. The rejection for the best b tagging algorithm $IP3D+SV1$ at 60% b efficiency with IBL and 2×10^{34} cm^{-2}s^{-1} pileup is better than the performance of the current detector at zero pileup.

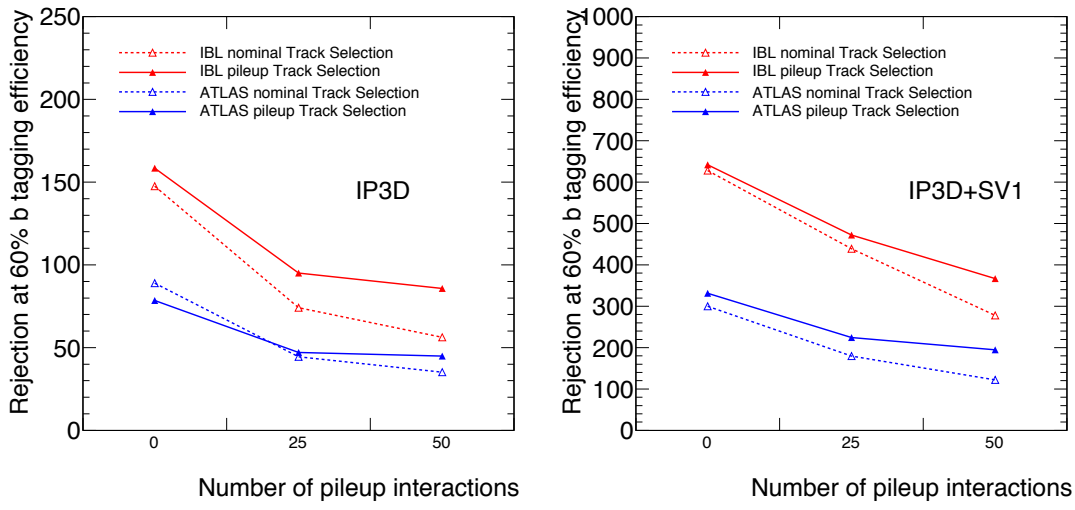


Figure 36. Light jet rejection in $t\bar{t}$ events for 60% b tagging efficiency as a function of the average number of pileup interactions, on the (left) for $IP3D$ and on the (right) for the combination of $IP3D+SV1$. Compared are the results with and without IBL. See text for details.

2.5 Effects of Detector Defects and Readout Problems on Performance with IBL

Hard failures in the *B*-layer and in the other layers will appear with time. For this study the current failed modules were taken into account for the simulation (see Table 3). As discussed in Section 1.2.2, readout inefficiencies induced by high occupancies will affect the *B*-layer more than other layers and would thereby limit the *b* tagging. Known dead modules in other layers can be handled in the reconstruction within limits, but if dead modules line up in too many layers this may lead to tracking inefficiencies even at low luminosity, because the number of layers available to constrain the tracking is reduced, causing more fakes. Different failure scenarios have been studied for events with Phase I pileup to demonstrate how the performance is recovered with the IBL.

2.5.1 Effect of detector and readout problems at low luminosity

The effect a readout problem in the Pixel detector will have on the tracking performance can e.g. be seen in the data of an ATLAS run taken in May 2010: due to a software problem in the ROD firmware more and more modules were disabled or desynchronized in the course of this run. While this bug has been immediately identified and fixed right after this run, it gives a good example of what kind of failure modes the tracking should be able to deal with.

In the left part of Fig. 37, the disabled modules in the *B*-layer towards the end of the run are shown as seen by the online monitoring. If one assumes that those disabled modules are not known to the reconstruction, then tracks would be marked as having a missing hit in the different layers. If there are too many such holes the tracks would be lost altogether. However, in this particular run the readout problems were monitored online and automatically made known to the reconstruction and therefore those tracks were mostly recovered as can be seen in the right part of Fig. 37.

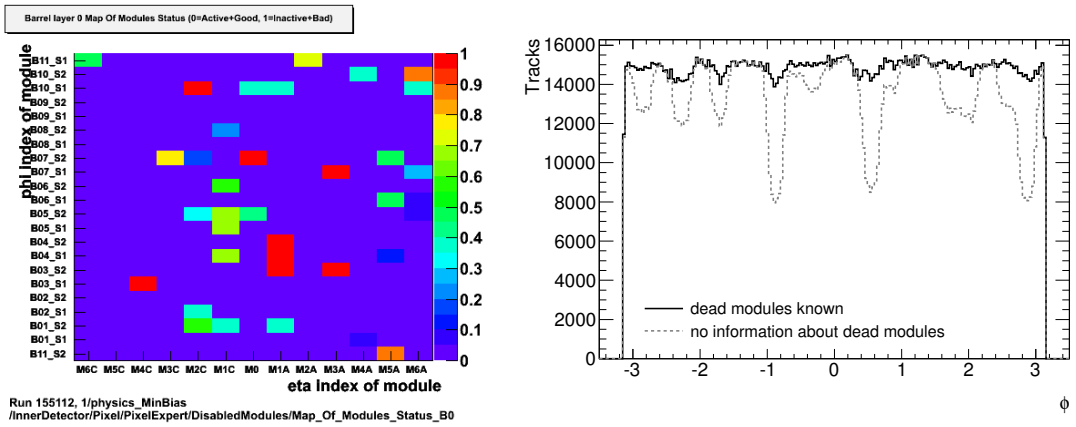


Figure 37. (Left) Histogram from the online data quality monitoring for run 155112 during which several Pixel modules were disabled, especially in the *B*-layer, due to a firmware problem in the readout. It shows the efficiency to find a hit in the *B*-layer, which illustrates which modules were off for some time. (Right) The rate of reconstructed tracks using the data from the most problematic part of the run for different track selections. Shown are the reconstructed tracks allowing for the known inactive modules, selecting tracks with cluster in the *B*-layer or hitting a known inactive *B*-layer module. Shown as well are the results if one just requires a *B*-layer cluster and does not correct for the inactive modules in the reconstruction. This particular problem in the readout was immediately identified and fixed right after the run.

While the tracks themselves can be recovered due to the knowledge of dead detector modules, the loss in resolution, especially the loss in impact parameter resolution in case of dead *B*-layer modules, cannot be recovered as the multiple scattering effects in the extrapolation from layer 1 through the *B*-layer to the interaction point completely dominates the impact parameter resolution. This automatically leads to the loss of *b* tagging performance. It should be noted that the inefficiencies discussed in section 1.2.2, will not result in modules with completely missing data, like in this case, but only is losses of a fraction of the hits. Not knowing where hits are lost, the reconstruction software will not be able to recover the affected tracks.

2.5.2 Simulation studies of detector and readout problems at Phase I luminosities

The effects of three different failure scenarios have been studied using dedicated simulation samples:

- Loss of 10% of the clusters in the *B*-layer e.g. due to FE-I3 inefficiencies at high luminosity
- A catastrophic failure of the full *B*-layer as a worse case scenario

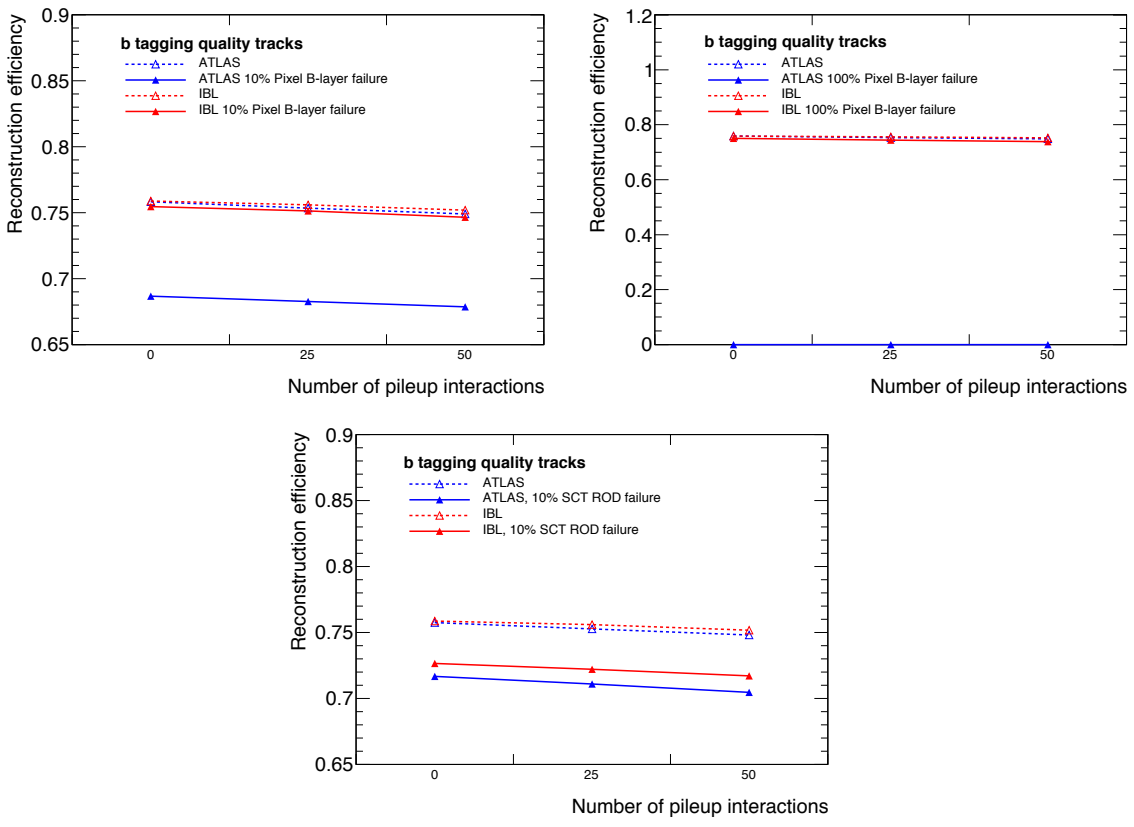


Figure 38. Efficiency for *b*-tagging-quality tracks with and without additional detector defects. Shown are the results for the 3 failure scenarios as a function of the average number of pileup events, for a detector with and without IBL.

- Disabling 10% of the Readout Drivers in the SCT in order to emulate the effects of known dead modules in several layers in certain $\eta - \phi$ regions

The first scenario leads to holes in the track reconstruction with IBL, as the efficiency of the detector is degraded. For the two other scenarios the dead modules are known and the reconstruction can attempt to allow for the failures by adapting the cuts.

Figure 38 shows for all three scenarios the efficiency to reconstruct *b*-tagging-quality tracks as a function of the average number of pileup events. Compared are the results for the detector with and without the IBL using the high luminosity track selection. Without IBL the loss in *b*-tagging-quality tracks is directly proportional to the loss in η coverage in the *B*-layer due to failures, even though the tracks may still be found. With IBL most of the inefficiency is recovered even in case of the 2nd scenario assuming a complete failure of the *B*-layer. For the 3rd scenario which assumes failures of SCT RODs the efficiency with IBL is significantly better than without, but the performance is not recovered completely as too many clusters are lost on the tracks in the affected $\eta - \phi$ regions. For such a scenario a dedicated retuning of the track reconstruction and *b* tagging software would be needed to further improve the results with IBL.

The loss in *b*-tagging-quality tracks directly enters into the *b* tagging performance, as shown in Fig. 39 for $IP3D$ and $IP3D + SV1$ using the high luminosity track selection. In all cases the reconstruction with IBL not only recovers from the failures introduced in the simulation, but exceeds the performance of the current detector without such failures. Even for a complete *B*-layer failure the IBL recovers good *b* tagging performance. Without the IBL one would need to fall back onto tracks with clusters in the second layer, at the price of a much reduced resolution and consequently some very limited light jet rejection. For the third scenario with SCT ROD failures the IBL leads as well to significant improvements, despite the residual loss in *b*-tagging-quality tracks, essentially maintaining the performance of a fully-working ATLAS detector.

2.6 Summary of the IBL Performance and Physics Studies

In this Chapter the physics impact of the IBL has been discussed. The IBL, with low mass and close to the interaction point, improves the quality of the impact parameter reconstruction for tracks and thereby the vertexing and *b* tagging performance. With the IBL the reconstruction is robust against pileup and hard failures of modules in the *B*-layer and in other silicon layers. The *b* tagging performance of ATLAS with IBL at 2×10^{34} cm^{-2}s^{-1} pileup is similar to the current detector without pileup. In all studied scenarios with detector defects the impact parameter resolution is recovered and the IBL improves the *b* tagging performance even in case of a complete *B*-layer failure. As a result, the IBL will lead to a better sensitivity of ATLAS during Phase I for signals in physics channels involving *b* jets. Work is on-going to quantify the improvement in physics performance in for example the low mass Standard Model Higgs search in the channel $WH \to b\bar{b}$.

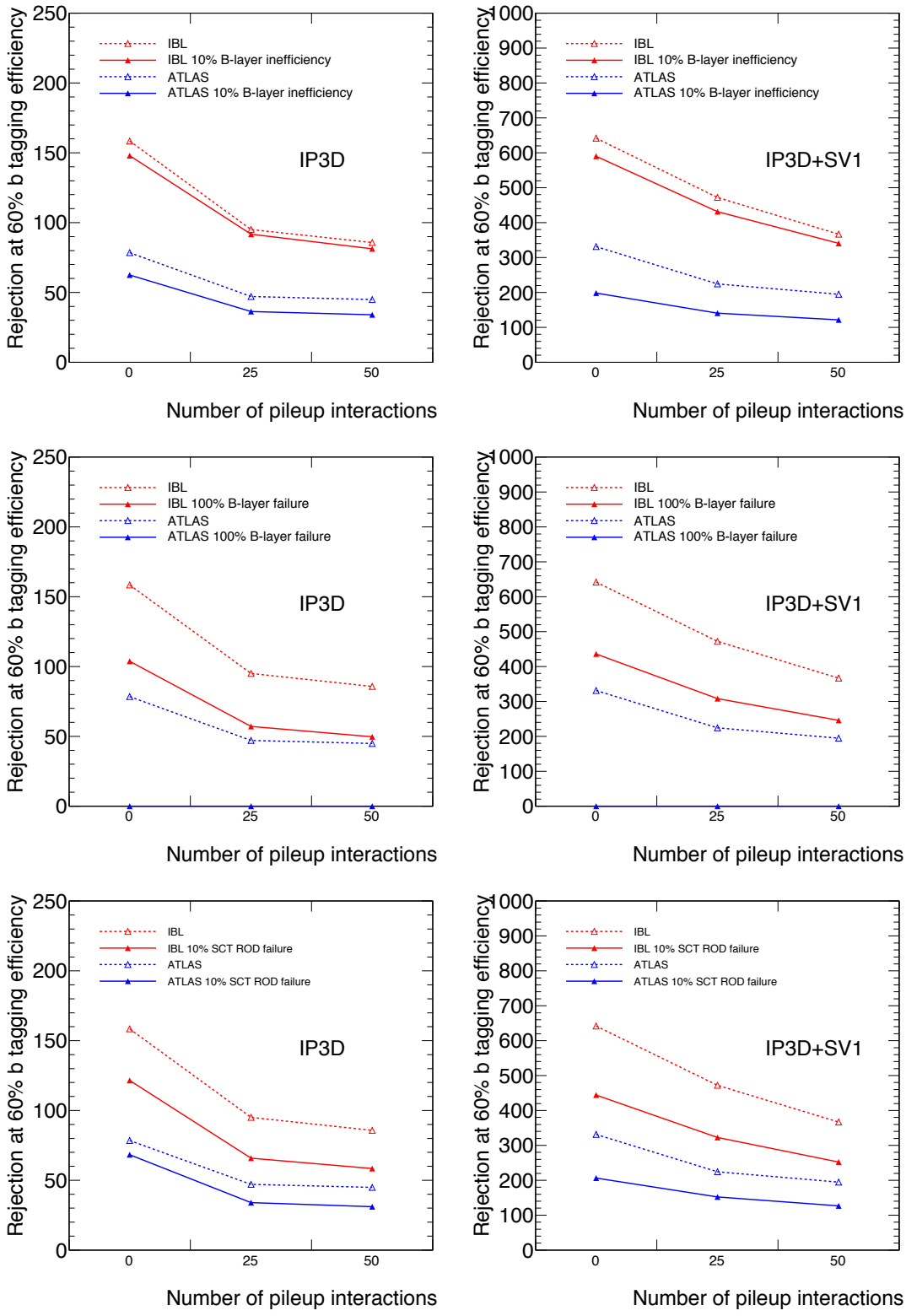


Figure 39. Light jet rejection at 60% b jet efficiency for (left) $IP3D$ and (right) $IP3D+SV1$ as a function of the average number of pileup events, for the three simulated failure scenarios for a detector with and without IBL.

3. Modules

The basic unit of the existing ATLAS Pixel detector is a module, containing 16 front end chips and one sensor. This module is a mechanical unit, a DAQ unit, and a DCS and electrical services unit. The IBL modularity will be different. The IBL module physical size depends on the still to be chosen sensor technology. There are 3 candidate sensor technologies: planar, 3D, and diamond, described later. If planar or diamond sensors are chosen the module will consist of two front end chips and one sensor (2-chip module), while if 3D sensors are chosen it will be a single chip and sensor (1-chip module). The I/O, services, and control modularities are independent of sensor technology. The DAQ unit always consists of two front end chips, with common clock and control inputs and two data outputs. This matches the mechanical module in case of planar or diamond sensors, but not in the case of 3D. For simplicity, the rest of this chapter will assume a 2-chip module, which is both a mechanical and a DAQ unit. Fig. 40 compares the footprints of the present detector and IBL modules on the same scale. The IBL power and sensor bias services unit consists of two modules in parallel.

The IBL module format is based on a new integrated circuit (FE-I4), described later. The front end chip used in the present detector (FE-I3 [28]) was excluded from IBL use due to two fundamental problems: the hit rate capability and radiation hardness are not high enough, and the active fraction of the footprint is too small to build a compact layer with high geometric acceptance. FE-I4 was designed to address these problems as well as to advance towards lower cost pixel detectors needed for an eventual replacement of the complete ID (outside the scope of this document). The 90% active footprint of FE-I4 (compared to 70% for FE-I3) enables the design of a low radial profile layer, as required for IBL. Additionally, the FE-I4 is a self contained electrical unit requiring no module control chip to attain the complete module functionality. The 2 chips within the IBL module are controlled in parallel (shared clock and command inputs), but each one has a dedicated data output, leading to one clock input, one command input, and 2 data outputs. In terms of number of signals, this is the same as a present detector *B*-layer module. Furthermore, the command and clock inputs are fully compatible with the present detector protocols, even if command bitcodes are slightly different. It is therefore possible to control an IBL module using present detector hardware (with software and firmware changes). The IBL module data outputs, on the other hand, must have a higher bandwidth than those used in the present *B*-layer to handle the increased hit

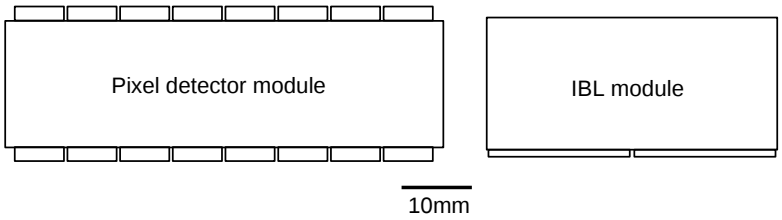


Figure 40. Comparison of footprints for present detector bare module and IBL 2-chip module on same scale. Viewed from the sensor side.

rate. These have therefore been designed with a new protocol that is not fully compatible with the existing detector DAQ hardware. However, it is still compatible with the optical hardware used in the present detector (VCSEL, pin array and related control and driver chips). These choices were made in accordance with the Upgrade System Task Force recommendations for IBL [29], which aimed to meet the bandwidth needs (including margin) with minimal development of new system components.

The module design has several technical points that must be resolved before production can begin.

- An engineering version of the FE-I4 chip must be fabricated and the design demonstrated to have the required performance.
- A sensor technology must be chosen. This choice will be based on testing of prototype modules using the FE-I4 chip.
- A low voltage powering method must be chosen. This choice will be based on system tests using prototype modules and prototype power supplies.
- A final chip thickness for bump bonded modules must be determined. Chip thickness is the main technical problem for bump bonding.

These points will be addressed in the appropriate subsections of this chapter.

3.1 Requirements

The performance requirements for the module stem from the overall requirements of the detector, while other requirements are due to constraints imposed by the mechanics, services, assembly and handling, installation, etc. The basic requirements are listed in Table 7. Mechanical dimensions will be given in the sensor Section.

Requirement	Value	Conditions
NIEL dose tolerance	5×10^{15} n_{eq}/cm^2	-
Ionizing dose tolerance	250 Mrad	-
SEU rate at peak luminosity	<1/(24 hrs)	For global configuration
Hit efficiency in active area*	>97%	Single MIP
r-ϕ MIP resolution*	<10 μm	2T B-field, 15° incidence
Z MIP resolution*	72 μm	Digital resolution for 250 μm pixel
Hit loss at peak luminosity*	<1%	Including SEU effects
As-built bad pixels	<0.2%	Sensor + Bump + Chip defects
Maximum bias voltage	1000 V	-
Radiation thickness	<500 μm Si equiv.	-

Table 7. Basic performance requirements for the IBL module; (*) after full dose and SEU is Single Event Upset.

3.2 Sensors

The IBL module outline using 2-chip assemblies is shown in Fig. 41. In the case 3D sensors are chosen, the same outline can be produced using 1-chip assemblies with narrow sensor edges as shown in Fig. 42. Active edge technology to produce such narrow edges is a feature of 3D sensors. There is no shingling in z of the IBL modules due to the extreme radial space constraints, and this results in slightly difference geometric acceptance for 2-chip and 1-chip assemblies. For 1-chip (2-chip) assemblies the nominal acceptance for particles normal to the beam is 98.8% (97.4%). An air gap of 100 μm (200 μm) between 1-chip (2-chip) assemblies has been assumed to take into account the higher bias voltages needed by 2-chip (planar or diamond) sensors. The 100 μm gap is considered adequate for 150 V (in a dry atmosphere) and the 200 μm gap is considered sufficient for placement of polyimide insulation film if necessary, but both must be validated with prototypes. A cross section view of the module valid for either 2-chip or 1-chip assemblies is shown in Fig. 43. For planar or diamond sensors the bias connection is made directly to the back of the sensor (opposite the chip), while for 3D sensors the bias is connected on the same side as the chip on the overhang on the left side of Fig. 43. This is the reason for the asymmetric sensor envelope allowing 1.5 mm margin on the edge away from the chip wire bond pads. Note that this is an envelope to fit into and the sensors themselves need not be asymmetric.

The three candidate sensor technologies may meet the IBL requirements with different trade-offs. The module format that has been defined can be satisfied with any of these technologies,

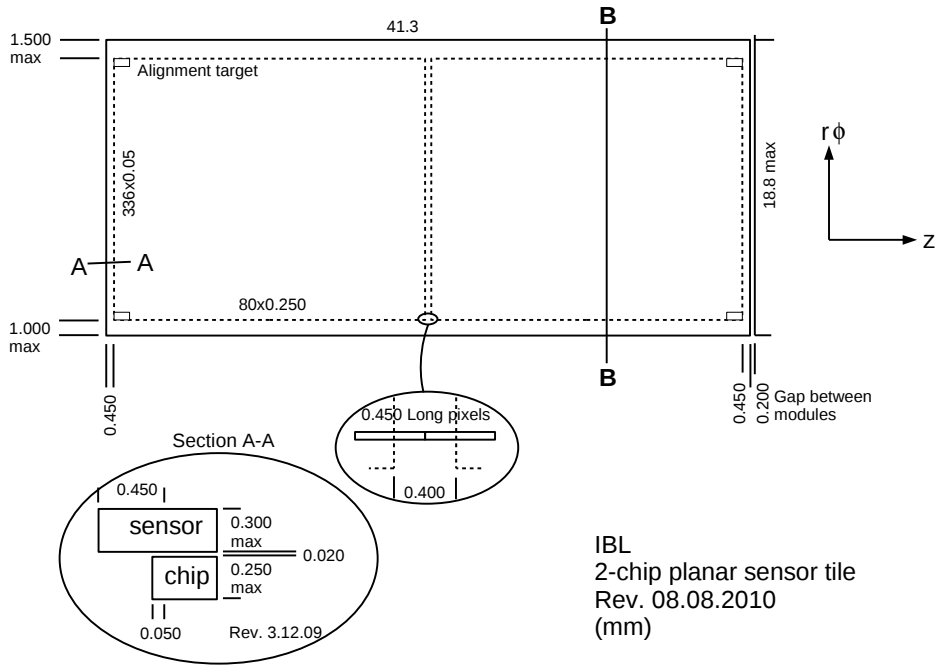


Figure 41. 2-Chip module format. The section labeled B-B is shown in a separate figure.

thus permitting some independence of the overall design. However, the two parameters operating temperature and bias voltage are different for each technology and have serious implications for the rest of the system. Planar sensors require the lowest temperature and high bias voltage, but have very well understood manufacturing sources, mechanical properties, relatively low cost, and high yield. 3-D sensors require the lowest bias voltage, intermediate operating temperature, and achieve the highest acceptance due to active edges, but their manufacturability with high yield and good uniformity must be demonstrated. Diamond sensors require the least cooling and have similar bias voltage requirements to planar sensors, but their manufacturability with high yield, moderate cost, and good uniformity must all be demonstrated. Each sensor candidate technology is described in more detail in the subsections below.

In addition to the above features, each sensor technology has different signal characteristics that influence the following performance measures:

- the charge collected per minimum ionizing particle (MIP) and evolution with irradiation,
- the width of the distribution of MIP charge collection,
- the operating voltage,
- the single pixel noise (due to capacitive load and leakage current presented to the amplifier),
- the minimum operable threshold.

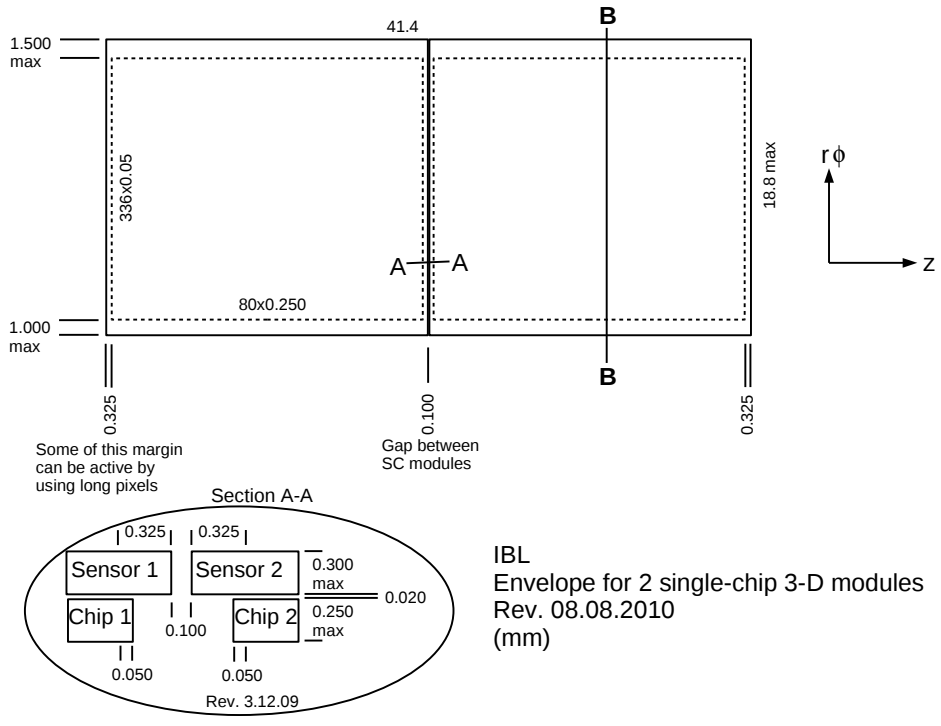
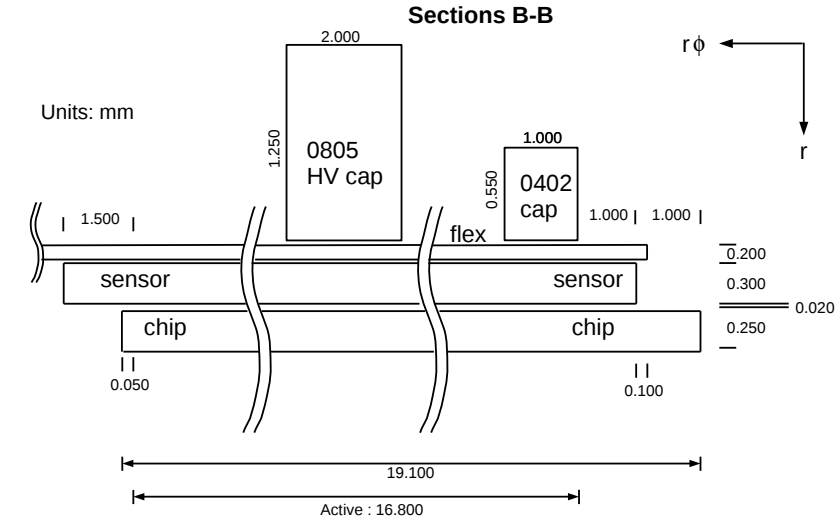


Figure 42. 1-Chip module format. The section labeled B-B is shown in a separate figure.

Present knowledge of these quantities has been obtained using the FE-I3 readout chip. The IBL sensor technology choice must be informed by new measurements using the FE-I4 chip, before and after irradiation to the required dose (Table 7). Note that the charge collection is not by itself a decisive figure of merit. A critical factor in making a sensor choice will be the electrical performance with the FE-I4 chip. In particular, the minimum stable operating threshold is considered to be the parameter that determines the required charge at end of life, and not the single pixel noise. However, the minimum stable threshold can not be determined with confidence from simulations, because it depends on coherent effects within the chip plus sensor assembly. A full system analog simulation has not been technically possible, and the exact impedance network presented by an irradiated, bump bonded sensor is not well known. Measurements of FE-I4 chip prototype modules are therefore essential for all sensor technologies. Any specific concerns particular to a given technology are discussed in the corresponding subsections below.

3.2.1 Planar sensors

The main technical concerns for planar sensors are radiation tolerance with limited bias voltage, the width of inactive edges, and the low operating temperature needed to avoid thermal runaway of the leakage current. The sensors of the present Pixel detector have an inactive margin of 1 mm and can be operated up to 700 V reverse bias at -10°C, which allows them to maintain acceptable charge collection efficiency and leakage current up to NIEL doses approaching $2 \times 10^{15} n_{eq}/cm^2$. In contrast, the IBL sensors must have at most 450 μm inactive edge and operate up to $5 \times 10^{15} n_{eq}/cm^2$ with the possibility to cool down below -25°C, but with a voltage not exceeding 1000 V. This

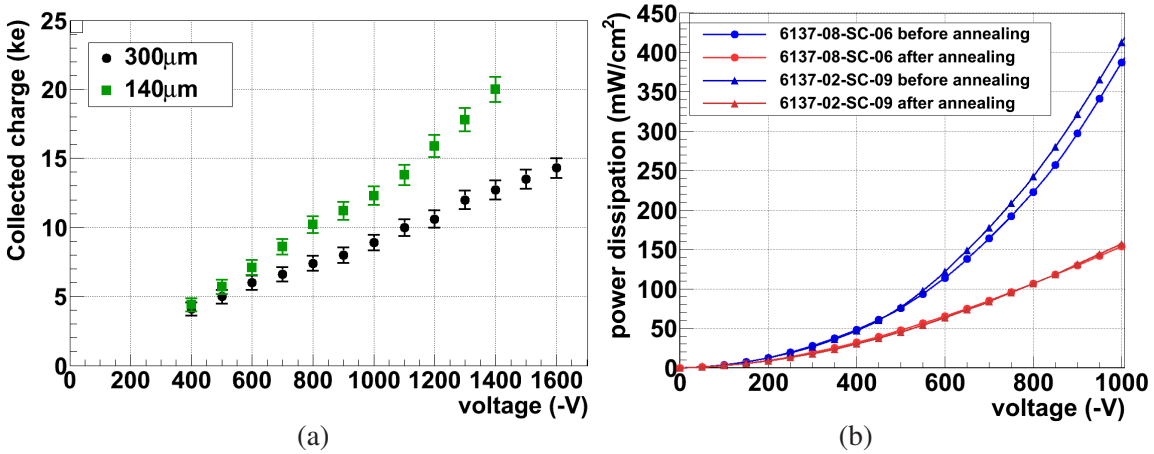


Notes:
* These are envelopes; nominal thicknesses are less
* Potential bows and thinning tolerance are included
* Flex includes glue interfaces
* Location of HV cap is not critical
* Wire bonds (not shown) are to the right of 0402 cap.

Figure 43. Cross section view of module assembly.

voltage limit is imposed by the IBL services and power requirements. There has been significant progress in planar sensor design since the present detector was built and it seems that these goals are achievable, but, as for all sensor candidates, the performance with the FE-I4 chip must be demonstrated. The reference planar sensor design is n-on-n as for the present detector, but with fewer guard rings yet sufficient voltage tolerance. There is also a modified n-on-n design to achieve even smaller inactive margins, as well as an n-on-p design. The n-on-p design has an additional burden to overcome, which is the isolation of the bias voltage from the readout chip, since the bias guard rings must be on the same side as the bump bonds. The very recent development of charge multiplication to increase the signal after heavy irradiation is not yet well enough understood to exploit for IBL, and generally requires higher bias voltage than allowed for IBL (for the baseline sensor thickness). Thus it is not proposed to rely on charge multiplication for IBL.

The charge collection of microstrip sensors after high dose hadron irradiation has been studied by the RD50 collaboration[30, 31]. Results obtained with miniature n-in-p strip detectors (1x1 cm^2) using 40 MHz clock rate electronics have shown that, even after 2×10^{16} n_{eq}/cm^2, planar sensors can yield signal charge equal or even greater than before irradiation [30, 32]. Reproducible and consistent results have been obtained with similar sensors made by different manufacturers over a wide range of radiation dose and voltage [31, 33]. The key feature to achieve large signal charge after heavy irradiation is high electric field, which for typical thickness sensors means operating at bias voltages well in excess of 1000 V. On the other hand, thin detectors can achieve high electric field with lower voltages. For fixed bias voltage (below 1000 V) after heavy irradiation, higher charge collection than for 300 μm thick silicon has indeed been confirmed with n-in-p sensors of 140 μm thickness [34] and 75 μm active thickness [35]. The charge collected can exceed the pre-irradiation value if the electric field is high enough. Fig. 44 (a) shows the measured charge after the IBL design fluence of 5×10^{15} n_{eq}/cm^2 in planar strip sensors [32], while Fig. 45 shows the charge collection vs. dose in 300 μm sensors limited to 900 V bias. It can be seen that, without relying on either kV range bias or thin sensors, the MIP signal charge for planar sensors after 5×10^{15} n_{eq}/cm^2 is approximately 8000 electrons.



(a) (b)

Figure 44. (a) Collected charge from ^{90}Sr after 5×10^{15} n_{eq}/cm^2 measured with planar strip sensors of different thickness. (b) Power dissipation per cm^2 at -15°C after 4×10^{15} n_{eq}/cm^2 measured with n-in-n FE-I3 single chip sensors from the ATLAS Pixel production.

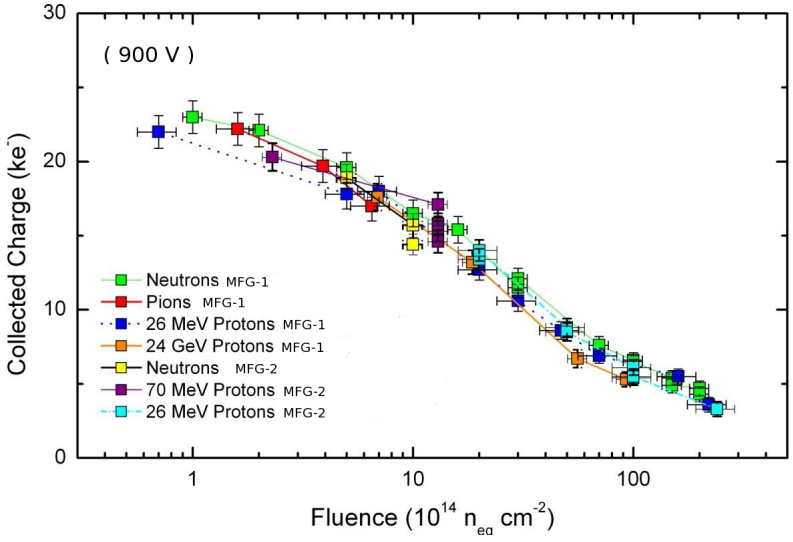


Figure 45. Collected charge as a function of fluence up to 2×10^{16} n_{eq}/cm^2 with planar sensors made by two different manufacturers (MFG), biased to 900 V.

The continued increase in charge collection with bias voltage after heavy irradiation is thought to be due to a charge multiplication mechanism [32, 36] triggered by a high electric field near the junction of irradiated devices. This mechanism is not yet fully understood, but investigations with Transient Current Technique (TCT) [36] and "edge-TCT" [37] indicate that the charge amplification is occurring in the vicinity of the n+ implantation. Investigations are ongoing using the TCAD semiconductor simulation package to reproduce the electric field depth profile of the irradiated devices, with initial results that qualitatively confirm the idea that impact ionization near the junction is responsible for the enhancement of the signal [38]. One can see in Fig. 44 (a) that the signal measured with 140 μm thick devices exceeds (by a factor of ≈ 2) the maximum signal measured by a non-irradiated sensor of the same thickness. These detectors have been operated at high voltage (in the charge multiplication regime) for several hours to a few days without breakdown, provided that the temperature can be maintained at -20 to -25 °C. The signal amplitude seen at a given dose and voltage is reproducible, independent of manufacturer, and insensitive to electrode geometry, but the homogeneity of the multiplication effect on larger area devices and long-term stability are still under study. Evidence of multiplication has also been reported for 3D sensors at high dose [39].

Apart from the signal, the increasing leakage current with irradiation and resulting power dissipation are main concerns for planar sensors. The leakage current is proportional to the received fluence, but can be reduced by annealing and by cold operation. About a 40% reduction of the reverse current is found after annealing an irradiated sensor for 80 days at 20 °C, while about a factor of two reduction is obtained with every 7 °C decrease in temperature [40]. The annealing of the sensor at 20 °C (or higher, up to 80 °C) does not adversely affect the collected charge, even after high irradiation doses. The annealing does affect the sensor capacitance vs. voltage and hence the traditional "depletion voltage" determined from a C-V curve, but it has been found that signal collection (for a given bias voltage) does not degrade with annealing. The signal as a function of time at 20 °C after irradiation is higher than the value measured just at the end of the irradiation for at least 1000 days [41]. The IBL cooling specification allows up to 200 mW/cm^2 sensor power

dissipation at -15 °C. Fig. 44 (b) shows the power dissipation per unit area of an ATLAS Single Chip sensor after irradiation to 4×10^{15} n_{eq}/cm^2 followed by annealing. The power dissipation specification can be met after leakage current annealing. More detailed leakage current annealing studies can be found in [40].

Different choices of planar sensor bulk material are possible for IBL. Studies within RD50 have shown [42] that for a radiation environment which is dominated by charged hadrons, magnetic Czochralski (MCz) bulk material shows no advantage over diffusion oxygenated float-zone Silicon (DOFZ). Beyond fluences of 10^{15} n_{eq}/cm^2, also the choice of n-bulk or p-bulk silicon appears to equally justified. n-in-p Sensors have the advantage of requiring only single-sided processing during production which facilitates the production of thin DOFZ wafers with the handling-wafer method [43]. With standard production methods, a larger number of vendors is available. Besides, the detectors can be operated underdepleted already before irradiation. But an important drawback of p-bulk sensors is the presence of a large fraction of the bias voltage (≈50% of up to 1000 V) on the pixel side of the sensor, which requires a reliable and radiation-hard passivation to prevent discharges towards the FE-chip.

To enable staves without shingling and still acceptable geometric efficiency, the inactive edges of the sensors have to be as narrow as possible up to the maximum 450 μm allowed for IBL. Taking into account inactive edge requirements and material choices, the following sensor variants are being studied for qualification:

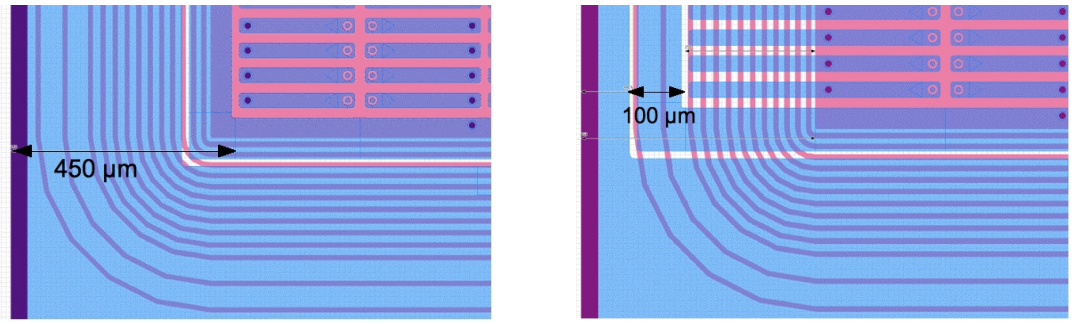
1. conservative n-in-n design

   The conservative n-in-n design (Fig. 46 (a)) tries to stay as close as possible to the proven and reliable present ATLAS Pixel detector [28]. To obey the 450 μm inactive edge limit, the number of guard rings (on the back side of the wafer) had to be reduced from 16 to 13. It has been shown experimentally that it is sufficient to typically exceed the full depletion voltage by more than 150 V. The pixel length in z has been reduced to match the new 250 μm pixel cell length of the FE-I4. The main advantage of the conservative design is that it uses sensors which are already known to work, while still fulfilling all requirements for IBL.

2. slim-edge n-in-n design

   As the guard rings of the n-in-n design are located on the p-side of the sensor, it is possible to shift them inwards, leading to a partial overlap with the outermost pixel row as shown in Fig. 46 (b). This will of course distort the field close to the sensor's edge, but from simulations [44] the effect is expected to be negligible after irradiation as most of the charge is collected directly beneath the pixel implant due to partial depletion and trapping. Before irradiation, some charge will be lost due to the weaker and distorted field, but the signal-to-threshold ratio before irradiation contains more than enough headroom to accommodate this. The edge efficiency of this design still has to be investigated in test beam studies, but an inactive edge of only 100 μm would lower the geometric inefficiency to 0.5% while still being quite conservative with respect to the overall sensor design which is identical to the conservative design.

3. thin n-in-p design

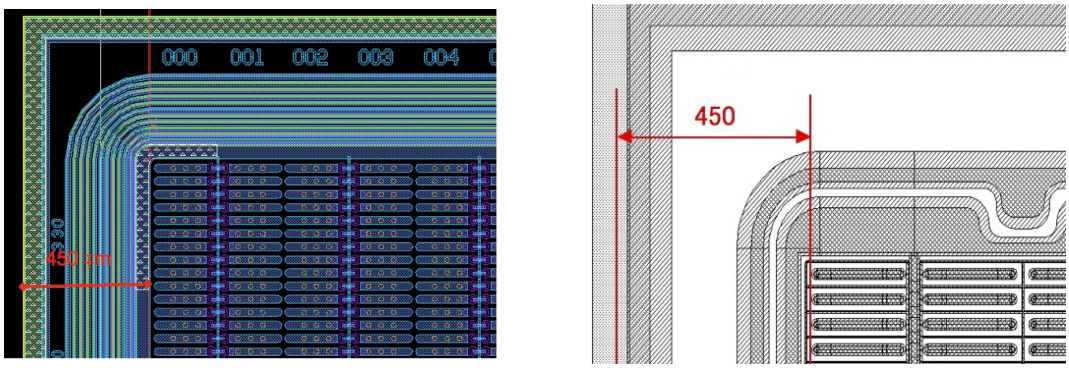


(a) (b)

Figure 46. (a) Conservative n-in-n sensor design. The number of guard rings is reduced from 16 (current ATLAS Pixel sensor) to 13 to obey the limit of 450 μm inactive edge. (b) Slim-edge n-in-n sensor design. To keep a fixed length of the sensor tile of 41.3 mm, the outermost pixel implants on the front side are extended to a length of 500 μm.

Sensors made on p-bulk are an interesting alternative to the more complex double-sided n-bulk sensors. n-in-p Sensors are the technology choice for future strip upgrades replacing the hole-collecting p-in-n technology which performs poorly after high fluences. Therefore, significant R&D is taking place within the ATLAS Upgrade environment in collaboration with leading semiconductor manufacturers from which an n-in-p IBL design would benefit. Performance before irradiation measured with the FE-I3 chip is equal to n-in-n sensors. The main drawback, HV discharges into the FE-chip, is addressed by an additional BCB (Benzocyclobutene) polymer layer on top of the standard oxide and nitride passivation layers. While tests before irradiation showed sufficient protection, the behavior after irradiation is still being investigated.

n-in-p sensors offer, in addition to the larger number of vendors capable of producing them,



(a) (b)

Figure 47. (a) n-in-p Sensor design. The number of guard rings is chosen to obey the limit of 450 μm inactive edge. (b) n-in-p sensor design. As in present strip sensor productions, only one guard ring is applied. The necessary safety margin around it has been verified to be compatible with the limit of a 450 μm inactive edge.

easier methods for thinning. A handle wafer based method has been developed to process n-in-p wafers down to thicknesses of below 100 μm, at which point the handle wafer is anisotropically etched to yield a mechanical frame of minimal radiation length [43, 45]. Good performance before and after irradiation has been achieved on FE-I3 compatible pixel sensors produced with this technique, having active thicknesses of 75 μm and 150 μm [46]. The feasibility of a 450 μm wide inactive edge has also been demonstrated with the sensors from reference [46] (Fig. 47 (a)). A parallel effort is also developing thin sensors using a conventional process (no handle wafer) to produce 6" wafers with thicknesses down to 150 μm. Such reduced thicknesses would – as shown in Fig. 44 – lead to an increased collected charge after irradiation. The reduced sensor thickness would also lower the IBL material budget, improving the ATLAS tracking performance.

While all results obtained with the current ATLAS Pixel sensors ought to describe the sensor behavior well up to a fluence of 2×10^{15} n_{eq}/cm^2, test beam investigations of the new sensors irradiated to 5×10^{15} n_{eq}/cm^2 are foreseen at DESY and CERN. Cluster sizes and spatial resolution are not expected to deviate significantly from results obtained with ATLAS Pixel sensors at 2×10^{15} n_{eq}/cm^2.

3.2.2 3D sensors

The main concerns specific to 3D sensors are manufacturability and uniformity of a production run. Different ways to manufacture 3D sensors have been investigated and the two proposed for IBL are called “double sided” [47, 48] and single sided “full3D” with active edges [49, 50] (Fig. 48). Prototypes have been successfully manufactured using both methods and characterized with FE-I3 readout electronics in particle beams over the past three years with and without magnetic fields [51, 52]. Test samples were characterized after the fluence levels expected for the IBL and also beyond. A common wafer floor plan has been defined for all FE-I4 compatible prototypes, to facilitate bump-bonding, alignment and comparative testing.

The electrode configuration chosen for the IBL is called “2E-250”. This means that 2 n-type electrodes will be used to span the 250 μm readout pitch [53]. This configuration has an inter-electrode distance of $\approx 70\,\mu$m and, for IBL-level radiation dose, is a good compromise between signal efficiency (charge collection) and capacitive noise increases with the number of electrodes per pixel. The selection was motivated by measurements using the FE-I3 readout chip. A summary of these measurements is reported in Table 8 where the threshold, in-time threshold and required signal (double the in-time threshold to take into account charge sharing among two adjacent pixels) are reported for different electrode configurations. The in-time threshold is the minimum signal that can produce a hit in the same 25 ns time window as all larger signals. The relationship between threshold and in-time threshold may not be the same with the FE-I4 chip. The 3E-400 configuration shown in Table 8 (in bold) corresponds to the 2E-250 configuration chosen for the IBL due to the larger readout pitch of the FE-I3 chip. It should be noted that the electrode diameter influences the capacitance and therefore the noise budget of the system. The measured devices have a diameter of $\approx 14\,\mu$m. This diameter directly depends upon the equipment used to etch the electrode holes. The new generation of etchers that will be used for IBL production can perform the same operation

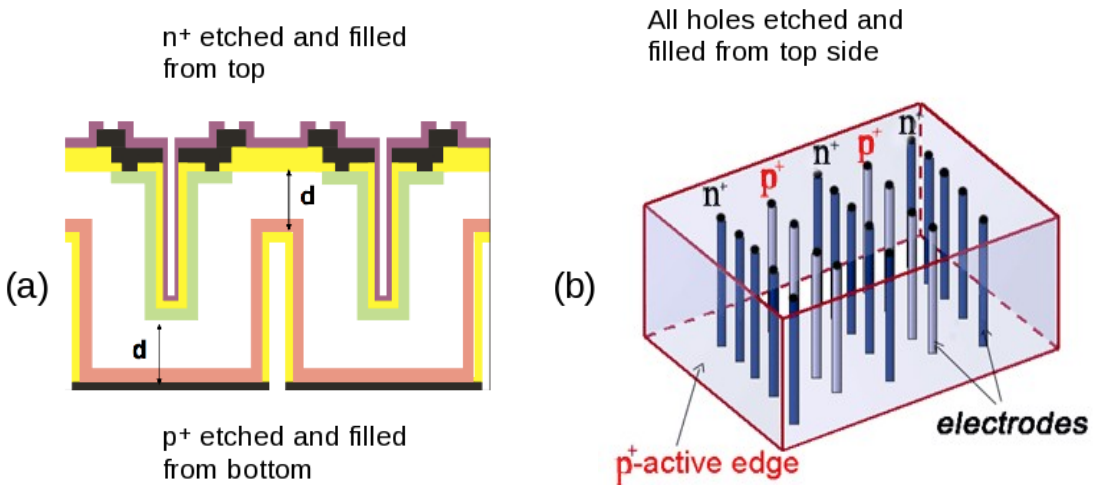


Figure 48. Double sided process (a) and full 3D with active edges (b). An un-etched distance d of order 20 μm is needed in (a) for mechanical integrity.

while keeping the electrode diameter smaller with consequent smaller capacitance and noise. The reported measurements are therefore worst cases and are expected to improve in the near future.

An important difference between full3D and double sided 3D is the presence of active edges. Active edges are difficult to incorporate in the double sided 3D processing. However, simulations and data have shown that the edge current can be completely controlled by the insertion of "guard fence" columns [54]. The perimeter occupied by guard fences has a width of approximately 200 μm. The bias voltage, in the case of full 3D with active edges, is currently applied on the same side of the readout electrodes. This is possible by using a bias tab placed along the column width on the opposite edge of the readout. The alternative would be opening a via from the front to the back side of the sensor.

The signal efficiency was measured independently for full3D and double sided 3D sensors with infra-red photons and minimum ionizing particles. A compilation of the results is presented in Fig. 49 (a), while (b) shows the expected most probable signal for a substrate thickness of 230 μm. After 5×10^{15} n/cm^2 the most probable signal is $\approx$ 12000 electrons.

The charge collection distance in 3D sensors is relatively short, and this has important system

Configuration	Bare threshold (e^-)	In-time threshold (e^-)	Required signal (e^-)
2E-400	2500	4300	8600
3E-400	**3200**	**6000**	**12000**
4E-400	3200	6540	13800

Table 8. Threshold, in-time threshold and required signal (double the in-time threshold to take into account charge sharing among two adjacent pixels) of full3D sensors with different configurations and electrode diameter of $\approx$ 14 μm. In bold, the 3E FE-I3 measurement which geometrically corresponds to 2E FE-I4.

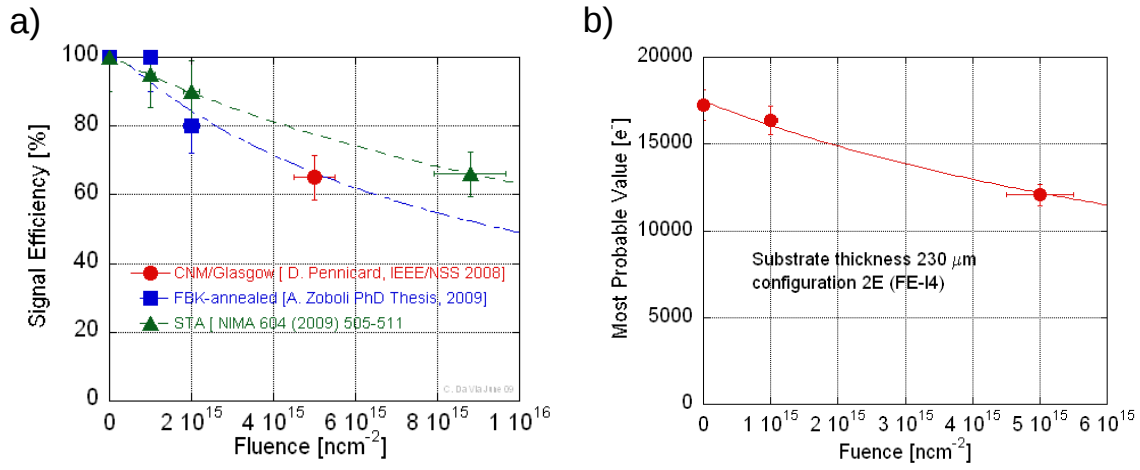


Figure 49. (a) Signal efficiency of double sided (CNM and FBK data points) and full3D (STA data points) 3E-400 electrode configurations. (b) Expected most probable signal for a 2E-250 electrode configuration, based on an averaged signal efficiency value from left. All sensors are 230 μm thick.

consequences. The required bias voltage is low even in over-depletion, both before and after irradiation and, as a consequence, the power dissipation is reduced, as can be seen in Fig. 50 [55, 56]. This is possible because the leakage current is dominated by the radiation induced deep generation centers. In 3D sensors the charge collection distance, which corresponds to the n-p inter-electrode spacing, is decoupled from the signal generation distance, given by the substrate thickness for charged particles traversing at near normal incidence. One can thus choose the electrode spac-

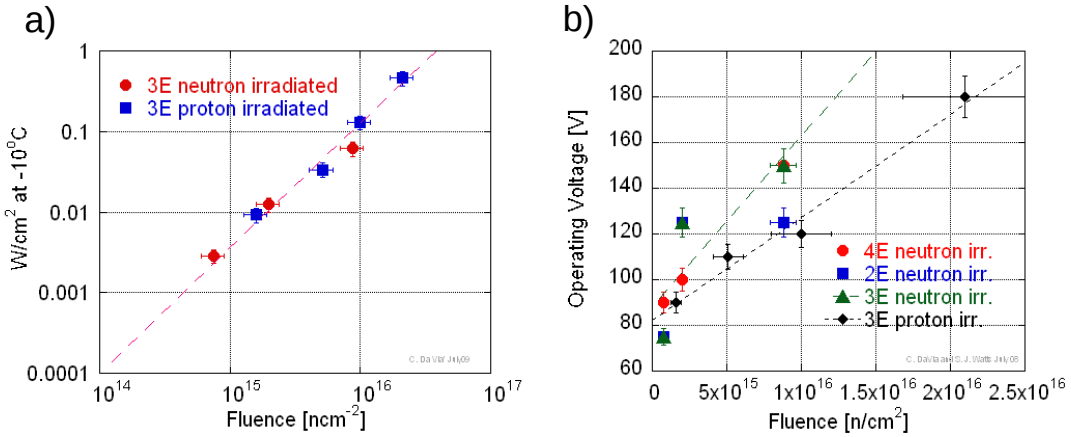


Figure 50. (a) Power dissipation per unit area measured at -10°C both for neutron and proton irradiated samples. (b) Operational bias voltages versus fluence. All sensors are 230 μm thick.

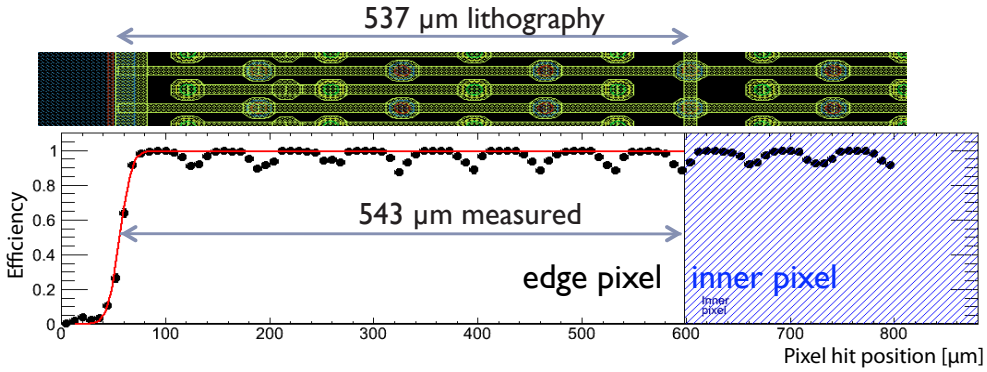


Figure 51. Active edge response of a full3D pixel assembly to normal incidence particles (points). Results were the same with and without magnetic field. The efficiency is high up to the physical edge of the sensor, with dips visible for both field and signal electrodes. A sensor layout image showing the electrode lithography is shown at the top. Structures visible in the layout from left to right are: active edge, signal electrodes, bias electrodes, bump bond pads, signal electrodes, etc.

ing for the desired charge collection efficiency and/or bias voltage after irradiation, and separately choose the thickness for a given total generated charge per particle. In Fig. 50 (b) it can be seen that the 3E-400 operating bias voltages (which include over-depletion to maximize signal amplitude) are: 80 V before irradiation, 120 V at 5×10^{15} n/cm^2, and 180 V at 2×10^{16} n/cm^2 fluence. Fig. 50 (a) shows the power dissipation per unit area versus fluence at -10°C. A compilation of the plotted data is collected in Table 9 [57].

The possibility to minimize its dead area at the edge to less than a few microns is one of the strong features of full3D sensors. This is achieved by etching a trench around the detector's physical edge and by diffusing in dopants to make an electrode. Recent test beam data, shown in Fig. 51, were collected with and without magnetic field. The minimum measured distance from the physical edge to a hit on beam tracks was $6 \pm 10\,\mu$m (the quoted error is the single hit position resolution). This value confirms previous test beam and x-ray measurements.

Bulk type	**Fluence** [n_{eq}/cm^2]	**Bias voltage (V_{OP})** [V]	**Current at -10 °C** [μA]	**Power density** [mW/cm^2]
n	7.5×10^{14}	75 (75)	0.3	3
n	2.0×10^{15}	100 (125)	1.0	12
p	1.6×10^{15}	50 (90)	1.5	9
p	5.1×10^{15}	70 (110)	3.9	34
n	8.8×10^{15}	150 (150)	3.3	61
p	1.0×10^{16}	120 (120)	8.8	130
p	2.1×10^{16}	150 (180)	2.5	463

Table 9. Compilation of current, voltage and power dissipation data at different fluence and configurations of 3E-400 full3D data. Operational voltages, defined as voltages to obtain the maximum signal, are reported in parenthesis. All currents are after annealing.

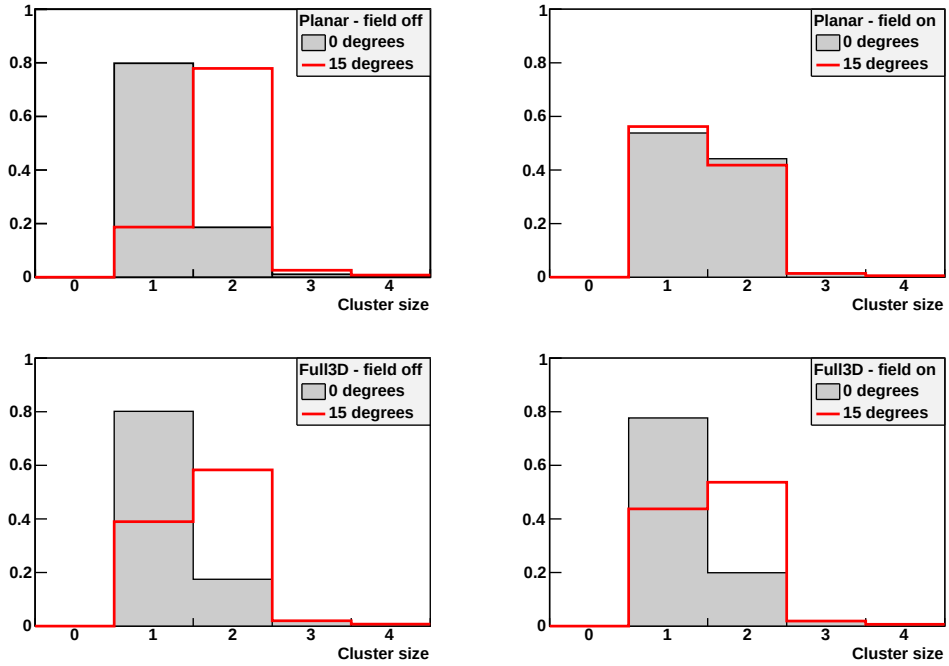


Figure 52. Distribution of cluster size at normal and 15° nominal incidence angles with and without 1.6 T magnetic field of a full3D with active edges device compared to an ATLAS prototype planar sensor. All distributions are normalized to unit area. Tilt is about an axis parallel to the beam. See later table for precise values and angles.

The efficiency for minimum ionizing particles was measured in several test beams between 2006 and 2009 at different angles using bump-bonded sensors to the FE-I3 readout electronics chips. The center of each electrode is not fully active, as can be seen from the dips in the plateau of Fig. 51, and affects the sensor efficiency for particles at normal incidence. This slight efficiency

Sensor	Incidence (0=normal)	Efficiency (%)		Charge sharing (%)		Resolution [μm]	
		B=0	B=1.6T	B=0	B=1.6T	B=0	B=1.6T
Planar	0	99.9	100.0	20.4	45.4	13.8	10.2
	13.8°	100.0	100.0	78.9	42.6	9.7	10.4
Full3D	0	96.7	96.5	20.2	23.0	14.3	13.9
	11.4°	99.9	99.9	60.3	55.7	10.8	9.8
Double sided 3D A	0	98.4	98.3	12.2	14.6	15.4	14.8
	14.1°	99.8	99.5	62.1	52.5	11.9	11.3
Double sided 3D B	0	99.2	99.1	17.6	18.9	14.0	13.5
	12.0°	99.8	99.9	51.6	47.1	10.4	9.7

Table 10. Resolution and efficiency measured at different incidence angles with and without magnetic field. Two different double sided 3D prototypes (from different manufacturers) are shown. Tilt angles are about an axis parallel to the beam direction.

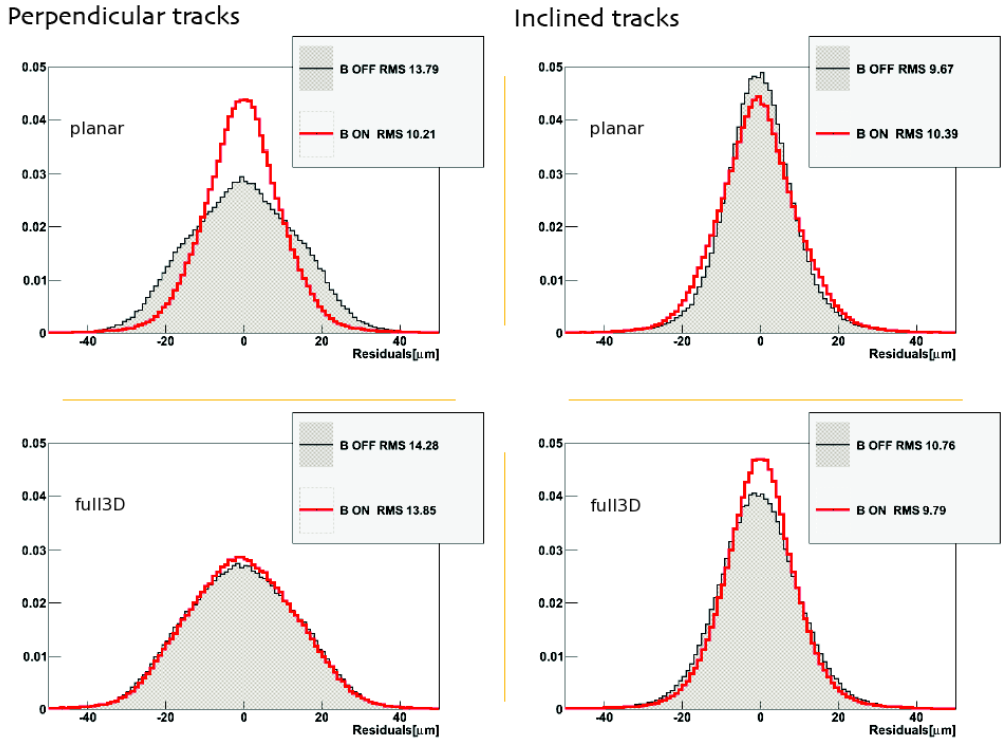


Figure 53. Track residual distribution at 15° and normal beam incidence with and without 1.6 T magnetic field of a full3D active edge device compared to an ATLAS prototype planar sensor.

loss due to the electrodes is a disadvantage of 3D technology, but this is not a problem for the IBL module geometry in which the modules are tilted at 14°. In addition, promising results on electrode efficiency improvement have been recently obtained by using different electrode doping processes. The measured efficiency with a 3200 e^- threshold is 96% at normal incidence and 99.9% at 15° from normal.

Because of the electrode geometry, charge sharing is less pronounced in 3D sensors and the Lorenz force does not distort charge collection. These facts have important implications for the cluster size, with less charge leaking to adjacent pixels, resulting in a larger minimum signal size which can lead to improved position resolution in the case of interest: tilted sensors in a magnetic field. Fig. 52 compares cluster sizes of 3D sensors with a planar reference, from test beam data. Fig. 53 compares position residuals of 3D sensors with a planar reference, using analog charge interpolation for 2 or more pixel clusters. A summary of the hit efficiency, charge sharing and resolution data of full3D and double sided 3D sensors with and without magnetic field at different angles is reported in Table 10. A sample of the currently installed planar pixel geometry is used as a reference.

3.2.3 Diamond sensors

The main concerns specific to diamond sensors are signal size, cost and uniform production in the quantities needed for IBL. Diamond detectors are attractive because they have very low leakage current and can be operated at room temperature with no thermal runaway problems. These advan-

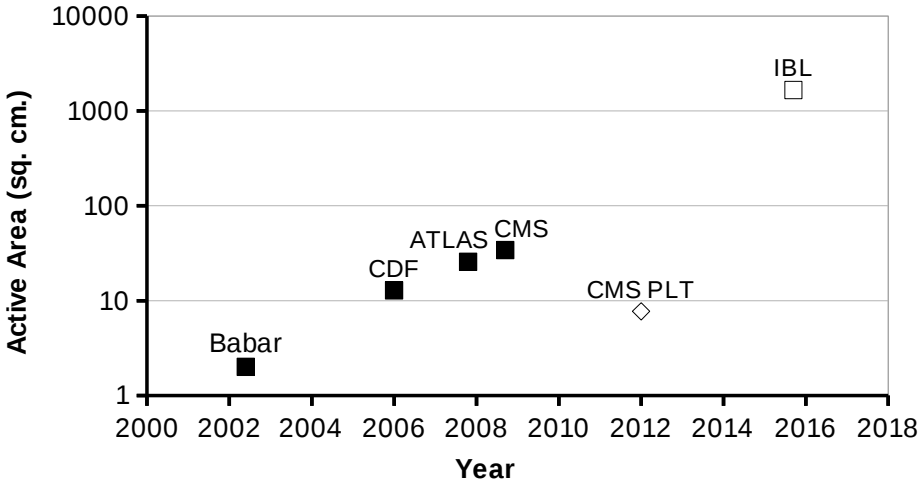


Figure 54. Total surface area of diamond sensors in HEP experiments as a function of their installation date. Future dates (open symbols) are estimates. The CMS PLT (Pixel Luminosity Telescope) uses single crystal diamond while the rest are CVD diamond.

tages come at the cost of just under half the signal size of silicon for equal thickness, which makes the ability of the readout chip to operate with low thresholds of particular importance to the use of diamond detectors. However, the single pixel noise is also smaller in diamond than in silicon, because the dielectric constant is smaller (and hence so is the pixel capacitance), and this may in turn help lower threshold operation.

Diamond sensors (not necessarily with pixellated readout) are/were used in BaBar, CDF, and all four of the LHC experiments. The IBL exceeds by almost 2 orders of magnitude the area of these previously produced diamond detectors (Fig. 54). While this is clearly a challenge, a key development during the last few years is that polycrystalline CVD (chemical vapor deposition) material has become readily available in the form of large wafers. The charge collection distance [1] is a measure of the quality of material and for present state of the art pCVD wafers it can exceed 300 μm, leading to an average of 11 000 electron-hole pairs per minimum ionizing particle (before irradiation). Single source supply of pCVD diamond wafers has been a concern until recently, but multiple, competing sources are now available. Therefore, it is expected that the price of sensor-grade diamond material will quickly decrease as industrial production becomes more widespread. The price of sensors is a consideration for the IBL, even if not a technical one. At present, pCVD wafers from two manufacturers are under study and the material is of similar quality to the 4-wafer sample described below.

The assembly methods and operation of diamond pixel modules of present ATLAS Pixel detector format have been demonstrated in small quantities. Fig. 55 shows four pCVD wafers studied over the last two years with as-grown collection distances between 280 μm and 315 μm. These wafers have been used to produce 5 full-size FE-I3 modules (fully compatible with the present

[1] The charge collection distance is the carrier lifetime times the average velocity.

Pixel detector) [58]. Three of them have been tested in beams and irradiated to different doses up to 10^{15} 24 GeV protons/cm^2. These modules show single pixel noise $\approx 140\,e^-$, and can be operated at thresholds <1500 e^- with >97% of the pixels responding to hits. Detailed measurements are on-going.

Detailed results on diamond performance come from studies performed by the RD42 and ATLAS-DPix collaborations on single-chip size samples. High quality pCVD diamond has been irradiated to a fluence of 1.8×10^{16} 24 GeV protons/cm^2 [59]. After irradiation an electric field of 1 V/μm yields 27% of the un-irradiated charge for MIPs, while an electric field of 2 V/μm yields 33%. These signal pulse heights, as well as results from intermediate fluences are shown in Fig. 56. At the IBL design fluence (5×10^{15} protons/cm^2) pCVD diamond sensors retain 66% of their initial charge at an electric field of 1 V/μm. At 2 V/μm (which would correspond to the 1400V operating voltage for IBL), the post irradiation signal corresponds to an average charge of 7,500 electrons and a most-probable charge of 5 500 electrons, independent of operating temperature.

After irradiation, beyond $10^{16}\,n_{eq}/cm^2$, the leakage currents in these sensors are less than 10 nA/cm^2. Thus the power consumption of diamond sensors operating at room temperature is well below the 200 μW/cm^2 IBL specification, providing considerable operating margin for the cooling system, potentially allowing a further reduction in the cooling/support structure in the IBL if diamond sensors are chosen.

Diamond sensors not only have low leakage current but also lower capacitance than similar silicon sensors due to the lower dielectric constant of diamond. Both these properties lead to lower noise. No change in the noise has been seen after irradiation. From Fig. 56 we therefore expect an S/N of almost 50 after 5×10^{15}. This should allow for a comfortable operating margin even after the full IBL exposure, as long as the FE-I4 chip is capable of stable operation at low threshold, as already pointed out.

Fig. 57 shows the spatial resolution for a single-crystal diamond pixel 1-chip module in a test beam at the CERN SpS [60]. Data from pCVD modules is still being analyzed. The figure shows the hit residuals in the long (a) and short (b) pixel directions. The open histogram shows the residuals for the single highest pulse-height pixel, while the cross-hatched histograms show the effect of interpolating between neighboring hit pixels using the pulse-height information. The latter show better than 10 μm resolution for 50 μm pixels, while the former shows digital resolution for single pixel readout, the expected operating mode of these devices after exposure to modest doses in the IBL.

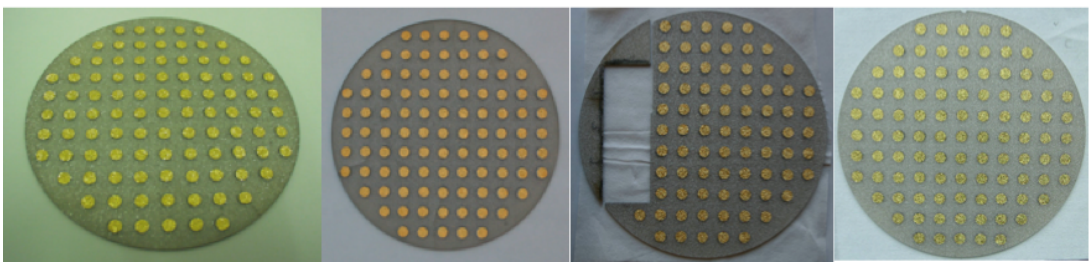


Figure 55. Four 12-cm diameter wafers of sensor grade pCVD diamond material.

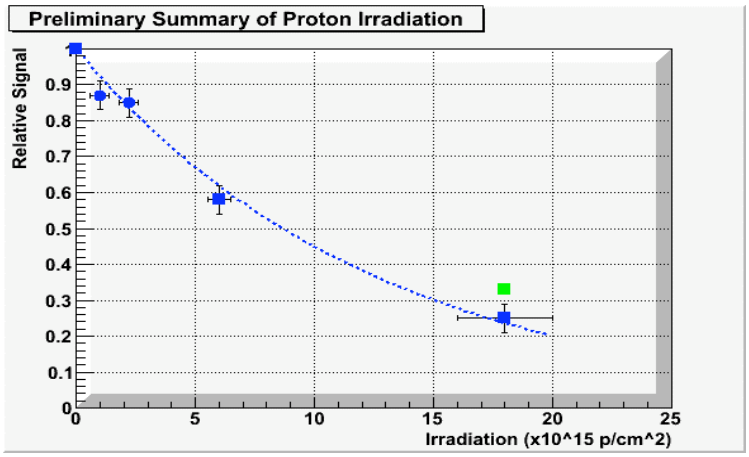


Figure 56. Relative signal charge for pCVD diamond sensors measured as a function of 24-GeV proton fluence. These sensors had 11 000 electron average signal prior to irradiation with 1 V/μm bias field. After the full irradiation the sensor was also operated at 2 V/μm.

3.3 Electronics

The FE-I4 integrated circuit [61, 62, 63, 6] contains readout circuitry for 26 880 hybrid pixels arranged in 80 columns on 250 μm pitch by 336 rows on 50 μm pitch. It is designed in a 130 nm feature size bulk CMOS process. Sensors must be DC coupled to FE-I4 with negative charge collection. Each pixel contains an independent, free running amplification stage with adjustable shaping, followed by a discriminator with independently adjustable threshold. The chip keeps track of the firing time of each discriminator as well as the time over threshold (TOT) with 4-bit resolution, in counts of an externally supplied clock, nominally 40 MHz. Information from all

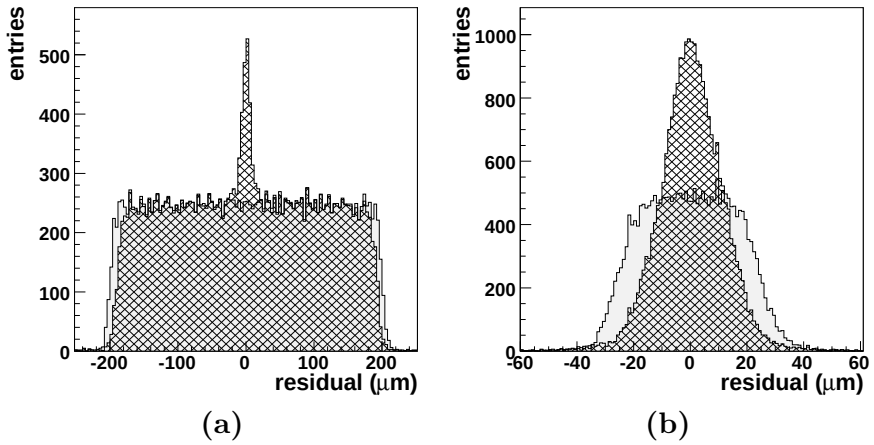


Figure 57. Position resolution for (a) long and (b) short direction of the pixel. The open histograms show the single pixel resolution while the cross-hatched histograms show the result of charge interpolation using pulse height information. Interpolation only leads to an improvement for tracks crossing two pixels, which rarely happened in the long direction (a), leading to the sharp peak over a single pixel "background".

discriminator firings is kept in the chip for a latency interval, programmable up to 256 cycles of the external clock. Within this latency interval, the information can be retrieved by supplying a trigger. The data output is serial over a current-balanced pair (similar to LVDS). The primary output mode is 8b/10b encoded with 160 Mb/s rate. The FE-I4 is controlled by a serial LVDS input synchronized by the external clock. No further I/O connections are required for regular operation, but several others are supported for testing.

As already mentioned, the main technical concerns for FE-I4 are the demonstration of design performance through an engineering version of the full chip, the power delivery scheme (discussed later) and the measurement of the minimum stable operating threshold for each sensor technology, a property that cannot be simulated with present tools. If the minimum stable threshold turns out to be high with little dependence on the sensor type, this will favor the sensor technology with the largest signal (Planar, 3D), whereas if a stable threshold even lower than with the present detector can be achieved, this will boost the viability of diamond as a sensor candidate.

The main performance specifications are summarized in Table 11. They have evolved from a combination of the existing detector properties, the expected higher rate and radiation needs for a new ATLAS inner layer at smaller radius, and compatibility with existing systems as well support for continued evolution.

3.3.1 System requirements for power

In the present Pixel detector power is supplied point-to-point to each module from voltage regulators at PP2 (via cables of approximately 10 m length). The output voltage of PP2 is limited to the maximum voltage that the module can tolerate without sustaining damage. This makes damage due to over-voltage impossible no matter what current transients are present. However, this configuration requires the voltage drop in the 10 m cable run from PP2 to the modules to be less than the difference between the maximum safe voltage and the operating voltage. Because FE-I4 is designed with a smaller feature size technology than the present detector, this voltage difference is significantly smaller, and the direct power option used in the present detector is ruled out due to the lack of space for wires to achieve a low enough voltage drop. Power conditioning within the chip will therefore be needed in addition to regulators at PP2. Several such power conditioning options have been designed and will be investigated with the engineering version of the FE-I4 chip (called FE-I4A). FE-I4A contains two stand-alone linear-shunt regulators that can be externally wired for any purpose, as well as a divide-by-two DC-DC converter, also to be externally wired. While the linear-shunt regulators permit implementation of serial power, the plan for IBL is to implement direct (parallel) power as the system is small and there is flexibility in the efficiency of the external services. This has the advantage of backwards compatibility with existing counting room power supplies and PP2 regulator components.

There are 3 possible ways to power an FE-I4A chip. The simplest is to directly connect external supplies to the power pins- the option that has been ruled out for IBL because the required volume of services along the beam pipe would be too great. the second option is to supply power through the linear regulators. These are designed to operate up to 2.5 V input voltage, and so by using them one can accept higher voltage drops and therefore smaller cables. This is a simple way to reduce cable volume without changing the current that must be supplied. Additionally, by using regulators one can implement power-up sequencing of internal nodes, making it straightforward to

have a single external supply, but separate analog and digital domains within the chip (the baseline for IBL). The third, more ambitious option to further reduce the required cable plant along the beam pipe is the use of the DC-DC converter, in which case only half the current must be supplied (so half the cable volume would be needed for the same voltage drop). In addition a higher voltage drop is allowed. Significantly more testing than for linear regulators alone is needed to qualify this option. The voltage ratings for the FE-I4A along with the projected current consumption are summarized in Table 12. The maximum current at maximum voltage ratings can be used to estimate the required cooling capacity.

3.3.2 Analog pixel and settings

A 2 stage amplifier configuration is used for the analog front end. The 1^{st} stage (preamp) is a straight cascode integrator with an NMOS input device operated in weak inversion. The preamp output is AC-coupled to a 2^{nd} stage folded cascode with PMOS input amplifier. The main motivation of this 2 stage system is to provide enough gain in front of the discriminator while allowing some independence in the optimization of the preamp feedback capacitor. Shaping of the input pulse is achieved by continuous reset of the preamp with a constant current feedback, which is optimized for a return to baseline of 400 ns after a -4 fC input pulse. The DC leakage current of the sensor is supplied by a leakage compensation current source in parallel with the input. The 2^{nd} stage provides only voltage gain and no shaping. The gain is approximately 60 mV/fC (6 V/V) for the first (second) stage, but the charge measurement linear range is greater than suggested by the combined 350 mV/fC total gain and the 1.4 V nominal supply voltage, thanks to the TOT digitization method used. Saturation of the 2^{nd} stage does not affect the TOT measurement (recall all shaping is done by the first stage).

The front end has been optimized to remain functional down to very low bias current. The nominal front end current for FE-I4, assuming a 400 fF sensor load, is 10 μA per pixel. For comparison, the nominal front end current for the present Pixel detector, scaled to the FE-I4 pixel size, would be 17 μA. At the nominal FE-I4 current the analog time-walk performance is worse than in FE-I3, and in fact a current close to 17 μA per pixel would be required to match the present detector analog time-walk. However, as explained in the next section, the FE-I4 region architecture compensates for the degraded analog timing performance with digital processing. For the ATLAS detector application we define a time-walk figure of merit ("overdrive") as the charge above threshold at which the delay at the discriminator output is 20 ns greater than for a maximum charge pulse. The FE-I4 overdrive at nominal current is 2000 e^-, while the present ATLAS detector operates with 1500 e^- overdrive. This nominal FE-I4 overdrive can be extracted from Fig. 58, which is the measured time delay at the discriminator output for a prototype of the FE-I4 front end circuit, after irradiation to 200 Mrad (Si).

The threshold dispersion caused by device mismatch is kept low by the AC coupling between the first and second stages. Threshold dispersion can only arise from the 2^{nd} stage and the discriminator itself. In a prototype chip with 854 pixels an un-tuned RMS dispersion of $300 \pm 100\,e^-$ equivalent input charge has been measured after 200 Mrad (Si) irradiation. The uncertainty is due to the absolute charge scale calibration, which is challenging for a test circuit with no sensor. The intrinsically low dispersion is further corrected with an independent threshold adjustment in each pixel. A 5-bit DAC with adjustable LSB size is used in order to ensure enough range to correct all

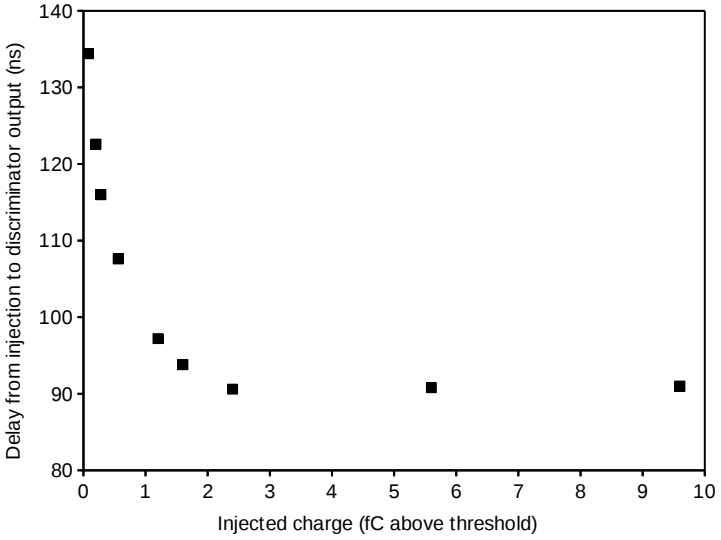


Figure 58. Measured time delay from charge injection to discriminator output in an FE-I4 front end prototype after irradiation to 200 Mrad (Si).

pixels in the large FE-I4 chip. The simulated noise with 400 fF load and 100 nA DC leakage current is under 200 e^-. Existing prototypes without a proper sensor load and leakage current provide only approximate noise information. Noise measurements in prototypes with an approximate load and no leakage current show $120 \pm 50\,e^-$ after 200 Mrad (Si), where again the uncertainty is due to the absolute charge scale.

While the minimum stable threshold can not be predicted from simulation and must be measured, a concerted attempt has been made in the design to minimize it by isolating digital activity from the substrate and reducing digital transients. In the region architecture the digital current increase caused by a new hit is small, because hit data are not transmitted outside the region. The region logic is synthesized using a commercial standard cell library that itself has no mixed signal provisions, but every digital circuit is placed over a deep implant that isolates it from the rest of the substrate. This deep implant is a conductor that acts as a buried electrosatic shield layer. All digital circuits are isolated from the substrate this way. This is expected to minimize induced noise from digital activity, which should in turn help low threshold operation.

3.3.3 Chip architecture

The outline of FE-I4 is shown in Fig. 59. The FE-I4 pixel array is organized in column pairs like the present detector's FE-I3 chip, but the readout architecture is very different. Instead of moving all hits from the pixel array to a global shared memory structure for later trigger processing, the FE-I4 double columns are further divided into 2×2 pixel regions. Each region contains 4 identical analog pixels, ending in a discriminator, and one shared memory and logic block. The digital region can store up to 5 "events". For each event, a counter clocked at 40 MHz keeps track of the

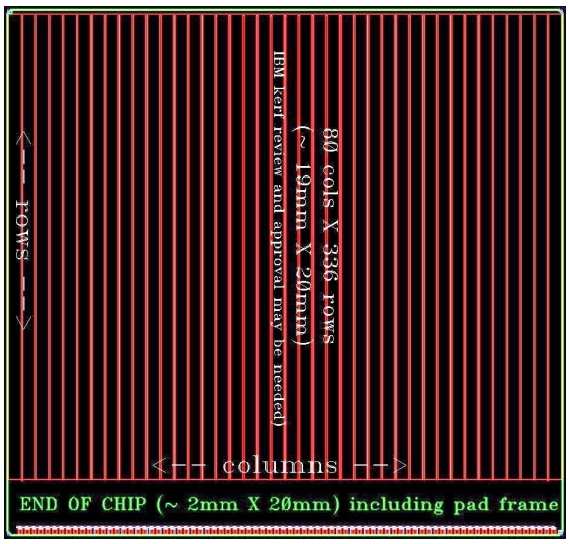


Figure 59. FE-I4 chip outline.

time elapsed since the event took place with 25 ns resolution. Clearly this requires distributing the 40 MHz clock to all the regions. The maximum skew of the clock distribution network is 2 ns. When an external trigger arrives, it is also distributed to all the regions simultaneously within 2 ns. The trigger selects any events for which the time counter matches the programmed trigger latency value. When the counter exceeds the latency without a trigger, the event is erased to make room for more. The events selected by a trigger remain in the region until it is their turn to be sent off chip via the serial LVDS output. All regions can be read out if they are all selected.

The individual discriminator outputs are synchronized with the 40MHz clock as they feed into the region logic, and all region operations are synchronous. Each synchronized discriminator output is further processed by applying a digital cut on the time over threshold (TOT). Hits smaller than a certain TOT (programmable between 1 and 3 clock periods) are classified as “small hits” and those larger as “large hits”. The next available time counter in a given region starts whenever there is at least one large hit. Small hits do not start a counter. Once a counter starts, the TOT value of all 4 pixels is always recorded (which is 0 for a comparator that did not fire). This automatically stores small hits in the same time bin as large hits from the same cluster. This relaxes the time-walk requirements on the analog circuitry, allowing lower current operation. As clusters will often straddle a region boundary, in addition to storing all 4 pixels within the region, 4 neighbour bits are stored to flag the presence of small hits in the pixels adjacent to the region in the phi direction. An association window of two clock cycles is used to capture small hits both within the region and in the 4 neighbor pixels. This scheme is equivalent to the hit duplication function of the FE-I3 chip, where all hits below a certain TOT value are copied to the preceding time bin, but it is more efficient in terms of memory and latency counter usage. Note that by setting the programmable digital TOT threshold to the minimum, one recovers traditional hit discrimination, in which all comparator firings are considered equal and recorded in the time bin that they occurred (which,

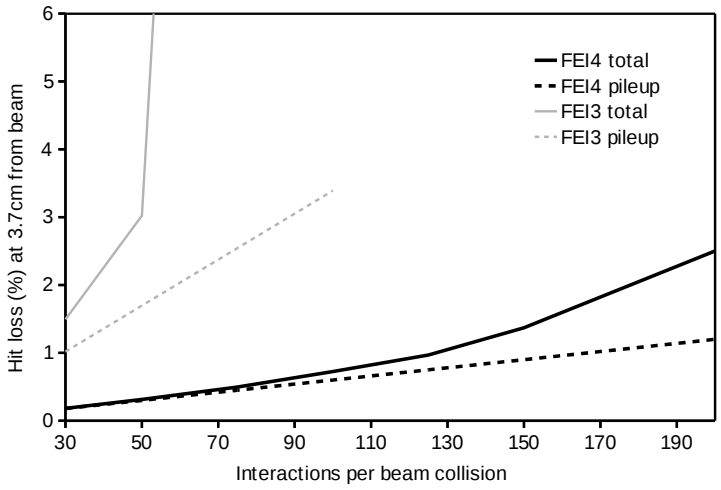


Figure 60. Simulated data losses for FE-I4 and FE-I3 chips placed at 33.25 mm from proton-proton beam collisions at 14 TeV. The simulation was performed with a sensor mean radius of 37 mm, and the results were then scaled to 33.25mm assuming that hit rate scales as $1/R^{1.9}$.

due to time-walk, tends to be the wrong bin for hits just above the analog discriminator threshold).

All the above data driven information is stored locally in the 4-pixel digital region and only moved further if selected by a trigger. The raw hit rate that this architecture can accommodate with high efficiency is a function of the amount of memory in the region, and how quickly this memory is emptied (given by the programmed trigger latency). Events selected by a trigger remain in the region much longer than the latency (until they are read out), and therefore a higher trigger rate contributes to filling up the region memory, but because the trigger rate is low relative to the raw hit rate this is not a dominant effect. Fig. 60 shows the simulated inefficiency for charge deposits in 250 μm planar unirradiated silicon at 33.25 mm radius as a function number of minimum bias interactions per 25 ns beam crossing, assuming a 3750 e^- discriminator threshold, 120 crossing latency, and 100 kHz trigger rate. The simulation was performed with a sensor mean radius of 37 mm, and the results were then scaled to 33.25mm assuming that hit rate scales as $1/R^{1.9}$ (this is an approximation that fits well radiation dose simulations in this ilminted radial range [64]). The simulated performance of the present FE-I3 chip under the same conditions is also shown for comparison. The FE-I4 inefficiency is dominated by single pixel pile-up, and not by the readout architecture, until well beyond the 75 interactions per crossing projected for IBL. The result can be applied to slightly different layer radius by scaling the horizontal axis as $1/r^1.9$. In this simulation the rate of discriminator firing (scaled to 33.25 mm) at 75 interactions per crossing was 490 MHz/cm^2. Single pixel pile-up, the main source of inefficiency, occurs when a pixel is hit while the discriminator is still high from a previous hit. The requirement to keep the total inefficiency below 1% was the driving reason for reducing the FE-I4 pixel area relative to FE-I3 as well as the TOT dynamic range

to 4 bits instead of 8.

The FE-I4 circuitry is divided into functional blocks with well-defined interfaces. This facilitated the design process carried out by a geographically distributed collaboration. Fig. 61 shows a simplified schematic of the data path in a typical data acquisition configuration, while Fig. 62 shows the simplified command and configuration path for typical single-chip operation. It may be appreciated from these figures that the output path is common for data and configuration, which both use a common fixed format record as discussed in the next section. In terms of physical area, 89% is taken up by the 40 column pairs, each consisting of two analog columns and a digital column pair. These are interfaced to the global control and logic on the chip periphery by a "horizontal" circuit layer running along the bottom of all columns and containing the end of digital column logic (Fig. 61) and the distribution of analog column configuration, bias, and calibration signals (Fig. 62). All the periphery circuit blocks are single column pair oriented, with data, clocks, biases, etc. distributed to/from one or more column pairs in parallel as programmed into the global configuration. A great many functions of the periphery logic blocks are programmable, and the global configuration is implemented as a random access memory of 16-bit words. For example, the clock source used to serialize output data can be selected to be any of the PLL outputs (40 MHz, 80MHz, 160 MHz, or 320 MHz), the raw 40MHz input clock, or an auxiliary input. The data output

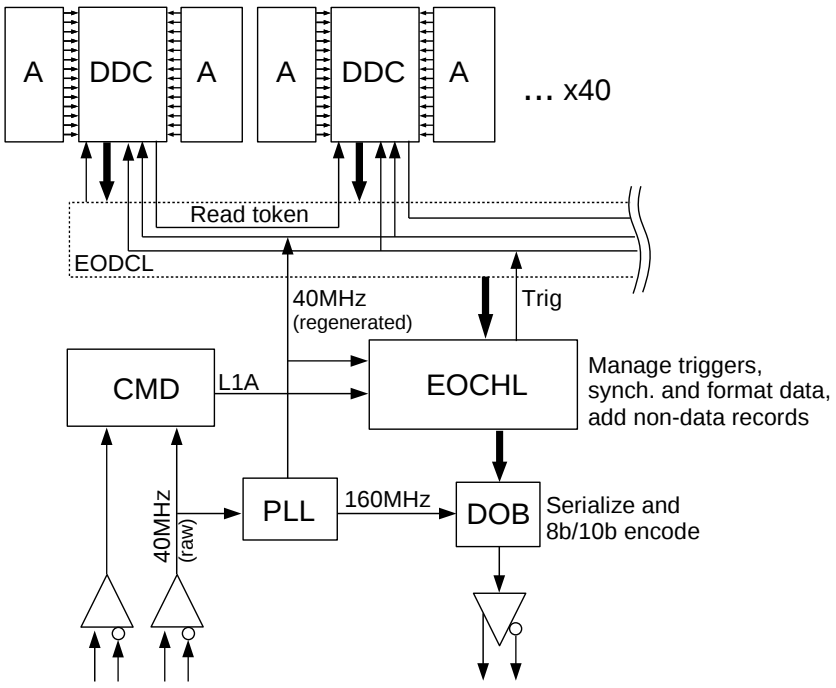


Figure 61. Simplified schematic of the output data path in a typical data acquisition configuration. Circuit blocks shown are analog column (A), digital double column (DDC), end of digital column logic (EODCL), command decoder (CMD), phase locked loop clock multiplier (PLL), end of chip logic (EOCHL), and data output block (DOB).

block can be configured to implement 8b/10b encoding or not, or to loop back the input clock, and so on. The configuration memory is implemented with triple-redundant SEU hard custom cells, while the digital logic blocks are either triplicated with majority voting or Hamming coded, always synthesized from standard cell libraries.

3.3.4 Input and output

The FE-I4 is controlled by an external clock (nominally 40 MHz) and serial command bitstream, where the bits are latched on the rising edge of the clock. This was defined to be exactly compatible with the down-link communication to a present detector module. The serial commands themselves, however, cannot be identical because they are connected to the internal details (for example a present module has 16 front end chips, while the FE-I4 is one single front end chip). Nevertheless, the command structure has been kept the same and "fast" commands are identical. Commands are divided into "fast" and "slow" as an indication of the number of bits needed to transmit the command. The fastest command is the level 1 trigger, which is 5 bits long and immune to any single bit flip. The remaining fast commands, all 9 bits long, are beam counter reset, event counter reset, and calibration pulse inject.

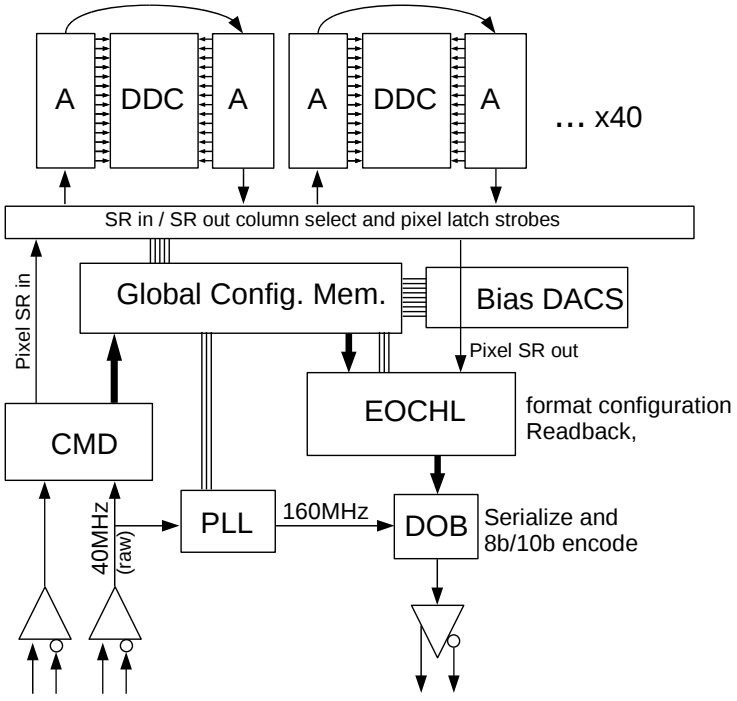


Figure 62. Simplified schematic of the configuration path for typical single-chip operation. Circuit blocks shown are analog column (A) including Shift Register (SR), digital double column (DDC), global configuration memory, analog bias digital to analog converters (DACS), command decoder (CMD), phase locked loop clock multiplier (PLL), end of chip logic (EOCHL), and data output block (DOB). The plain lines without arrows indicate static configuration bits.

Slow commands are at least 19 bits long and are specific to FE-I4. All programming of internal settings, queries, diagnostic functions, etc. take place via slow commands. Even though the FE-I4 has increased functionality, the internal control structure and therefore the variety of slow commands is simpler than for the present detector. The control is designed almost entirely around programmed settings, and these settings are organized as a random access memory of 16-bit words. Thus for most operations there are only three basic commands: write or read a 16-bit word, and something equivalent to "execute". The main exception is the programming of the pixel configuration registers. For this case there is a dedicated command to send a bitstream to a 672-bit shift register. This is the number of pixels in a column pair and each column pair is independently addressable.

The FE-I4 output is significantly different from the present detector. The most obvious difference is due to the requirement that a single output link be capable of 160 Mb/s (including encoding overhead), in order to cope with the expected IBL hit rate at 100 kHz trigger with a manageable number of connections (1 LVDS output per chip). Because of this unavoidable incompatibility with the present system, the FE-I4 output format was not made backwards compatible, and instead was designed to improve upon the present experience. The main new feature is the use of the DC-balanced 8b/10b commercial standard that was specifically developed for reliable optical communication and has been very successful. This encoding does entail a 25% bandwidth overhead relative to raw, un-encoded output, but the 160 Mb/s data rate has room for it. In addition to more reliable optical link operation, the 8b/10b encoding provides the necessary features of loss of lock detection, synchronization, and robustness against single bit flips. Additionally it provides error detection for every frame and the possibility of clock recovery using commercial parts at the receiving end. As all these functions are provided for, the data before 8b/10b encoding is organized into fixed frame 24 bit records, avoiding the complications of a variable frame format with synchronization bits as presently used. As almost everything in FE-I4, the use 8b/10b encoding can be selectively configured.

Each 24-bit frame (before 8b/10b encoding) can be a data frame containing the address and TOT values for two pixels, a data header indicating that data records follow, a configuration value, a configuration address to identify said value, or a service record containing error messages. 32 Different error types are logged and counted. All non-data records have unique patterns that can never occur in data records. This is thanks to the fact that the numbers of rows and columns in the chip are not powers of 2, leaving unused addresses in the binary encoding. There is no data trailer, as this is provided by the 8b/10b code. When 8b/10b is turned off there is also an empty record (consisting of a programmable bit pattern) that doubles up as a data trailer. The FE-I4 output is never idle, it is always sending empty frames (or "commas" in 8b/10b mode) when there is nothing else to send. The programmability of the empty frame when 8b/10b mode is turned off can be useful, for example, to implement custom loop-back tests. A direct loop-back of the 40 MHz clock is also provided.

The maximum IBL output data volume was estimated by using charge deposits in an unirradiated, planar silicon sensor as input to a chip behavioural model with 3750 electron discriminator threshold. The model includes the full data formatting, including dynamic phi pairing of hits and 8b10b encoding. The charge deposits were generated with full physics simulation of tracks from 75 piled up minimum bias interactions at 40 MHz rate for 2 seconds, with the detector layer placed

at 3.7 cm radius. The chip was read out with 100 kHz random triggers. The result of this simulation was scaled to the lower IBL radius with also lower number of interactions per crossing (55)– two cancelling effects. After scaling, the average output data volume was 88 Mb/s. The fluctuations are small since the number of hits per chip per crossing is about 40. Also the dependence on module location along Z is negligible. Therefore, the 160 Mb/s output bandwidth provides enough margin to cover uncertainties in the simulation (for example from track multiplicity of minimum bias events at 14 TeV center of mass, different sensors or threshold, or non-collision beam backgrounds).

3.3.5 Simulation and measurement

Many of the sub-circuits that make up FE-I4 have been prototyped in silicon as stand-alone test chips. These include several scaled versions of the analog pixel array including current reference [65] and bias generator, the clock multiplier and output data serializer-encoder, the LVDS input and output drivers, the SEU tolerant latches [66], and scaled down versions of the voltage regulators [**?**] and the DC-DC converter. For all these circuits simulation results were in excellent agreement with bench measurements on the test chips, validating the transistor models used in the entire range needed for the full chip. While the models are very accurate, it is not practical to perform analog simulations of the full 87M transistor chip. The validation strategy therefore relies on a 3-step approach. (1) Behavioral simulation using a digital model for the full chip, which is produced from the physical layout by commercial software tools. (2) Mixed mode simulation where some analog circuits, power distribution, and interconnects are simulated within the full chip behavioral model. (3) Full analog simulation for short times of individual blocks. The goal of the behavioral simulation is to model the full chip as a "black box" that can only be contacted using the final I/O pads. Thus, simulations of configuration, calibration injection, and hit data acquisition are performed using identical command sequences and output parsing as will be run on a real bench test setup.

The prototype test chips have served not only to validate the simulation models, but also to verify the radiation tolerance of the process. Some of the results have already been presented in Section 3.3.2. Test devices have been irradiated with protons up to doses of 400 Mrad and no loss of digital functionality has been observed. Analog measurements have only been performed up to 200 Mrad because the bias generator of the second stage feedback drifted outside the operating range beyond that dose. The design of this particular bias has been corrected based on this experience. No other biases had problems and the behavior is understood. Radiation effects on pixel noise are expected to be very small, but accurate measurements have not been possible due to the lack of prototypes with a proper sensor load. Attempts to bump bond miniature sensors to the 2 mm $\times$ 3 mm pixel array in a prototype test chip have failed. Measurements with built in diode loads show a modest noise increase with radiation, but this is thought to be due to changes in the diode properties rather than the amplifier (Fig. 63). In addition to the problems with internal diode loads, these measurements have a systematic uncertainty that could be as much as 40% due to the absolute charge scale calibration, which is challenging for a test circuit with no sensor and thus no source of reference charge.

3.4 Integration

Sensors and FE-I4 chips are integrated through flip chip bump bonding. The resulting assembly

is called a bare module, which can be a single chip module or a 2-chip module, depending on the sensor technology. This bare module is then made into a fully stand-alone detector unit by adding a flexible printed circuit board (flex) with passive components, a method of external connection, and a support frame. This exactly parallels the assembly steps followed for the present detector [28]. The construction of a stand-alone object in a disposable support frame was extremely useful for testing, burn-in, and general handling, and so should be maintained for IBL. The important development needed for IBL is the elimination of individual module connectors. An IBL stave will have 32 (16) single chip (2-chip) modules. A pigtail style connector on each one (as used in the present detector barrel) would translate into a large amount of dead material and would require a significant amount of space which does not exist. Conversely, an individual, long cable permanently attached to each module leading to a distant connector (as in the present detector end-caps) would bring serious complications for assembly (making it very difficult to replace an arbitrary module on a stave) and would require challenging strain relief in the active region. The solution under development for the IBL is therefore to have cables already integrated on the stave mechanical structure before any modules are loaded, and to connect such cables to each module (after the module has been loaded) by some permanent, reworkable method, such as wire bonding. It is important the connection be reworkable to allow replacement of an arbitrary module. The module flex would be very small with bond pads within the sensor perimeter or on a very short tail. Fig. 64 shows a possible design with a very small flex (mini-flex) that covers less than half of a single chip bare module. The final flex module is cut away from a much larger sacrificial PCB frame with laminated flex circuit after all tests and burn-in have been completed. This module design is compatible with a stave with integrated cable featuring flex "flap" at the position of each module, to be affixed to the bare part of the sensor and then wire bonded to the mini flex (see Sections 4.3.3 and 4.4).

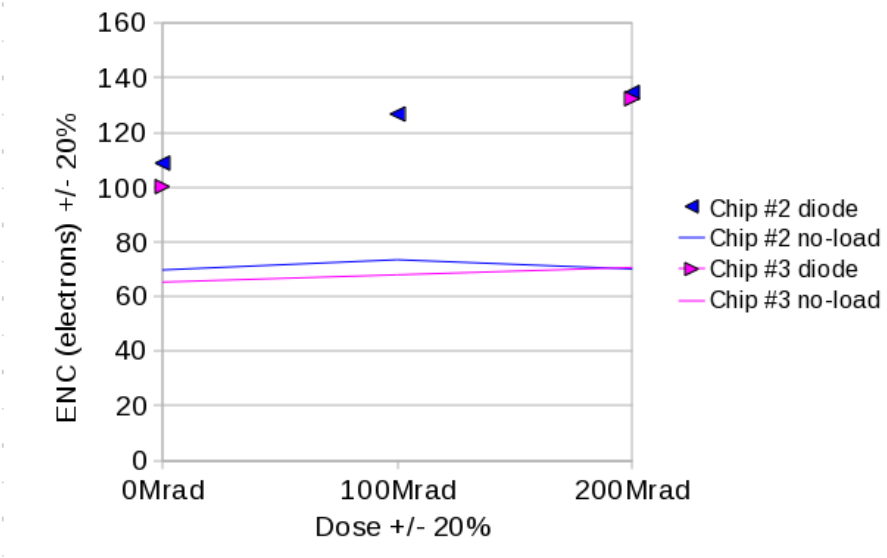


Figure 63. Measured pixel noise vs. radiation dose for unloaded channels and for channels with an internal diode load. The radiation induced changes on the internal diode load are not well known.

3.4.1 Bumping and flip-chip technology

A key step of the IBL module integration is the flip-chip bump bonding process which connects each sensor pixel with the corresponding readout cell of the FE-I4 chip. The general requirements for the bump bonding process are:

- bump pitch of 50 μm.
- bump density of 80 bumps per mm^2 or 26,880 bumps per readout IC.
- defect rate $< 10^{-4}$.
- flip-chip using FE-I4 chips thinned to less than 200 μm.

These requirements are similar to those met for the present detector. However, the large format of the FE-I4 makes the IBL flip chip process more challenging. For the present detector, the FE-I3 chips were thinned to 190 μm, and this was thick enough to control the bow of the chips to within the bump height tolerance when changing between room temperature and solder reflow temperature. Because of the larger size, the FE-I4 chip would have to be approximately 400 μm thick to achieve the same bow control. Since this is unacceptable for IBL, a modified flip chip process must be used. The modification can entail the use of a support wafer temporarily bonded to the thinned FE-I4 chips in order to control bow during reflow, and which must be removed before flex module assembly. This new process step is the main technical challenge for IBL flip chip bump bonding.

During the production of the current ATLAS Pixel detector two different bump bond technologies were used, indium and solder, with approximately half of the modules built with each.

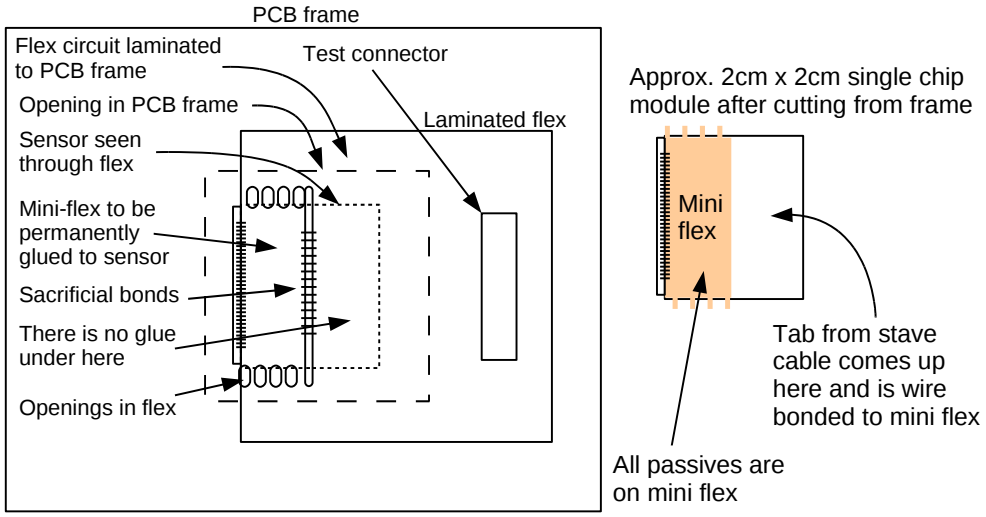


Figure 64. Mini flex concept for single chip module

Indium technology is based on evaporation of the metal on both sensors and readout chips, followed by interconnection through a thermo-compression step to produce an indium-indium bond. The mechanical strength of this bond is relatively weak. Solder technology uses an electroplating of eutectic solder on only one wafer whereas the other is only treated with the Under Bump Metallization (UBM). The interconnection is made by solder reflow at a temperature of about 250° for lead-free solder (the current practice). Both technologies met the requirements for the present detector, but in a direct comparison the fraction of defective solder bumps is smaller and constant, while the fraction of defective of indium bumps is larger and has increased slightly during operation. The baseline bump bond technology for IBL is therefore solder. Tests of indium bump bonding will nevertheless be carried out as a backup and to understand the chip size implications for that technology.

In addition to solder and indium, new technologies have become available since the construction of the present detector and have been surveyed for IBL. Table 13 summarizes the bump technologies currently available on the market. All of these technologies are in use within the HEP community, although sometimes only in first prototypes with limited statistics. Because the number of IBL modules is small compared to the current detector the baseline technology choice has been limited to one of the two already proven in ATLAS. However, the progress of the other, newer technologies will be closely observed in case the choice must be reconsidered when more results are available.

The IBL solder flip chip process consists of four main steps:

1. UBM treatment of the aluminum bump pads on both readout chip and sensor and the deposition of bumps on the chip;

2. Thinning of the readout IC wafers to the target thickness of 200 μm or less and the bonding of the thinned wafer to a carrier, followed by the dicing of sensor and chip wafers (including dicing of the carrier);

3. Flip-chip assembly of the sensors and readout ICs with an accuracy of a few μm, and

4. Removal of the carrier wafer element from the flip chip assembly.

Whereas the first two steps are wafer scale processes, the flip-chip is usually a single die process after cutting the sensor and readout IC wafers. The temporary support wafer bonded to the back side of the readout chip counteracts the temperature induced bow during the reflow operation. This ensures that bumps make contact over the entire surface. After the reflow there is no longer a temperature induced bow and this support can be removed. Well below the melting point the solder bump connection is rigid enough to keep the assembly flat. This technique has been demonstrated on FE-I4 sized wafer fragments of FE-I3 chip wafers. Such samples have been thinned to about 90 μm and bump bonded to dummy sensors with high bump yield. The samples were made of FE-I3 chips cut in 2-by-2 arrays (roughly 15×22 mm^2). After the solder bump deposition, the FE-I3 IC wafer was thinned to 90 mm using standard wafer grinding methods and mounted onto a thick glass support wafer using polyimide film. The full assembly of glass plus IC wafer was fully diced into 2-by-2 chip arrays as described. The polyimide bond can withstand solder reflow temperature without losing adhesion. The IC-glass sandwich arrays were flipped onto the dummy

sensors without any thermally induced bow. After flip-chip, the glass support was removed by laser exposure of the polyimide film through the glass. Fig. 65 shows a cross-section picture of a flip-chipped device after support wafer removal. One can clearly recognize the uniform ball shaped solder bump bonds with a pitch of 50 μm. No evidence for disconnected bumps has been found in the full assembly. The effective readout IC thickness is measured to be 87 μm. But the handling of these devices is demanding and in subsequent assembly steps like gluing to the support structure and wire bonding can easily lead to disconnected bump bonds. To summarize, the results of aggressively thinned flip-chipped pixel assemblies are encouraging, but still in a development stage and more work is needed before the method is qualified for production and module to stave loading.

Other than the thickness of the readout chip, the bump bonding must be compatible with the three proposed sensor options. For the current Pixel detector planar, n-on-n sensors have been used. This sensor type thus already been demonstrated to be compatible with the solder and indium bump bonding technology. For the other sensor options, i.e. the 3D sensors and the diamond sensors, the experience with bump bonding is much less. 3D sensors have been bump bonded to FE-I3 single chips at different vendors. For diamond sensors, solder bump bonding to current ATLAS pixel readout ICs has been successfully demonstrated. In fact, the standard UBM technique has been used to deposit metal on diamond sensors to form the pixel electrodes on the bare diamond substrate. A possible compatibility concern arises with n on p type planar sensors, due to bias voltage being present on the same side of the sensor as the bumps, presenting the risk of high voltage breakdown to the chip surface (bias is also present near the chip for 3D sensors, but the lower depletion voltage of 3D sensors is not considered a potential problem for the sensor-chip air gap). The potential breakdown problem for n on p sensors is being addressed with a BCB protective layer.

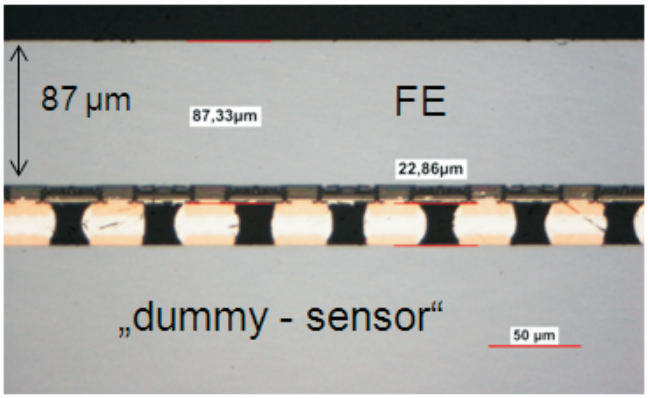


Figure 65. Cross-section of a flip chip test assembly of FE-I4 size, thinned down to 87 μm and bump bonded using using a glass carrier wafer as described in the text. The 87 μm includes the dark area just above the bumps, which is the IC circuitry. The gap between chip and sensor (height of the connected bumps) is shown as 22.86 μm.

3.4.2 Module assembly, test, and burn-in

Similar terminology is used for IBL module production as was used for the present detector. The flip chip assembly of one sensor plus readout integrated circuits is called a bare module. The addition and wire bonding of a flexible printed circuit (flex hybrid) turns the bare module into a flex module. This operation is called module assembly. The IBL module production flow will be based on that used for the present detector, but with some simplifications: there will be no single chip probing of FE-I4 chips after wafer dicing, no bare module probing, and no rework of flip-chip assemblies except in the case that diamond sensors are selected. These simplifications follow from the facts that the IBL module has only up to 2 chips instead of 16, and there is no module controller chip that must be added with the flex hybrid during module assembly. Thus there is no need to maximize the yield of known good FE-I4 chips before flip chip, and there is no benefit reworking a module with a bad FE-I4 chip relative to just making a new module. The case of diamond sensors is the exception, because the cost of diamond sensors is expected to be high, and diamond sensors can be recycled (stripped down to the bare diamond an reused as new sensors) as often as necessary. The module production flow including testing is shown in Fig. 66.

The module handling techniques should be based on those successfully used in the present detector. A handling frame should be implemented as previously explained. The wire bonds to connect the FE-I4 chip to the flex hybrid should have their feet encapsulated to rule out the possibility of resonant vibration in the 2 T magnetic field [67].

3.5 Production and Qualification

The module and its components must undergo a qualification program before production can begin. This is a different, later stage than the initial prototyping leading to a final design, including a sensor technology choice. It is expected that this qualification will be performed after a final design

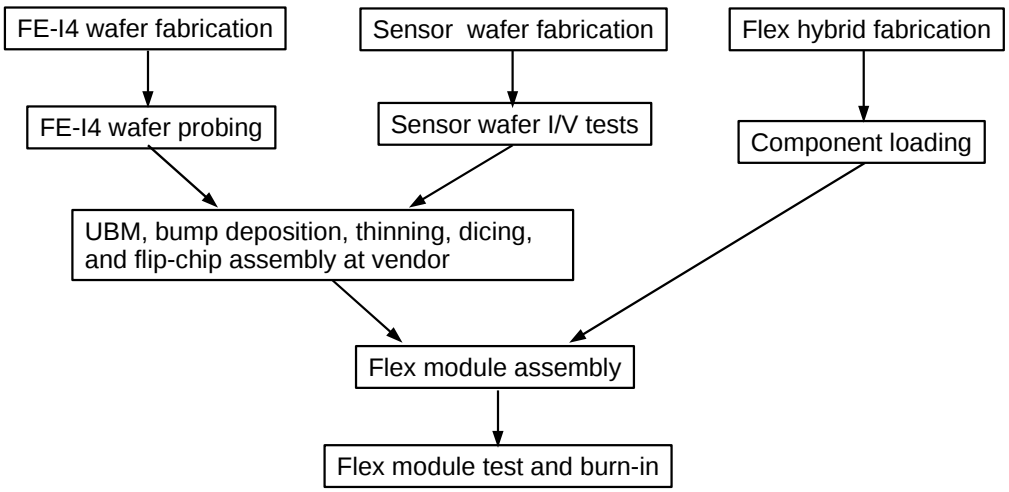


Figure 66. Flow diagram of IBL module production and testing.

review and will lead into a production readiness review. This qualification will be based on early prototypes plus a pre-production statistical sample using the final design for every component. Radiation tolerance and test beam performance will be measured in early prototypes, while properties requiring larger statistics will be confirmed with the pre-production. Following this qualification the pre-production modules can be used to assemble pre-production staves to qualify the stave assembly and testing. Estimated component quantities for pre-production are given in Table 14 (for the example of 2-chip modules), taking into account expected yields.

The purpose of the qualification is the demonstrate that the final design meets the performance requirements and that the assembly is robust enough such that performance does not degrade with handling, assembly, and operation. The following guidelines should be followed.

- Radiation tolerance. At least 3 modules with the final sensor choice should be irradiated using protons or pions to the IBL lifetime NIEL dose and operated in the lab and in a teat beam. The hit efficiency and position resolution should be verified to remain above the minimum required values in a test beam following the irradiation. In addition to total dose, at least one module should be exposed to high dose rates (10^9 protons/cm^2/s) with full power and bias voltage to check that no permanent damage occurs. This test could be combined with SEU measurements.

- As built bad bump fraction. The full sample of qualification modules should be subjected to a burn-in program involving of order 50 thermal cycles with power on between +40 °C and -35 °C. Live channel fraction should be determined with a radioactive source scan after burn-in. In addition, a group of 3 to 5 modules should be subjected to a more extreme program involving thermal shock and power-off cycling between +80 °C and -40 °C, with mechanical attachment to dummy stave substrates using the baseline adhesive. If any damage is seen in these modules, the mechanism should be understood, including cycling more modules as needed. The survival of +80 °C with power off is not a baseline requirement, but could be adopted as production test to guarantee that beam pipe bake out is a safe operation even without cooling.

- Wire bonding. A standard pull test program should be followed to monitor the quality of wire bonds in the full sample. Since the FE-I4 chip has a large number of I/O pads for testing that will not be needed for module operation, as many as possible of these pads should be dedicated to make sacrificial wire bonds to matching dummy pads included on the flex hybrid. These sacrificial bonds should be destructively pulled at various stages of assembly and testing to track any evolution of the bond strength.

Item	Value	Units
Pixel size	50×250	μm^2
Bump pad opening diameter	12	μm
Input	DC-coupled -ve polarity	
Maximum charge	100 000	e^-
DC leakage current tolerance	100	nA
Pixel array size	80×336	Col $\times$ Row
Last bump to physical chip edge on 3 sides	≤ 100	μm
Last bump to physical edge on bottom	≤ 2.0	mm
Normal pixel input capacitance range	100-500	fF
Edge pixels input capacitance range	150-700	fF
Pixel analog power (for meeting specs)	15	μW
In-time threshold with 20 ns gate (400 pF)*	≤ 4000	e^-
Hit-trigger association resolution	25	ns
Same pixel two-hit discrimination (time)	400	ns
Single channel ENC sigma (400 fF)	< 300	e^-
Tuned threshold dispersion	< 100	e^-
Charge resolution	4	bits
ADC method	TOT	
Radiation tolerance (specs met at this dose)	250	Mrad
Operating temperature range	-40 to $+60$	°C
Average hit rate with $< 1\%$ data loss	400	MHz/cm^2
Per pixel digital power with above hit rate	<15	μW
Readout initiation	Trigger command	
Max. number of consecutive triggers	16	
Trigger latency (max)	6.4	μs
Maximum sustained trigger rate	200	kHz
External clock input	40	MHz
Single serial command input	40	Mb/s
Single serial data output	160	Mb/s
Output data encoding	8b/10b	
I/O signals	LVDS	

Table 11. Basic specifications for FE-I4. (*) This specification applies to the discriminator output. Hit detection using region timing will reduce sensitivity to time-walk.

	Internal nodes	Linear regulators	DC-DC converter	Units
Min. operating voltage	1.20	1.30	1.30	V
Maximum operating voltage	1.50	1.65	3.40	V
Nominal operating current	0.60	0.60	0.31	A
Maximum current at max. voltage	0.90	0.90	0.46	A
Peak transients allowed	1.75	2.00	4.0	V
Maximum voltage at power supply	2.10	2.50	4.73	V
Derived R/T drop allowed in cables	0.60	0.85	1.33	V

Table 12. Voltage ratings and current consumption of FE-I4A

Bump technology	Possible Vendors	Status
Solder (SnAg or PbSn)	3	Used for ATLAS, CMS & ALICE Pixel; experience with big and thin chips
Indium	1	Used for ATLAS Pixel
Indium with reflow	1	Used for CMS Pixel
Solid Liquid Interdiffusion (SLID)	1	First dummies produced
DBI Oxide Bonding	1	First tests with 3D-Integration
Glue Injection Mirco-Bonding	1	First tests with 3D-Integration

Table 13. Bump technologies and number of vendors currently available.

Component	Number needed	Yield into next line
Total FE-I4 wafers	4	50%
Good FE-I4 chips	120	93%
Good 2-chip sensors (*)	55	93%
Total bare modules	51	93%
Total flex hybrids	48	93%
Good flex hybrids	45	-

Table 14. Pre-production quantities needed for module qualification; (*) sensor wafer quantity depends on chosen technology.

4. Staves

The IBL modules are supported by means of fourteen local supports, the *Staves*, arranged cylindrically around the beam pipe. Some overlap between modules is provided by tilting each stave about 14 degrees. The nominal layer radius, that is the distance from the beam axis to the sensor's centre-of-mass, is $R = 33.25$ mm. The overall layout of the detector is presented in Section 2.3.4 and details can be found elsewhere [68].

This chapter describes the stave and the associated electrical services. Following a conceptual overview, the mechanical design and prototyping work are described in Section 4.2. The on-stave (type 0) electrical services are discussed in Section 4.3, and the assembly procedure is detailed in Section 4.4. A description of the internal type I services is included in Section 4.5.

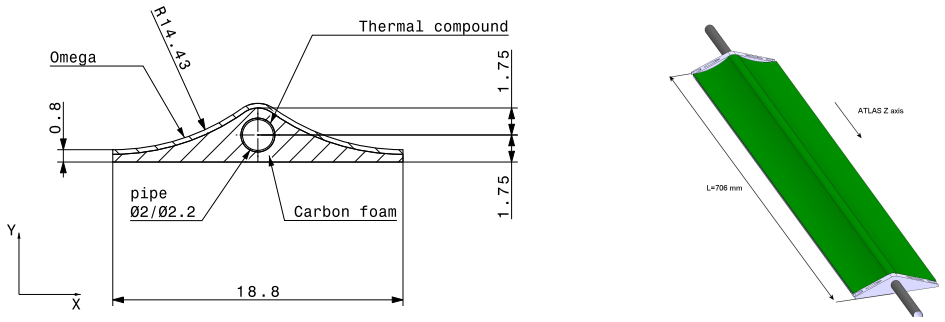
4.1 Requirements and Conceptual Design

The stave design is based on carbon foam material that provides a path for the heat generated in the sensors and in the front-end chips, to the cooling fluid boiling at low temperature in the cooling channel. The stiffness of the structure is provided by a quasi-isotropic carbon fiber laminate, the *Omega*, that is bonded to the foam. Figure 67 shows the cross section and a 3D view of the stave. The cooling pipe is sandwiched between the carbon foam and the *Omega*. The pipe is hard bonded to the structure, the thermal contact being provided by a thermal compound based on epoxy-loaded resins.

4.1.1 CTE mismatch

The evaporation of the coolant takes place typically in the temperature range between $-30\,^{\circ}$C and $-40\,^{\circ}$C. Assuming that most of the IBL assembling process takes place at room temperature, the structure is subject to a thermal load of $-60\,^{\circ}$C. The mismatch of the Coefficient of Thermal Expansion (CTE) between the different parts of the stave assembly has a significant impact on the stress level and on the deformation induced by the cool down. In particular, the most critical issues are the shear stress in the adhesive layer between the pipe and the foam, and the deformation induced by the cool down.

As shown in Fig. 67, the cross section of the stave is not symmetric and the CTE mismatch between the pipe and the foam induces a bow of the stave in the vertical plane. The amplitude of



(a) Cross-section (b) 3D view

Figure 67. Cross section and 3D model of the IBL stave. Dimensions are in millimeters.

the bow depends upon the thermal field in the structure. The maximum deformation is reached when the stave is cooled down with no thermal load from the modules (modules "off") since this maximises the temperature difference from the room temperature at which the stave is assembled. When the modules are powered, a thermal gradient is established in the cross section. This causes the stave to change the shape as function of the power generated in the modules. The module power is indeed not constant and it depends upon the *state* of the front-end chip and upon the irradiation of the sensor.

The minimisation of the CTE mismatch is an important design guideline because it increases the geometrical stability of the sensors for the different operation states and it reduces the stress level in the bonding layer. The adhesive layer is critical for the thermal performance of the stave; adhesion failures would result in an unacceptable degradation of the performance.

4.1.2 Design requirements

Table 15 lists the thermo-mechanical requirements of the stave. The hydraulic part is driven by the choice of the coolant. At the moment the most demanding fluid considered for the structure is CO_2.

CO_2 has a rather high critical pressure (73.8 bara) at 31 °C. In case the plant looses the cooling power, the pressure can reach and even exceed this value. The maximum design pressure (MDP) has been therefore set to 100 bara.

The triple point is at -56.5 °C at 5.1 bara, below which the sublimation line starts and the phase is solid. While the operation temperature range is set by the module requirements, the temperature range for non-operational conditions depends upon the failure scenarios: the triple point temperature on the lower side, and maximum foreseen temperature in case of failures during the beam pipe bake-out.

The geometry accuracy and stability are set on the basis of the inter-stave clearance as detailed in Fig. 68, see Table 15. Assuming the two staves are off-nominal by 0.25 mm in the opposite directions, the remaining clearance is still about 1 mm.

The deformation induced by the CTE mismatch during the cool down allows a maximal displacement of 0.15 mm. This reduces the remaining clearance to 0.7 mm, which is enough to avoid interferences and clashes.

4.2 Details of the Stave Design

As outlined above, the stave assembly has three main parts: the boiling pipe, the Omega skin, and the carbon foam. This section outlines the design considerations and material selection criteria for each of the three parts, and goes on to describe thermal and mechanical issues pertaining to the integrated stave.

4.2.1 Boiling pipe

The design of the boiling channel focuses on three targets: i) minimize the material, ii) pressure resistance at a 100 bara MDP and iii), match the CTEs of the surrounding materials. Two different pipe materials have been considered and developed: Titanium (Ti) and Carbon Fiber (CF).

Several considerations, discussed later in this chapter and Chapter 10, led to the choice of the Ti pipe eventually. However, the development of the CF pipe is considered still relevant for future

Item	Requirement
Normal Operating Thermal Conditions at Full Power	
Max thermal figure of merit Γ over the full lenght	≤ 30 K·cm^2/W
Operational temperature range	-40 °C to $+60$ °C
Storage and/or non operational temperature range	-60 °C to $+80$ °C
Normal operating pressure conditions	
Nominal operational pressure	10.0 bara
Max design pressure	100.0 bara
Structural safety factor for composite pipe	$SF \geq 4$
Structural safety factor for metal pipe	$SF \geq 2$
Radiation Conditions	
Total integrated dose	350 MRad
Material Budget	
Radiation length of the mechanics (active region) - goal	$\leq 0.7\%\ X_0$
Miscellaneous Conditions	
Dynamic stability as supported -goal	≥ 100 Hz
Conducting particles from carbon or other materials	Not allowed
Corrosion from all sources	Prevent
Erosion from fluid flow	Prevent
Surface characteristics	Compatible with module
Maximum leak rate of boiling channel	10^{-7} atm·cc/s of He
Maximum leak rate of each connection	10^{-5} atm·cc/s of He
Envelopes and tolerances	
Max deviation from nominal shape	0.25 mm
Module interface planarity	0.05 mm
Stave Stability Tolerances	
Max displacement during cool-down	0.15 mm

Table 15. Summary of mechanical requirements for the local support.

upgrades, hence this chapter describes its development in some detail, and sometimes compares the performance of staves built with the two pipes considered.

The titanium pipe is a thin walled Ti Grade 2 cold drawn tubing. The choice of titanium is appealing due to the availability of pipes of almost any diameter, with thicknesses down to one tenth of a millimetre. The yield stress of the titanium allows 100 μm wall thick pipes for a 2 mm ID at a MDP of 100 bara. The resulting structural safety factor is SF > 4, which is compliant to the design guidelines for the hydraulic and pressure lines ANSI/AIAA S-080 [70]. The main characteristics of the Ti pipe are listed in Table 16.

The CF pipe is an epoxy-based, extruded tube obtained by impregnating a carbon fiber braid under vacuum. A drawing process over polytetraflouroethylene (PTFE) dies follows the impregnation to form the tubing. The braid has T300 1K rowing fibers organised in a 12 by 2 yarn at $\pm 45^\circ$. Table 17 summarises the characteristics of the CF pipe.

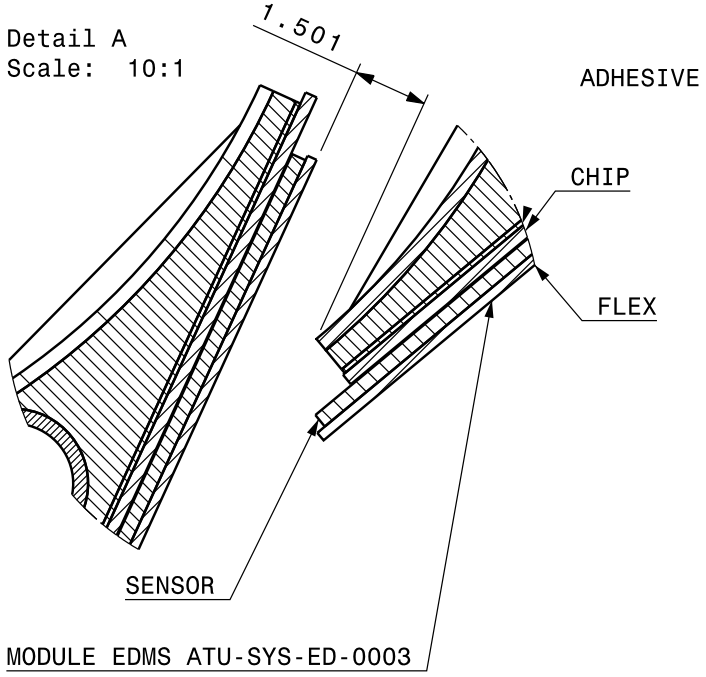


Figure 68. Inter-stave nominal clearance detail (extracted from [69]). The assembly tolerances are set to prevent clashes between adjacent staves.

4.2.2 Omega

The Omega provides the structural stiffness to the stave assembly (Fig. 67). It is a carbon fiber laminate based on the YS-EX1515 cyanate ester pre-preg. The actual layout depends on the cooling pipe material, which exert different bending forces on the Omega, due to their different CTEs.

Table 19 gives the induced bow of the stave during the cool down; to obtain comparable bowing sags, a stave with a titanium pipe requires a thicker Omega. The laminate needs to be 300 μm thick, with a 12-plies quasi-isotropic layup $(0/60/-60)_{S2}$. For the carbon fiber pipe, the Omega would be much thinner, 150 μm with a 6-plies layup $(0/60/-60)_{S1}$.

Material	Ti Grade 2 (Ti40).
Dimensions	2 mm ID, 0.12 mm Thickness
Density	4.51 g/cm^3
Temper state	Annealed
Tensile strength (yield)	275 MPa
Tensile strength (ultimate)	344 MPa
Coefficient of thermal expansion (CTE)	8.9 ppm/°C
Thermal conductivity	16.4 W/m°K

Table 16. Thermo-mechanical properties of the Ti Grade 2 pipe.

Material	CF laminate
Dimensions	2.4 mm ID, 0.3 mm Thickness
Density	1.5 g/cm^3
Fiber	T300
Braid	24 x 1k rowing, $\pm 45^\circ$
Fiber volume ratio	50%
Coefficient of thermal expansion (CTE)	2 ppm/°C
Thermal conductivity	0.5 W/m°K

Table 17. Thermo-mechanical properties of the CF pipe.

4.2.3 Carbon foam

The carbon foam provides the thermal path to the cooling pipe. There are several different types of carbon foam with different thermal conductivities, as a function of the density; Table 18 shows the key parameters of the two carbon foams being considered. The choice of foam is a trade-off between the thermal performances of the stave and the overall stave mass.

4.2.4 End of Stave cooling connections

The transition from the in-stave boiling channel to the internal services is highly critical as any failure would prevent the operation of an entire stave. The End of Stave (EoS) region is however highly space-constrained, which excludes the use of standard fittings. The mating of the stave to the 2×3 m long pipes has implications for the module loading and integration work flow, as outlined in Section 5.1.

A full-custom connector based on the design used in the current Pixel detector has been studied. Important requirements include sustaining 10 mating cycles, leak tightness over the full temperature range, and a maximum outer diameter $OD < 10$ mm. Initial prototypes have successfully passed leak rate tests, however a full qualification remains to be done.

Considering a number of permanent connection technologies, orbital tungsten inert gas (TIG) welding seems particularly well suited for the EoS transition, and are already considered as qualified with respect to tightness and reliability. There are however serious concerns about any type of arc-welding in close proximity to potentially ESD-sensitive detector modules. In spite of the

Item	**Symbol**	**POCOGRAPHITE Low Density**	**Koppers KFOAM L1 250**	**Unit**
Density	ρ	0.55	0.245	g/cm^3
Thermal expansion	CTE	-0.7/+0.6	2	ppm/°K
Thermal conductivity	°K	135/45 ($\parallel$ / $\perp$)	30	W/m°K
Compress. modulus	E	0.373	0.894	Gpa
Compress. strength	$p^{\max}$	3	9.9	Mpa

Table 18. Main thermo-mechanical characteristics of the two carbon foams considered for the design of the IBL stave.

obvious complications for the subsequent work flow, the current baseline is therefore to complete the TIG-welding prior to module loading.

4.2.5 Design choice

The composite pipe has several advantages that mitigate its more complex fabrication process. Its CTE is well matched to that of the surrounding composite structure, resulting in a minimal deformation during the cool-down. The contribution in terms of % X/X_0 to the mass budget is also expected to be lower than for a metallic pipe. However, these benefits are somewhat offset by the fact that the CF fiber pipe has a minimum achievable inner diameter of 2.4 mm while the optimum diameter for the current application is about 1.5 mm. Furthermore, the thermal performance of the CF pipe stave turns out to be marginal. The transverse thermal conductivity of the composite laminate is dominated by the matrix, and has been measured to $0.5\ \mathrm{W/mK}$, to be compared to the Titanium thermal conductivity of $16.4\ \mathrm{W/mK}$, see Tables 16 and 17. The resulting thermal figure of merit of the stave is significantly worsened by the CF pipe due to a significant ΔT across the pipe wall.

Table 19 compares the parameters of the two stave options considered for the optimisation of the design. The following considerations shall be taken into account:

Radiation length X/X_0: the radiation length is given for the stave with and without modules and services. The assumptions on the thicknesses used for the estimate are: 250 μm and 90 μm for sensor and FE chips respectively, and $X/X_0 = 0.18\%$ for the on-stave electrical services.

Thermal figure of merit: the thermal performance of the stave is characterized by the thermal figure of merit,

$$\Gamma = \frac{\Delta T}{\delta p}\ \left[^{\circ}\mathrm{K}\cdot\mathrm{cm}^2/\mathrm{W}\right] \tag{4.1}$$

where ΔT is the temperature difference between the sensor and the inner pipe wall, and δp is the area density of the module power. Multiplying this value with the power density $\delta p\ \left[\mathrm{W/cm^2}\right]$ entering into the stave from the carbon foam, gives the temperature difference between in the inner surface of the boiling channel and the sensor; see also Eq. 10.2.

In order to obtain the total ΔT between the sensor and the boiling fluid, the contribution of the convection should be added. This can be calculated by means of the Heat Transfer Coefficient (HTC). In case of the CO_2 cooling at the evaporation temperature $T_{\mathrm{ev}} = -40\ ^{\circ}\mathrm{C}$ and at a nominal flow rate of $2\ \mathrm{g/s}$ the convection ΔT is:

$$\Delta T_{\mathrm{conv}} = \delta P \cdot \mathrm{HTC}, \tag{4.2}$$

where the $HTC = 6.000\ \mathrm{W/m^2\cdot K}$, and δP is the area density of the power at the inner surface of the boiling channel.

For the 2 mm ID Ti pipe stave, the δP is $2.2\cdot 10^4\ \mathrm{W/m^2}$ and the convective contribution $\Delta T_{\mathrm{conv}} = 3.5\ ^{\circ}\mathrm{K}$.

The Γ-values in Table 19 are from FEA simulations. Preliminary results on prototypes of stave have shown a difference of about 30%, indicating an overestimation of the thermal performances by the FEA.

Item	Symbol	Ti Pipe	CF Pipe	Unit
Omega thickness	d	300	150	μm
Foam density	ρ	0.25	0.25	g/cm^3
Pipe material		Ti Grade 2	CF	
Pipe diameters	ID/OD	2.0/2.2	2.4/3.0	mm
Material	bare/assy	0.57/1.166	0.36/0.956	% X/X$_0$
Thermal figure of merit	Γ	10.2	25	$^\circ$K$\cdot$cm^2/W
Thermal deformation	δ	41	50	μm

Table 19. Comparison of the thermal and mechanical performances of the two stave design options.

Thermal deformation: the values in Table 19 give the sag induced by the cool down (from $+20$ °C to -40 °C) as calculated for the stave supported on its final mounts. The deformation is induced by the CTE mismatch. The predicted values are largely within the specification indicated in Table 15.

Mechanical integrity: the mechanical integrity has been verified using FEA simulations, considering the stress induced by the pipe pressurization at 100 bar and by cool-down, applying to the following reference safety factors:

- Titanium pipe:

  Maximum tensile/compressive stress

  Maximum Von Mises stress

  Safety Factor (SF) of the pipe (yield stress / max Von Mises stress): SF ≥ 2

- CF pipe:

  Maximum tensile/compressive and transverse shear stress for each ply

  Maximum transverse strain for each ply: $\varepsilon_t \leq 0.1\%$

  SF of the pipe calculated by the Tsai-Hill failure criteria: SF ≥ 4

- Foam:

  Maximum tensile/compressive stress

  Maximum Von Mises stress

  SF of the foam (comp. strength / max comp. stress): SF ≥ 2.

- Adhesive:

  Maximum shear stress

  SF of the adhesive (ratio shear strength / max shear stress): SF ≥ 1.5

Table 20 summarizes the stress and the safety factors as simulated. More information is available elsewhere [71].

Stave type	**Load**	**Pipe von Mises or Tsai-Hill stress**		**Foam compression stress**		**Adhesive shear stress**	
		MPa	SF	MPa	SF	MPa	SF
Ti pipe Stave	$\Delta T = -60\,^{\circ}\mathrm{C}$	57	5.9	-0.9	11	1.9	5.4
	MDP = 100 bar	102	3.3	-0.4	28	0.6	15.6
CF pipe Stave	$\Delta T = -60\,^{\circ}\mathrm{C}$	-	-	-0.8	13.2	4.0	2.5
	MDP = 100 bar	$\sigma_{\parallel}^{\max} = 108$ $\sigma_{\perp}^{\max} = 8.7$ $\tau_{\mathrm{lt}}^{\max} = 10.1$	3.9	-2.3	4.2	5.3	1.9

Table 20. Simulation results for the stresses in the various parts of the stave under the pressure and cool-down loads.

In conclusion, the baseline for IBL is the titanium pipe stave. This gives much larger headroom for the thermal performance while avoiding the technological complications of the CF pipe. As previously mentioned, the titanium pipe is not optimal for the material budget, but the difference appears marginal.

4.2.6 Stave qualification plan

The stave qualification plan is documented in [72], the main qualification issues are outlined below.

Qualification of the titanium pipe and welding: the bulk material of the Ti pipe has been inspected to reveal systematic production defects; the thin wall can turn out defective and leaky due to flaws in the drawing process or to an excessive size of the metal grain compared to the pipe thickness. Metallurgic inspections have been performed on Ti Grade 2 by the metallurgic service at CERN (EN/MME-MM), showing a good material bulk homogeneity without evident defects [73].

All the pipes have been pressure tested at 150 bar and leak checked with helium at the level of 10^{-7} atm$\cdot$cc/s, as it has been specified in the requirements, Table 15.

The techniques considered for the permanent joints between the boiling channel in the stave and in/out lines are fusion welding (EB/Laser and TIG). The qualification of such welds are on going and follows the standard level B of ISO 13919-1 [74].

Measurement of the thermal performance: a campaign of measurements has been launched to evaluate the conductive thermal resistivity of the stave and the HTC of the boiling fluid. Samples of staves with different pipes and designs have been loaded with silicon heaters and connected to CO_2 and C_3F_8 cooling systems. The thermal figure of merit will be measured on irradiated and thermally cycled samples in order to reveal degradation of the thermal performances.

Preliminary tests have shown thermal figures of merit that are about 30% worse than the simulations. Initial evidence indicates the problematic areas being the interface between the cooling pipe and the carbon foam and, for the case of the CF pipe, its transverse thermal conductivity. Further measurements are in progress to better understand the nature of the mismatch and to improve the modeling in the simulations.

Measurement of the bow during the cool down: the expected stave sag induced by the cool down will be directly measured on few prototypes by means of an optical survey; the stave is supported on its final mounts and cool down in an environmental chamber, its deformation is measured and compared to the simulated value to qualify the stave for the geometrical stability budget as indicated in Table 15.

Mechanical qualification of the pipe-foam interface: the validation of mechanical integrity under the considered loads is performed according to the protocols outlined in [72]. Eventual failures of the adhesive layers between the boiling channel and the foam can be detected by comparing the thermal figure of merit before and after 100 thermal cycles between $+30$ °C and -50 °C.

4.3 Electrical Concept

The on-stave type 0 electrical services connect the Modules (Chapter 3) to the type I internal services (Section 4.5) at the EoS. Due to material budget and space constraints the services have to be tightly integrated with the stave itself, causing a number of important electro-mechanical concerns, such as thermal issues, implications for the stave loading process, and aspects related to stave rework.

On the electrical side, a major challenge is the transmission of 160 Mb/s data across the stave to the EoS, and 6 m onwards to the opto-boards at PP1. It is expected that reliable links can be achieved by carefully matching the transmission impedance of each section. Signal integrity and transmission quality are being evaluated by means of realistic full-chain bit error rate test set-ups at several collaborator sites. Equally challenging is keeping the low voltage (LV) drop within budget, as set by voltage regulators and front-end ASIC operating conditions. In order not to inflate the total material the LV conductors will be in aluminium.

4.3.1 Requirements and reliability

The detailed specifications for the on-stave high-density interconnect are listed in Table 21. Since the flex is potentially a single point of failure for the entire half stave, its reliability is of critical importance. This has obvious implications for the design itself, as well as for the choice of implementation technology, the quality assurance planning, and the assembly procedures. Industry standards [75] will be applied as appropriate, noting however that there is no specific standard for aluminium flexible circuits.

4.3.2 Layout and envelope

A single stave is served by two flex buses, one from each end, running along the back side of the stave, i.e. facing away from the interaction point. The connections for each module branch off into a *wing* and pass around the edge of the stave to make contact with the module pigtail. The topology is outlined in Fig. 69, adapted from [68].

As each half stave is served by a separate bus there is no routing past the global support at $z = 0$. The situation at the stave ends is somewhat more complicated; the flex must be narrowed in the ϕ-direction in order to clear the stave support, then curve to a smaller radius in order to connect with the Type-1 services, see Section 4.5. Since the flex is manufactured as a flat sheet it cannot curve in more than one direction, and its transverse cross section must be straight.

Item	Symbol	Value	Unit	Remark
1 Mechanical				
1.1 Dimensions				
1.1.1 Thickness	d	< 0.7	mm	Laminated on stave
1.1.2 Radial envelope	IR	> 32	mm	Design value
1.1.3 Axial length	l	< 320	mm	Middle of stave to end
1.2 Thermal				
1.2.1 Minimum temperature	$T^{\min}$	-60	°C	Back-pressure loss
1.2.2 Maximum temperature	$T^{\max}$	$+80$	°C	Bake-out
1.2.3 Nominal thermal load	ΔT^0	-60	°C	from -40 °C to $+20$ °C
1.2.4 Maximum thermal expansion	CTE	4	ppm/°K	Stave support structure
2 Electrical				
2.1 Low voltage				
2.1.1 Granularity	$N_{V_{\rm dd}}$	2	#	Type-1 granularity: 4
2.1.2 Nominal current	$I^0_{\rm dd}$	0.59	A	Per FE-I4
2.1.3 Worst case current	$I^{\max}_{\rm dd}$	0.91	A	Per FE-I4
2.1.4 Voltage drop	$\Delta V^0_{\rm dd}$	< 200	mV	Round-trip, nominal
2.2 High voltage				
2.2.1 Granularity	N_{HV}	2	#	
2.2.2 Maximum voltage	$V^{\max}_{\rm HV}$	1000	V	Pending sensor
2.2.3 Test voltage	$V^{\rm test}_{\rm HV}$	1500	V	Pending sensor
2.2.4 Insulation	$R^{\min}_{\rm HV}$	> 100	GΩ	$V^{\rm test}_{\rm HV}$, 20 °C, 40% RH
2.3 Downlink				
2.3.1 Clock granularity	$N_{\rm cmd}$	2	#	Multidrop
2.3.2 Clock frequency	$f_{\rm clk}$	40	MHz	
2.3.3 Command granularity	$N_{\rm cmd}$	2	#	Multidrop
2.3.4 Command data rate	$f_{\rm cmd}$	40	Mbps	NRZ, not DC-balanced
2.3.5 Impedance matching	Z	80	Ω	Pending type-1
2.4 Uplink				
2.4.1 Uplink granularity	$N_{\rm data}$	1	#	
2.4.2 Uplink data rate	$f_{\rm data}$	160	Mbps	8-10 encoding
2.4.3 Impedance matching	Z	80	Ω	Pending type-1
2.5 DCS				
2.5.1 DCS granularity	$N_{\rm DCS}$	4	#	

Table 21. High-density interconnect specifications.

The preferred way of attaching the flex to the stave is by continuous lamination; this guarantees that the entire object stays inside the imposed envelope, and eliminates the point stresses associated with discrete attachments. However the CTE of the Cu/Al/polyimide circuit is expected to be poorly matched to that of the stave. The thermally induced stress must therefore be absorbed by the mechanical structure without it exceeding the very tight deformation limits. Studies are underway

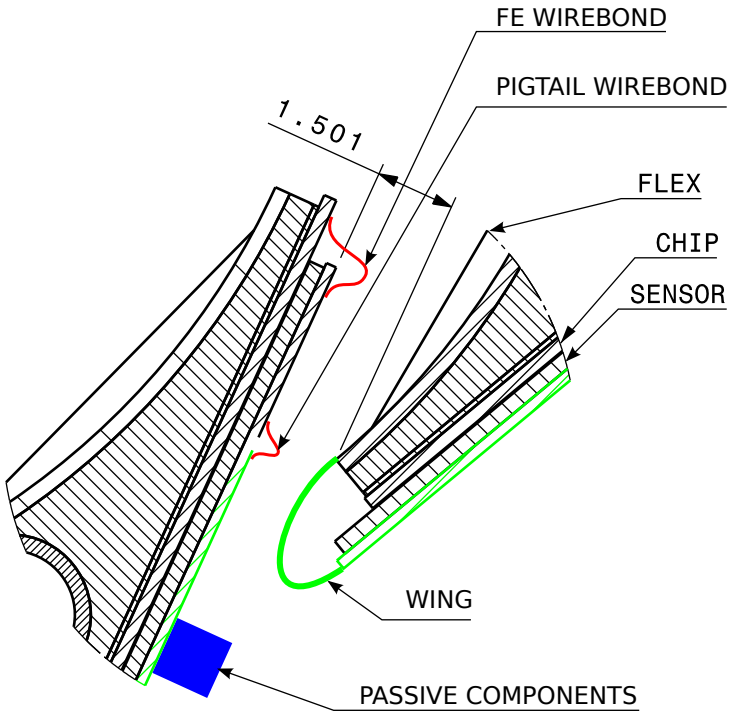


Figure 69. Type 0 services topology and stave-to-stave clearance. The wing (green), which is an integral part of the flex, is glued onto the sensor after loading, and connected to the module pigtail using aluminium wedge bonding (red). The passive components (blue) have to be low profile in order to fit within the module envelope.

to evaluate the impact of the flex on the stave bowing.

4.3.3 Flexible bus

Two alternative designs are described: a multi-layer approach, which relies on copper and aluminium conductive layers and via interconnects, and a stacked single-layer design, which uses tape automated bonding (TAB) [76] for cross-layer connections as well as for attaching solderable component carriers.

The multi-layer flex is built using six layers interleaved with polyimide dielectric layers. There are five signal- and HV layers using copper conductors, while the two LV layers use aluminium for minimum material. Routing between layers is available using vias, this implies that LV, HV and signals can be completely regrouped at the EoS. The *wing* part, which folds around the stave edge and connects to the module, is implemented in a single Cu-conductor layer. A prototype layout is shown in Fig. 70.

The single-layer flex concept employs a staggered set of eight identical flex cables for each half stave, each serving a logical module, i.e. two FE-I4s. Each cable is implemented using a single aluminium layer, sandwiched between two layers of ultra-thin polyimide. Cross-routing, required by e.g. the multi-drop clock and command signals, is achieved by implementing the *wing* as a separate object which is TAB-bonded to the main bus (Fig. 71(a)). Stacks of flex cables will be laminated, attached to the stave and tested on-stave before module loading.

The multi-layer as well as the stacked single-layer flexes are currently being prototyped and evaluated. Assuming both technologies eventually qualify in terms of manufacturability, reworkability and reliability, it is expected the overall material budget will have a strong weight in deciding between the available options.

4.3.4 Qualification and testing

As the long-term reliability is a prime concern for the flex, it is important to specify a relevant prototype qualification plan, as well as stringent production quality assurance and test procedures. Two important concerns are damage due to repeated bending, and the stress induced during thermal cycling.

A particular problem with Al/polyimide flex circuits is that aluminium conductors that are plated for soldering become brittle and crack during handling. The two designs described here eliminate the problem by not requiring plated conductors in the flexible sections: the multi-layer flex has soldered components only on the top Cu-layer, the single-layer flex uses separate Al/polyimide component carriers that are TAB-bonded to the main flexible circuit.

Bending: prototype flex cables will be test-bent and inspected for micro-cracks. For assembly, tooling and handling procedures will be designed to ensure that the manufacturer's minimum bending radius is not exceeded, and that the number of cycles is kept at a minimum.

Thermal cycles: as a first step, electrically working flex prototypes will be subject to standalone thermo-mechanical tests. However, the eventual thermo-mechanical qualification will require a number of stave/flex assemblies to survive a few times the lifetime-expected number of full thermal cycles.

Production QA: the vendor is expected to ship fully tested and working items, documented according to the relevant industry standards [75]. On reception, the flex will be subject to burn-in at an elevated temperature, cycled once through the full thermal range, and electrically tested, prior to assembly on the stave.

4.4 Module Loading

The module loading consists of populating a stave with individual functional modules such that the

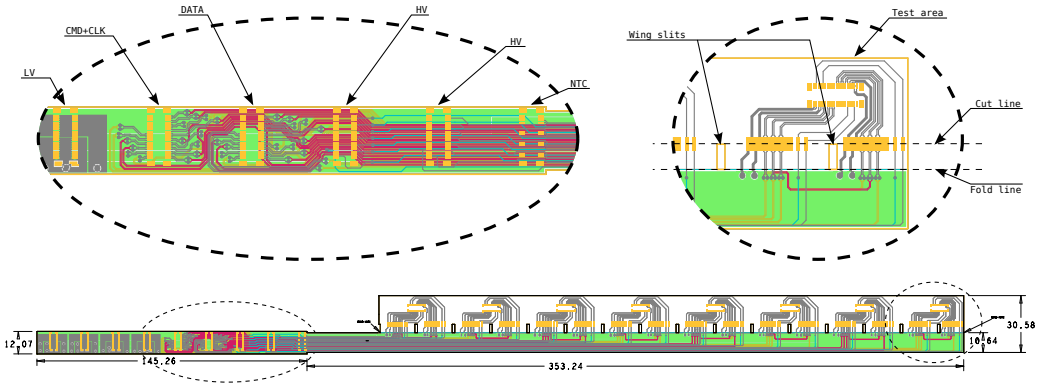
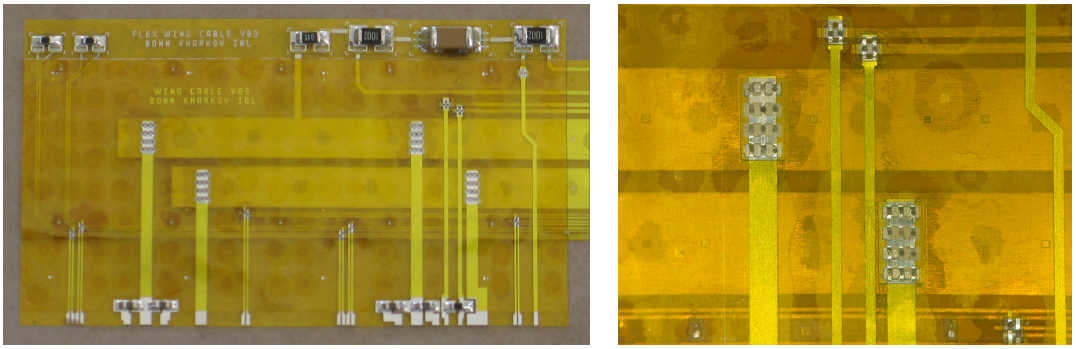


Figure 70. Multi-layer Cu/Al/polyimide flex circuit layout. The wings, i.e. the area between the fold line and the cut line, are separated by mechanical slits; the area above the cut line is for prototype testing only.



(a) Bus and wing interconnect (b) TAB detail

Figure 71. Single-layer flex prototype. The flex bus and the wing are manufactured separately then connected using TAB-technology.

final product is a fully integrated mechanical, thermal and electrical unit of the final detector. The loading, as well as the subsequent integration and commissioning steps, will take place in the clean room of the ATLAS surface building SR1. For this activity important engineering and R&D efforts are still in progress.

4.4.1 Assembly sequence and QA

Figure 72 summarizes the assembly and test flow during the stave loading activity. Quality assurance steps will be carried out at various stages of the stave assembly flow, as shown in the figure.

The assembly sequence starts with the reception of the main items like modules, the bare stave and the electrical service tape. Each item follows a reception procedure consisting of a visual inspection, electrical test integrity of modules and service tapes, metrology survey of bare staves, and leak tightness tests of the encapsulated cooling pipe.

The module loading starts as soon as enough components are locally stored and accepted in the reception tests. The loading activity consists of mounting consecutively all of the 16 or 32 modules, depending on the module size, with a well defined assembly technique (see Section 4.4.2). Once completed, the stave is probed electrically, before the connection of the module pigtail to the flex is made. A series of electrical tests, metrology survey and thermal cycling will be made to finalise the quality assurance. The metrology allows tracking the *xzy*-module position and can serve to identify possible anomalies after the thermal cycling. The thermal problems may also be identified by monitoring the module temperature for a given power and cooling condition. Repairs are possible at several stages of the whole process; some rework options are discussed in Section 4.4.4.

4.4.2 Module loading and tools

The stave loading for the IBL is being developed based on two approaches: i) the robotic system used for the original Pixel project module loading, which is a 6 degrees of freedom (DOF) robot with 4 motorized axis and 2 manually adjustable ones (Fig. 74), and ii) a new tool based on a cradle and mechanical references for stave and the module edge contact, that would avoid a metrology system while loading (Fig. 73). This system uses a set of jigs to mechanical reference both the

stave and the module to the precisely machined cradle. The final solution will combine the best features of these two approaches and will require further work and optimization.

For the modules loading, the following steps are needed:

1. Fixation of the stave on a cradle with the mechanical references of the structure.

2. The glue or grease is dispensed on the targeted place of the stave using motorised stage for short travel distances, or by hand if found to give satisfactory results.

3. The module is taken either with the robot manipulator system by sucking the module top side and by integrating pressure gauge, or using a manual handling jig.

4. The module has to come against the mechanical references in place on the cradle. With the robot this can be done via pressure gauge signal when the module edge is touching the mechanical reference pins.

5. All the odd modules are first assembled relative to reference pins versus the module edges.

6. The even modules are inserted with the same technique as in a rework procedure (using the insulating shims as guides). When using the manual handling jigs, the module is pushed against the reference pins in the lateral direction. In the case of the robot head, the references

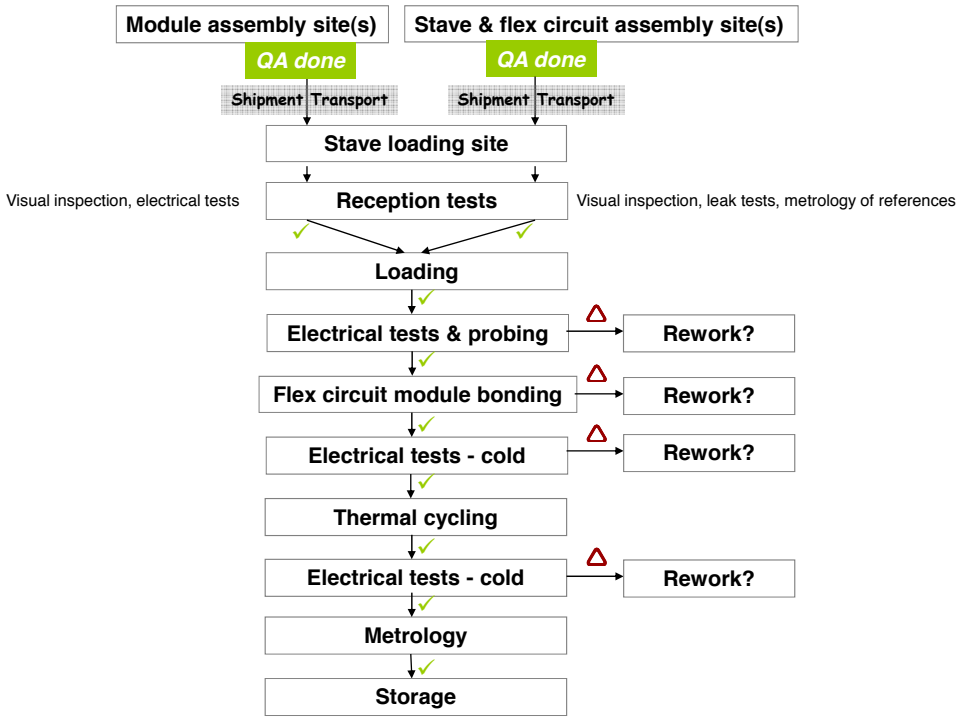


Figure 72. The planned assembly and test flow during the stave loading activity.

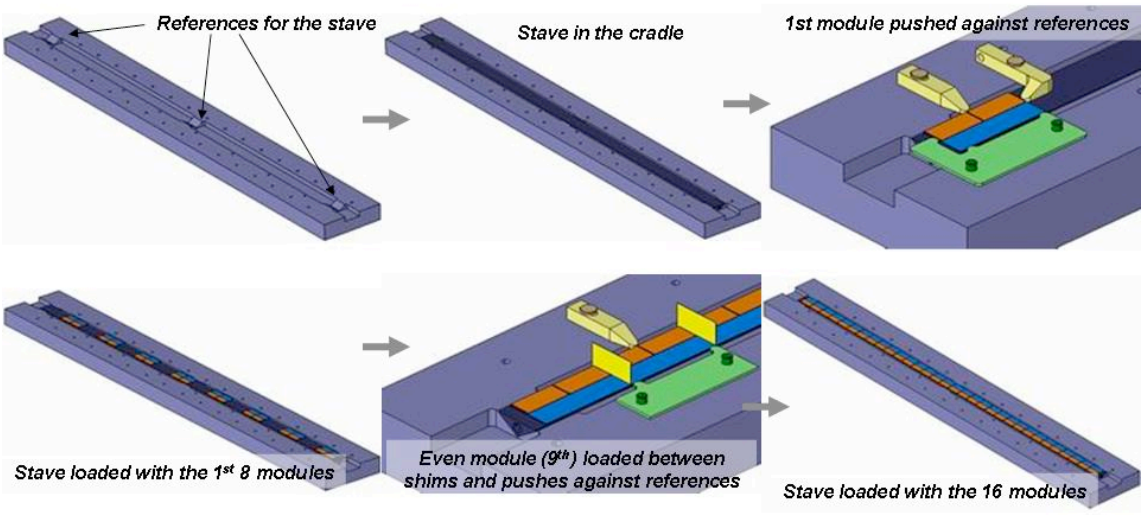


Figure 73. Illustration of the sequence for module loading using a cradle and mechanical references, for both the stave and the modules.

Figure 74. Pixel loading robot (left) and glue deposition tool (right).

will be taken against the reference pins when the pressure gauge sign is given. Shims are left glued for the module-module electrical insulation.

For the curing of the glue, which may take several hours, the module will be left in place with a calibrated load in order to free the robot or handling manipulator.

4.4.3 Assembly requirements

The module loading is carried out in a strictly controlled environment, employing best practices with respect to temperature, humidity control, and electrostatic discharge protection. Elevated temperature curing is not permitted and module manipulation is exclusively carried out with dedicated tools. The target is to achieve a loading yield close to 100%, at a rate of 2 weeks per stave. This time estimate accounts for all operations, from the individual reception tests to the final stave QA

[77]. If the tasks are paralleled, the total time for all the 14 to 15 staves can be reduced significantly.

Assembly tolerances

z loading accuracy: in Eq. 4.3, Z_M is the module z coordinate and G the inter module gap on stave, as shown in Fig. 75.

$$\Delta Z_M = \pm\left(\frac{G}{2} - S\right) \tag{4.3}$$

G has a high influence on the accuracy which has to be achieved during the module loading. The safety margin S could be reasonably set to 0.01 mm. If $G = 0.05$ mm, then $\Delta G = \pm 0.015$ mm. Over the 800 mm stave length this value seams difficult to achieve. Taking $G = 0.1$ mm, $\Delta G = \pm 0.04$ mm. This sets the value close to the tolerance achieved for the module loading of the current ATLAS Pixel detector.

x loading accuracy: the X_M (module x location in stave frame) value tolerance depends on the overlap between two staves in the ϕ-direction and the stave assembly accuracy (X_S in the barrel frame). The IBL detector layout gives an overlap of 9.6 pixels in *Phi* direction. The minimal allowable overlap is one pixel (0.05 mm) to provide an optimal coverage in the Phi direction. Symmetry of the tolerances will be assumed. Therefore, the 0.48 mm distance D can be tolerance as $D = (0.48^{+0.43}_{-x})$ mm. The D tolerance is driven by ΔX_M and ΔX_S, as $\Delta D = 2 \times \Delta X_M + 2 \times \Delta X_S$. A first approach consists of considering that $\Delta X_M = \Delta X_S$, $\rightarrow \Delta X_M = 0.053$ mm. This value is highly constrained by the stave assembly accuracy; relaxing the stave assembly tolerance will increase the accuracy needed on the module placement.

y loading accuracy: this module coordinate is mainly constrained by the glue layer. The glue thickness is typically 0.1 mm; however most thermal glues contain thermally conductive particles of a given size, typically 0.04 mm. The minimal tolerance of the thickness can be deduced from this value. The maximal thickness tolerance is less constrained. A value of $Th^{+0.1}_{-x}$ is proposed, and y = Th - (fillers particles maximal size + 0.01 mm + safety margin).

Module attachment

The interface layer between IBL staves and modules has three main functions: i) electrical insulation, ii) thermal coupling, and iii) module fastening on stave (see electrical and thermo-mechanical specifications in Table 22).

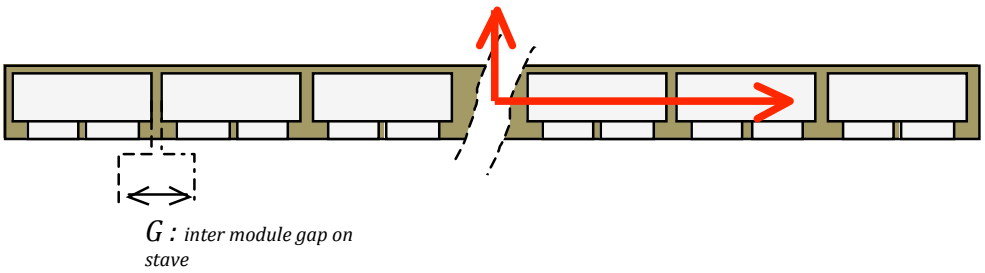


Figure 75. Module on stave top view scheme.

Thermal conductivity	$> 10000\ \mathrm{W/m \cdot K}$
Volumetric resistance	$> 10^{10}\ \Omega\mathrm{cm}$
Polymerization temperature	Ambient
Dielectric strength	$> 10\ \mathrm{kV/mm}$
Dielectric constant	≤ 6
Shear strength	> 8 MPa

Table 22. Deposition requirements.

Two design options are therefore possible: using an unique compound thermal glue or a two compound layer, a thermal paste coupled with glue dots (Fig. 76). The advantage of using only the glue as the thermal interface is not obvious when considering the rework ability of replacing modules. Likely the glue layer will enter and close the porosity of the PocoFoam, hence breaking the glue link over the all module backplane surface may seriously damage the stave foam in this region. The second option of using stable and pasty thermal grease is considered possible, provided that the mechanical stability of the module is ensured by some glue drops. The two options are currently under detailed investigation and the more convenient one will be qualified in terms of the thermal and mechanical stability, as well as the rework ability.

The principal risk of the glue/grease deposition is the pollution of the Pixel region by capillarity absorption in the inter-chip region. Any product in this region will induce parasite capacities, which would increase the noise in the Pixel modules. Having the lowest possible dielectric constant and a high electrical resistivity are therefore important selection criteria. Moreover, the glue/grease deposition will be restricted to the chip, minus a safety factor. Usually the covered surface will represent 60 to 95% of the chip area.

4.4.4 Rework options

For the current ATLAS Pixel detector, about 10% of the pixel staves had to be repaired by replacing one or several modules during the production phase. This does not take into account the staves which had to be repaired by remaking module wire bonding on a loaded stave. Damages can occur at any stage of the detector assembly and therefore a realistic repair plan has to be foreseen. Several actions are considered for the IBL:

1. Replacing a module after connection to bus cable to be able to remove a module after glue polymerization, and to disconnect and reconnect a module from/to the bus cable.

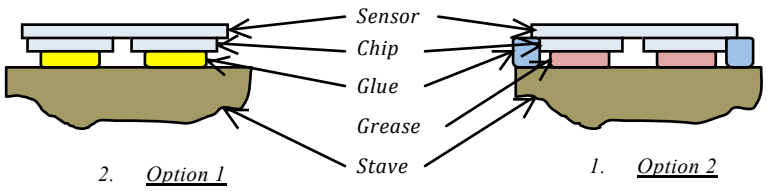


Figure 76. Module attachment options.

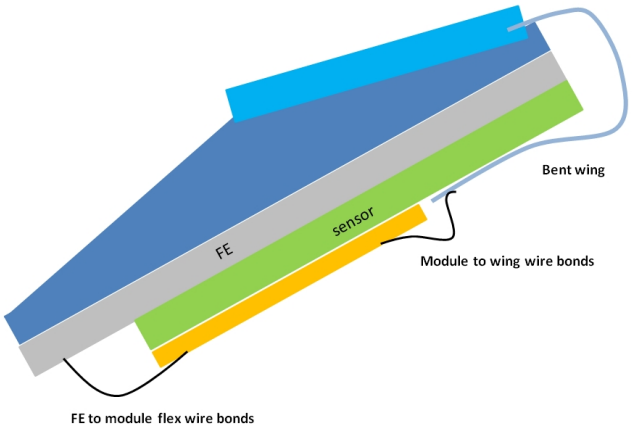


Figure 77. Stave flex to module attachment via a kapton wing and wire bonds.

2. Replacing a damaged stave by a new one. If enough spares are foreseen, option 1) might not be needed.

3. Repairing wire bonds on a loaded stave.

4. Replacing a bus cable.

Option 1) is highly dependent on the module attachment method and the compounds used. Soft glue was used in the current Pixel detector, therefore removing a module consisted of cutting the glue with a thin Tungsten wire. For the IBL, several alternatives will be studied.

4.4.5 Interfaces

This section describes the most important interfaces between the module and stave and the stave and its services.

Flex

The electrical interface to a module is made by a type 0 service tape. Each module is electrically linked to a tape via an extension wing that runs from the tape at the back of the stave *Omega* shape, and is bent towards the top module side and then glued (Fig. 77). The electrical connection is made by wire bonding between the wing and the flex hybrid that was already assembled on the module at an earlier stage. In terms of quality, the wire bonding process has to be reliable and the glued surface should be free of air bubbles below the wing; the gluing technique should also be reliable and reproducible. The first tests carried out on dummy silicon modules where the top surface is glued with copper gold kapton show excellent pull strength forces. Further efforts are being made to get rid of air bubbles.

Chip and sensor edges

The chip and the sensor cutting edge precisions are critically depending on the module layout and

the module to module distance along the z-axis. The expected distance between two modules along z is 100 μm (Fig. 78), in case of a single chip to sensor module, and 200 μm in case of 2 chips for 1 sensor. In addition, an insulating material, like polyimide, will be located in this inter-module gap. Therefore the cutting edge accuracy relative to the fiducial or alignment marks must be below the remaining distance when taking into account the placement accuracy and the thickness of the insulating polyimide between the two modules.

A polyimide insulator of 30 μm and a maximum module placement accuracy of 40 μm can lead to module loading clashes. If the module placement accuracy is 20 μm, then the remaining cutting accuracy has to be 15 μm. Given the tight numbers for the placement accuracy it is therefore specified that the item which defines the outside module enveloped in z will have to be diced with an accuracy of $\pm$10 μm. The cutting edge can also be used in one of the assembly techniques being studied in order to ensuring an optimal module placement accuracy.

Stave to module interface

The stave to module interface is an essential part of the assembly. It is defined by the thermal, electrical and mechanical specifications. Concerning the thermal performances, the glue or grease interface should have a thermal conductivity above 0.6 W/m°K, or even close to 1 W/m°K. The choice of the thermal interface should not be only based on the thermal conductivity but also the viscosity, practicalities and its radiation hardness. Therefore various compounds are being investigated with thermal fillers such as AlN, boron, or metal oxide. The filler have the role to increase the thermal conductivity in a range of 0.6 - 1.5 W/m°K. For the thermal performance it is of major importance that the glue or grease on the chip backplane is thin.

For what concerns the electrical specification, an electrical insulation is needed between the carbon foam and the chip backplane, in addition to an electrical insulation from the detector edges to the carbon foam. The distance from the detector edge to the stave plane can be as close as 350 μm, which is not a safe distance for the breakdown voltage in some of the detector technologies. Therefore, the stave should be coated with a Parylene layer [78] of about 10 μm. This will have to be investigated together with the adherence of the glue or grease to this material, which is known to be slippery. The last requirement for this interface is that it should be stable during operation. Thermal cycling tests will be used to evaluate if the components are moving.

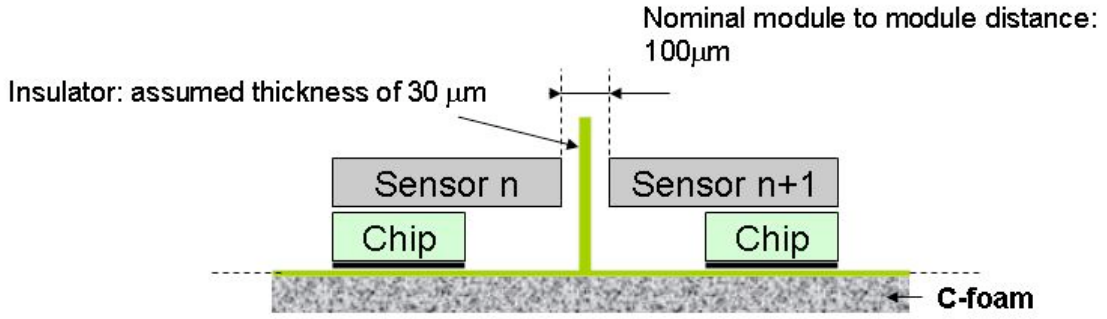


Figure 78. The module edge versus the module gap.

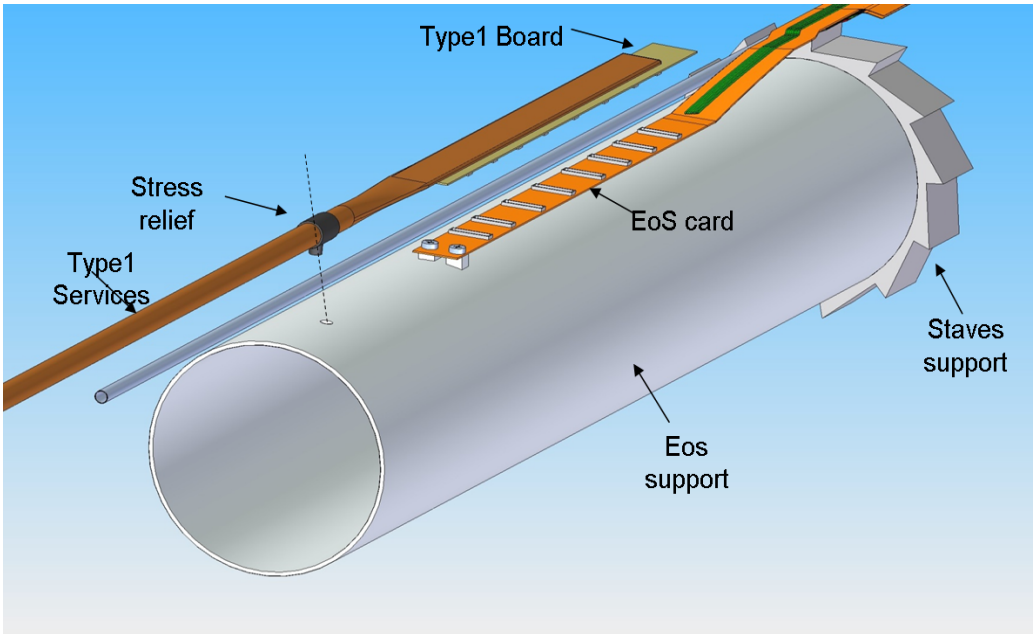


Figure 79. Stave flex and type I cable connection concept at EoS.

4.5 Internal Services

The design of the $\sim$ 3 m long internal (type I) services from the End of Stave (EoS) region to the PP1 at $z \sim \pm 3.5$ m on each side of the IBL detector has to meet the significant challenge of fitting into the very limited space available and also allowing a viable installation. The confinement for the internal services to a significant lower radius of < 4 cm compared to the existing pixel detector PP0 and service panel radius of $\sim$16 cm also demands a different data transmission strategy. The overall inner service design has adopted a passive EoS containing just a set of high density connectors to transition from the type 0 flex to type I wires.

The type I and EoS connection concept is illustrated in Fig. 79. The layout and dimensions of the EoS connectors are shown in Fig. 80. The fairly bulky type I cable bundle occupying space on the outer radii implies that the flex coming from the stave into the EoS region needs to dive down

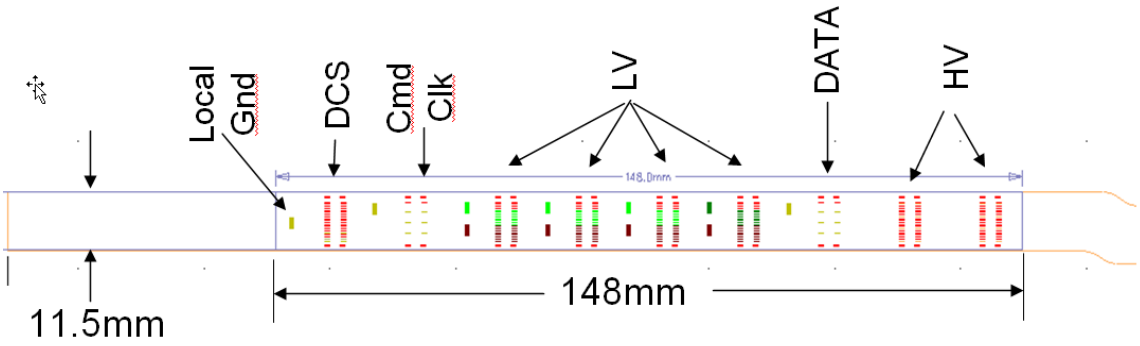


Figure 80. EoS connector layout.

to a lower radius to be supported on the EoS shell just outside the beam pipe. The "dog leg" bend in the flex in the EoS region is necessary to allow the flex to lower into the gap between the cooling pipes. An alternative connection scheme of soldering the type I and flex together and coil the type I bundle as a harness loop was also considered. This was later abandoned due to the bulkiness of the cable and connector ensemble and stiff LV wires making assembly and testing more cumbersome.

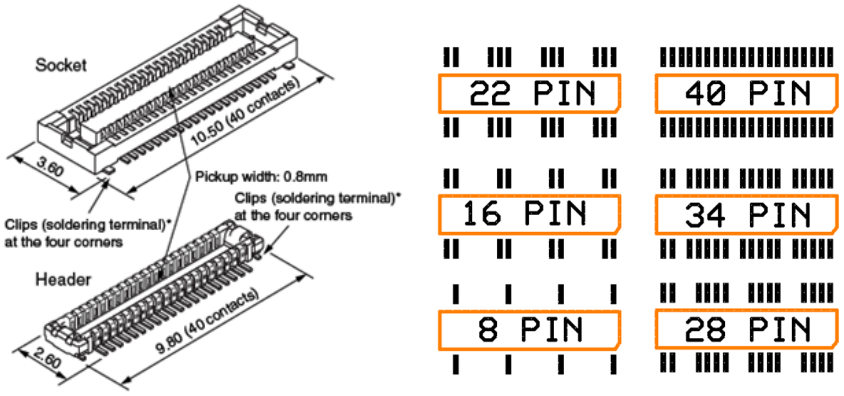
4.5.1 Low voltage powering

The inner service material is dominated by the LV supply wires to ensure a small enough resistance to avoid excessive voltage drop. Each FE-I4 has a nominal operating current of 0.6 A and expected final delivered voltage of 1.2-1.5 V at the front-end. The LV supply is organised in groups of four FE-I4s. The voltage regulators located at PP2 are connected through to the front-end first via the type II cables to PP1 region, then $\sim$4 m of type I cable to the EoS and finally 20-40 cm of type 0 flex cable to the FE-I4 modules. Among the various LV powering options the FE-I4 could potentially accommodate, direct powering would only allow a 0.6V voltage drop on the combined path of Type 0/1/2, while voltage regulators on FE-I4 would allow a voltage drop of 0.9 V. Having 1-to-2 DC-DC converters on FE-I4 could tolerate a drop of 1.33 V. The direct powering option is essentially ruled out just from the type I bundle cross section for fitting within the IBL envelope, besides the undesirable excessive material. The LV powering baseline is therefore working with the assumption of regulators on FE-I4 and a total voltage drop budget of 0.9V divided into 0.2:0.3:0.3 between type 0:I:II.

For the type I LV cables, copper-clad aluminium wires are used in order to minimise the radiation length of the system. Copper wires would be more compact and mechanically sturdy, but it takes a factor of ~ 2 in material radiation length to accomplish the same resistance. Out of concern of connect-ability and routing flexibility, the LV lines for each four-FE-I4 group are split into $4 \times$ AWG21 for each way of inlet and return. Each half-stave also has a in+return pair of LV sensing wires of the same diameter. The LV Hi-sense wire could have been thinner, but the concern of stress in a bundle has led to the uniform size decision. The LV sense wires terminate at the EoS. The LV and sense wires all have radiation hard quad polyimide insulation. Each LV+sense wire group of (4+4) takes up a 40 pin Panasonic AXT connector on the EoS, with the 0.6 A current on each AWG21 wire flowing into 4 pins on the EoS connector to be well within the current limit per pin of 0.3 A. The type I LV wire group will be a straight bundle without twist due to the lack of space and the rather rigid wires.

4.5.2 Sensor bias high voltage

The baseline HV supply requirement to accommodate the scenario of heavily irradiated planar sensors needing up to 1 kV of bias high voltage dictates much of the HV service considerations. The minimum spacing required for the HV connection points is the primary implementation issue. One measure to reduce the number of HV connection points is to not having separate HV return wires and just using the LV return as reference. The type I HV distribution is segmented to one AWG36 copper wire per two-FE-I4 module. The connection of the 8 HV feeds per half stave at the EoS is implemented on two separate 40 pin Panasonic AXT connectors of 4 groups each but with pins removed to meet the HV clearance gap. A set of tests are performed for various configurations of pin grouping/removal patterns as indicated in Fig. 81. The HV tests are conservatively done in



(a) Panasonic AXT connector (b) HV connector patterns

Figure 81. EoS Panasonic AXT connector and HV test pin patterns.

air up to 3 kV with 10 mA current per channel and with results summarised in Table 23. The 28 pin option with 1.2 mm gap between groups and still a fairly strong snap of the connector force appears to be the optimal choice. The HV connectors at the EoS are placed closest to the IBL detector as shown in Fig. 80 to make the earliest transition to type I cable to minimize the complication of a close placement of an open HV contact spot among other types of traces and connections at the dense EoS region.

4.5.3 Control and read-out

The control and readout signals lines have to be routed close to the beam pipe at low radius so that there is no viable means for optical transition until beyond PP1. The space limitation and radiation level concerns led to a position for the IBL opto-box at outer radius of the ID endplate. This requires a rather long $\sim$6 m electrical transmission between the EoS and opto-box which is a significant departure from the data transmission scheme of the present pixel system and with a significantly higher data transmission rate of 160 Mb/s.

The command and clock lines are one twisted pair of AWG36 copper wires each for a two-FE-I4 module with 1-to-2 multi-drop share between the two FE-I4s in the same module. These thin wires are adequate for the relatively slow 40 MHz signals. There is no material savings by going to aluminium wires as they cannot be thinner than AWG30 due to brittleness. The data signal lines are one twisted pair of AWG28 Cu-clad aluminium wires per FE-I4. The larger wire size here is

Configuration	HV held [kV]	Assembly force [kg]
8 pin	3.0	0.30
16 pin	3.0	0.45
22 pin	2.5	0.75
28 pin	2.5	1.10
34 pin	1.75	1.20
40 pin	Not tested	1.50

Table 23. EoS HV connector pin pattern tests.

necessary to ensure the data transmission quality at 160 Mb/s. Both control and readout twisted pairs have double quad polyimide insulation.

Given the central importance of validating the new data transmission scheme for the IBL, a dedicated test setup is built to test the various stages and options. The High Speed I/O (HSIO) board with a large variety of I/O connection ports is used as the digital control hub driving patterns and comparing the received data using the on board Virtex-4 FPGA. The control of the HSIO is through a multi-Gbit/s optical link to a Reconfigurable Cluster Element (RCE) ATCA DAQ board with extensive software support. A full electrical transmission chain is assembled for 16 data channels and 8 Cmd/Clk channels corresponding to a half stave. LVDS drivers designed for FE-I4 are mounted at 4 locations along 40 cm long flex cables previously used on the present pixel PP0. The flex LVDS pairs are vertically stacked with 75Ω impedance. The flex cables are connected to 6 m long twisted pair wires with micro Hirose connectors similar to the Panasonic AXT for the EoS. The Cmd/Clk and data twisted pair signals wires are connected to DORIC (see Section 6.5.1) and VDC ASICs respectively on the rear transition board of the HSIO. The clocks can switch between a commercial digital block to the PLL driver designed for the FE-I4. The data patterns can be driven single channel alone, all channels synchronously or asynchronously to test cross talk effects with the twisted pairs bundled together.

The Cmd/Clk path test was driven by DORIC with Bi-Phase-Marking at 40Mb/s and ran error free for the Bit Error Rate (BER) tests down to 4×10^{-13} level. The FE-I4 LVDS receivers were tested OK but the 1-to-2 multi-drop was not yet exercised. A detailed look at the eye diagrams indicated the latest 100Ω impedance twisted pairs gave much cleaner transmission than an earlier 80Ω version. The data signal BER tests with 8b/10b encoding were also error free up to 180 Mb/s but with rather little head room. The VDCs were verified to work at 160 Mb/s and appeared to be able to cope with voltage swings down to 50 mV level and still passing BER tests. Detailed examinations of the transmission eye diagrams were able to detect the influence of many factors degrading the transmission quality: reflections due to impedance mismatch between twisted pairs and the flex, reflections on the Hirose connector, cross talks between channels, and channel to channel variations. Detailed studies are still in progress to evaluate the adequacy of headroom and optimisation of impedance matching. As an example to illustrate transmission quality variations, eye diagrams for two different setups are shown in Fig. 82.

4.5.4 Monitoring

One temperature sensor on each two-FE-I4 module is served by a twisted pair of AWG36 copper wires. Four additional DCS environment signals per half stave are also served by same type of twisted pairs terminating at the EoS.

4.5.5 Interface to external services and supports

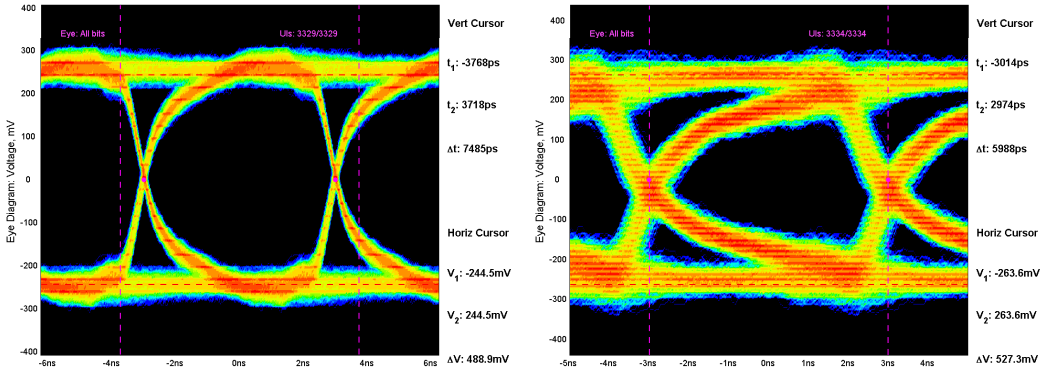
The type I service support at the EoS connections region is expected to be a carbon fiber cylinder as illustrated in Fig. 79, with the EoS connectors fastened by screws on the cylinder. The bundles for each half stave are expected to be potted near the EoS connection and sleeved with kapton or silicone. Along the length of the type I cables, supporting ring clamped to the beam pipe will provide the slots to hold the type I groups from each stave in place. An important requirement on the beam pipe construction is to have a split flange just beyond PP1 to allow the type I cables and

their PP1 end connectors to run over the low profile split flange to hide the type I end pieces inside the beam pipe envelope for the IBL installation which will thread the type I service bundle through the current pixel detector.

Unlike the current pixel detector quarter service panels with packed connections at PP1 transitioning to type II cables, the IBL type I services will not have the necessary space to make the type II transition all within the IBL radius. The PP1 end of the type I services therefore have to first turn onto the ID endplate to route toward larger radii until appropriate locations with opening for type II transitions are available. The precise locations for these transitions are still to be defined. The Cmd/Clk and data signal transition opto-box is expected to be as far of the outer radius of ID volume to result in 6m long type I services while other transitions are expected to be at lower radii. Some preliminary investigation of the connection mechanisms for the various type I to type II transition connections have been made. The lemo styled connector are found to be generally unsuitable for space and installation restrictions. Crimping and soldering in situ are also impractical as the PP1 area will be radioactive by the time of IBL installation. The preferred solution is currently high density board-to-board connectors. The type I service bundle cross section and the volume of candidate type II transition connectors are shown in Fig. 83.

4.5.6 Internal Service Summary

The type I internal service multiplicity and characteristics are summarized in Table 24 together with their smeared material radiation length contributions for tracks traversing perpendicular to the service cylinder radially. Among the total radiation length of 2.6%, the LV wires can be seen to be the largest material and cross section contribution at 1.7%. Establishing DC-DC conversion on FE-I4 will be a very effective means of reducing the internal service material and congestion.



(a) Single channel AWG28 twisted pair wires only with digital block.

(b) Multi-channel bundle AWG28 twisted pair wires + flex chain with FE-I4 PLL.

Figure 82. Electrical data transmission test eye diagram examples.

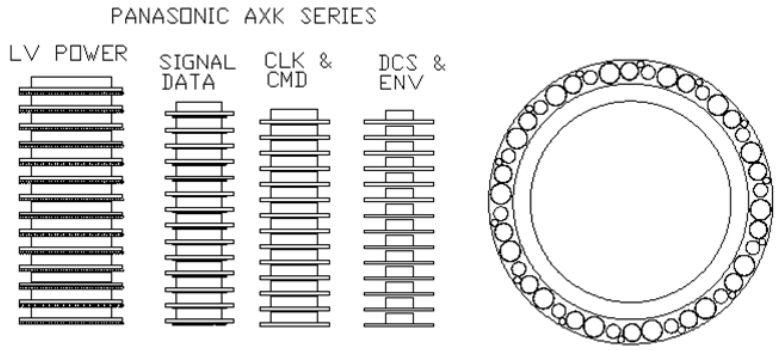


Figure 83. Type I service bundle cross section and candidate type II transition connector volume.

Electrical Element	**Count per half stave**	**Description**	**Wire OD [mm]**	**Insulation thickness [μm]**	**Packing Form**	**Rad.lenght** [%]
LV wire	2×16	AWG21 CC-Al	0.723	57	power bundle	1.58
LV sensing	2	AWG21 CC-Al	0.723	57	power bundle	0.10
Signal data	2×17	AWG28 CC-Al	0.321	84	twisted pairs	0.38
Clk+Cmd	2×17	AWG36 Cu	0.127	45	twisted pairs	0.21
DCS & Env	2×9	AWG36 Cu	0.127	45	twisted pairs	0.11
HV	8	AWG36 Cu	0.127	45	twisted pairs	0.05

Cooling Element	**Count/stave (2 sides)**	**Description**	**Pipe OD [mm]**	**Pipe wall thickness [μm]**	**Material Form**	**Rad.lenght** [%]
inlet pipe	1	Ti	1.2	0.20		0.06
outlet pipe	1	Ti	3.0	0.30		0.28
inlet fluid	1	CO_2	0.8	-	100% liquid	0.01
outlet fluid	1	CO_2	2.4	-	60% liquid	0.04

Table 24. Summary of type I services. Note that cooling pipes are the sum of both sides.

5. Integration

The integration of the IBL comprises the preparation of the beam pipe with IBL stave and services support rings, the mounting of the staves around the beam pipe and the final surface tests of the IBL prior to its installation in the pit. All these operations are carried out in the ATLAS ID integration facility, the SR1 building at Point 1. Details of the integration steps and the tests during this process are described hereafter.

5.1 Integration Process

The integration process is split in three phases: i) the preparation of the beam pipe with supports, ii) the mounting of the staves, and iii) the final survey and testing of the completed IBL package. Figure 84 presents a flowchart with the key integration processes to be executed in the SR1 facility.

1. Preparation phase:

   - The beam pipe is received at SR1 and installed in the IBL Integration and Testing Tool (ITT). This tool carries the beam pipe, IBL, internal services and PP1 during the whole integration process and final tests.
   - The stave and services support rings are mounted on the beam pipe. Collars, which position those rings, have already been fitted to the beam pipe before delivery.

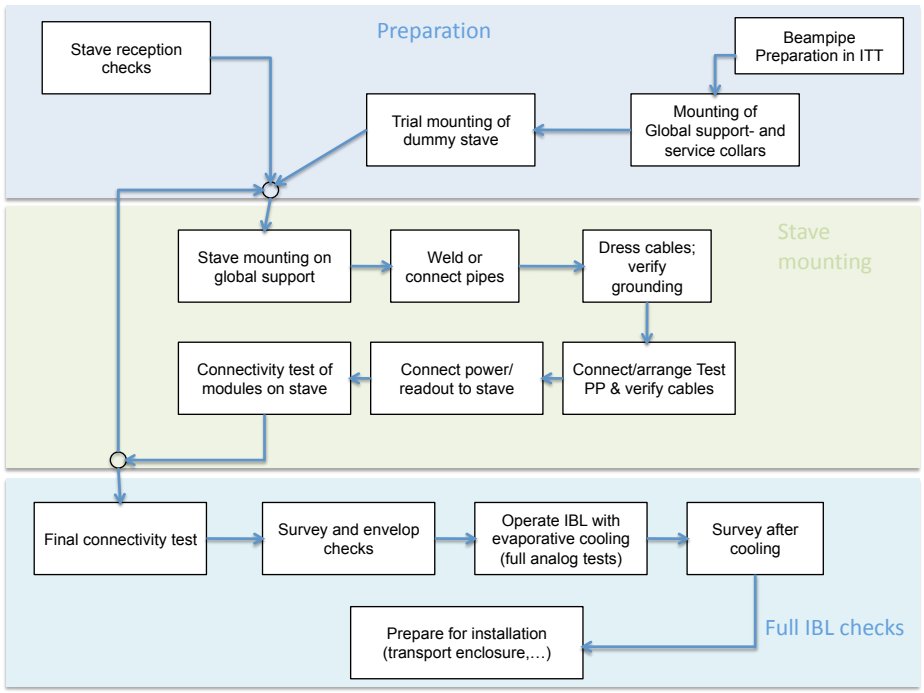


Figure 84. Flowchart of the IBL integration process.

- One or more mechanically precise dummy staves are fitted into each stave location on the stave support to check stave positioning, mounts and overall envelope. The dummy stave is fitted with services to verify the services manipulation and routing the PP1 at the end of the beam pipe.

The IBL staves are loaded with modules in the SR1, on fully-qualified CF-base staves. Currently it is assumed that the staves have a permanent connection of cooling pipes up to PP1, these being qualified on each stave before module loading. Electrical services, power and readout, are fitted from the EoS card to PP1 during the stave mounting. Module loading at the integration site avoids the necessity to shipping the staves between sites and the extra step of testing staves upon reception.

2. Mounting of staves:

   The mounting of staves on global supports around the beam pipe is shown schematically in Fig. 85.

   - The completed stave is lifted from its module loading frame with the Stave Mounting Tool (SMT) and positioned with guiding rods, which are referenced on the stave support rings in their final position on the stave support rings. The guiding rods allow to control clearances between staves during the mounting process.
   - Cooling inlet and outlet pipes are tied to the services support rings and their ends clamped in the PP1 feedthrough and service support rings.
   - Electrical services between EoS card and the PP1 feedthrough are dressed to the services support rings for the mounted stave. The services are fitted with a "loop-back" test card at the EoS end and a Test Patch Panel (TPP) at the PP1 end to check their electrical integrity in its final location before connection to the stave. The test includes ground isolation checks.
   - Electrical services are connected to both stave ends at the EoS card.
   - A connectivity test to each module (see Section 5.7) is carried out to check for open or shorted connection as well as module readout.

3. Full IBL package survey and test:

   - When all staves are mounted, a final connectivity test and grounding tests are carried out.
   - The position of all staves is surveyed and envelops are checked. A surface scan will be carried out for future reference and envelop checks. This survey is repeated after the final IBL tests, with cooling on, to measure positional changes before and after cool-down and warm-up.
   - After the survey is completed, the ITT and IBL package are enclosed in the testing enclosure that maintains a dry environment during the final tests. Test services (cooling for all staves, power and readout for two staves) are connected to the TPP and powering and readout system.

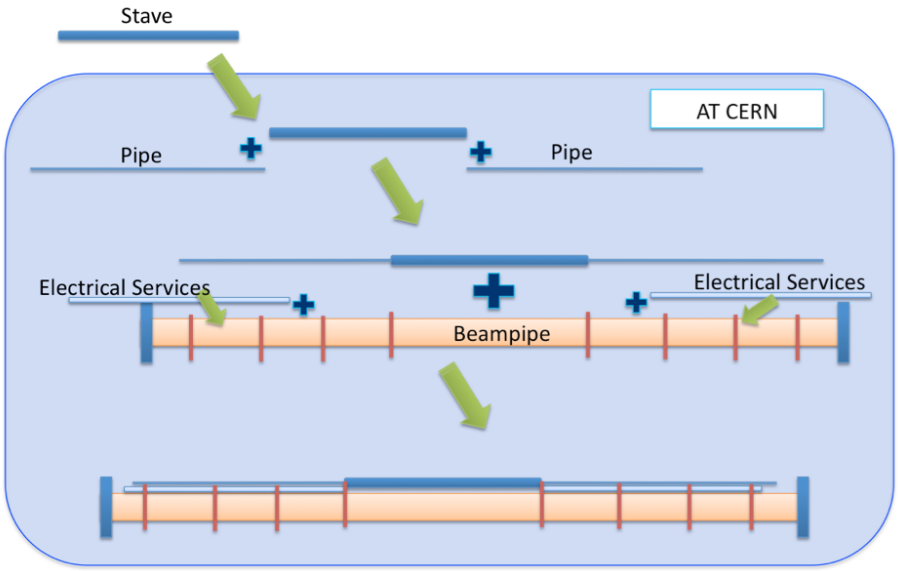


Figure 85. Stave and beam pipe integration procedure in simplified workflow. The support collars along the beam pipe are also sketched.

- The final test of the IBL is carried out with the detector cooled to the test operation temperature of <-30°C with the CO_2 cooling system (see Section 5.7).
- After completion of the final tests, test services and TPPs are disconnected, a final survey repeated and the IBL package is transferred to the installation tool.

5.2 Beam Pipe Design

The overall IBL beam pipe layout follows heavily the current VI beam pipe, with changes to the diameters of pipe and flanges and potential changes to the aluminium faraday shielding. Currently, the total lengths, $z$positions of welds, flanges, and heater contacts, as defined by the CERN beam pipe group, are expected to closely resemble the current beam pipe.

The VI beam pipe features a Be vacuum vessel fabricated from approximately 1 m long prepared sections. These sections are machined and welded together to form the 7.3 m long finished pipe. The IBL beam pipe will feature a 25 mm inner radius, 0.8 mm Be wall, interior activated NEG coating, exterior laminated inconel/kapton heater for in-situ beam pipe bake-out, 3 mm of aerogel insulation, and an as yet to be defined aluminium foil faraday cage (Fig. 86). Machined collars in carbon-reinforced polyimide and aluminium, situated in line with the aerogel insulation, will be placed around the beam pipe.

The IBL beam pipe vacuum flanges, which connect to the VA beam pipe sections on either end, will feature a new split flange allowing a reduction in outer diameter from the current 86 mm to 70 mm[2]. This dimension allows for passage through the current *B*-layer. The split flange contains a small inner ring, through which the vacuum seal is made, and an outer, rotatable split

[2]This split flange diameter is valid for the present beam pipe inner diameter of 58.4 mm; further reduction of the inner diameter beam pipe is to be confirmed by the CERN beam pipe group.

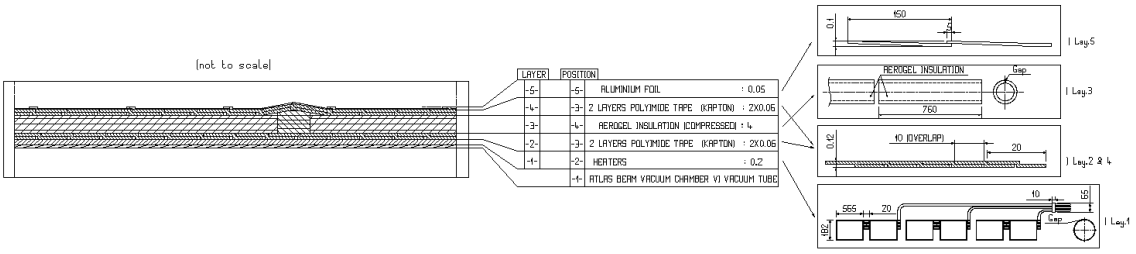


Figure 86. Beam pipe section showing heaters, insulation, mounting collars, and EMI shield.

ring which bolts to the adjoining flange and provides the compression force on the seal to the inner ring. Figure 87 shows the design of the split rotatable, reduced diameter flange concept for IBL beam pipe based on the present beam pipe inner diameter of 58.4 mm. Table 25 summarizes the main parameters of the current and the envisaged IBL beam pipe.

5.3 Global Stave Support and Services Support

5.3.1 Stave support

The 14 IBL staves are individually supported from two flanges mounted loosely around beam pipe attachment collars, one at each end of the stave, as well as from an independent support ring at the stave midpoint (z_0). The two end flanges provide R and z fixation for each stave. The stave support ring with staves mounted to it is shown in Fig. 88 for one stave end; the figure on top shows the front view along the z-axis, the bottom figure shows a side view (stave flex circuits and screws have been removed from the bottom figure for clarity). At the end of the stave, a machined CFRP insert provides a flat surface and accurate edge that fits into a machined flat on the support ring; the stave is held in place with two accurate shoulder screws (pin/screw hybrid), one of which is accessible through a cutout in the overlapping stave.

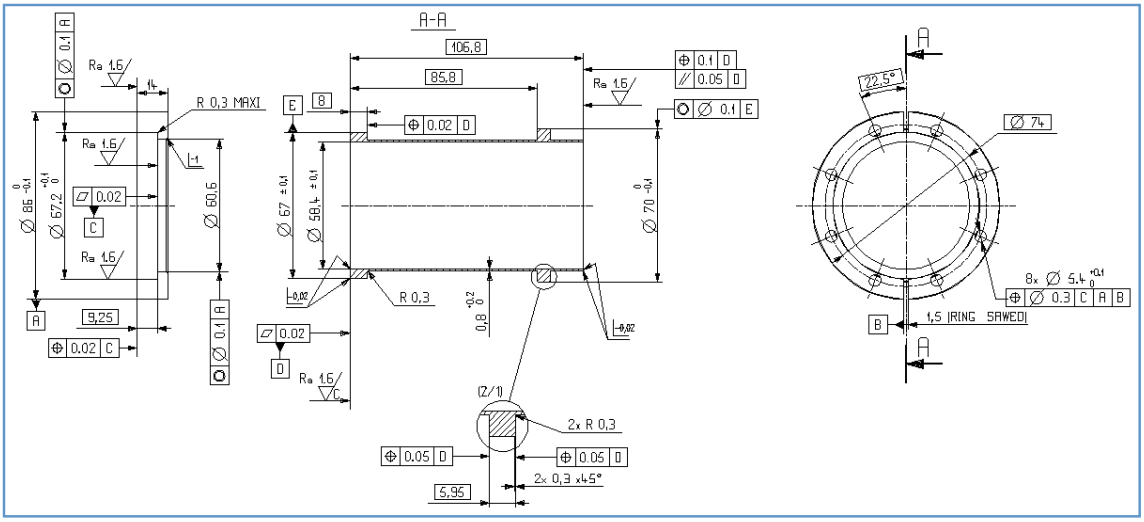


Figure 87. Split rotatable, reduced diameter flange concept for IBL beam pipe.

The stave mid-ring, on the other hand, only locks the phi angle of each stave and its position relative to other staves. The mid-ring neither penetrates to the beam pipe nor attaches to the IST wall. The purpose of this ring is to improve stiffness of the IBL assembly. Without the mid-ring, the staves behave as individual elements, but with the ring, they act as one shell, thus increasing the natural frequency of the assembly by a factor 2.5 (see Fig. 93).

5.3.2 Services support

The entire service chain from EoS card to the PP1 penetration requires support from the beam pipe and IST. During integration and transport, services (both cooling and electrical) are supported by the beam pipe and/or temporary tooling. However, the mechanical parts that support the services from the beam pipe also provide support for the beam pipe from the IST with a loose fit around the beam pipe. In this way, the services support is shared in some ill-defined manner between the beam pipe and IST. The services supports must be located at a short enough interval to provide good strain relief to the services themselves while also providing adequate structural support to the beam pipe along its length. After installation in the IST, the service supports will rest on the IST. Figure 89 shows the service support rings around the beam pipe for one side of the IBL.

Figure 90 (top) shows the front view of a service support ring filled with services for one side of the IBL. The bottom figure shows a detailed view of one slot with all services for one half stave.

In addition to the regular services supports along the bulk of the beam pipe, there will also be specialized supports near the end of the stave, in order to support the EoS card and corresponding electrical connectors, which will need to be mounted in-situ. It is foreseen that these supports will consist of a concentric cylinder around the beam pipe, mounted to the stave end support ring, that provides backing support to the EoS card (or flex) creating a strong foundation for pressing the connectors of the type 1 cable onto the connectors of the EoS card. Figure 91 shows the transition region from stave to type 1 services.

Parameter	**Current Beam Pipe**	**IBL Beam Pipe**
Inner Diameter	58 mm	50 mm
Wall thickness	0.8 mm	0.8 mm
Heater Thickness	0.32 mm	0.32 mm
Heater Type	Inconel/Kapton Flex	Inconel/Kapton Flex
Insulation Thickness	4 mm	3 mm
Insulation Type	Aerogel (Pyrogel AR5223)	Aerogel XX
EMI Shield	50 μm Al	50 μm Al
Vac Flange Type	Fixed	Split Rotatable
Vac Flange Diameter	86 mm	tdc
Flange Diameter (fixed)	NAs	$\gtrsim$ 59 mm *(tbc)*
Fixation Collar Material	Carbon-reinforced polyimide/Al	Glass/Carbon Fiber Composite
Vacuum coating	NEG	NEG
Bakeout Temp. (Max.)	250 °C	250 °C

Table 25. Key parameters for the current and the envisaged IBL beam pipe.

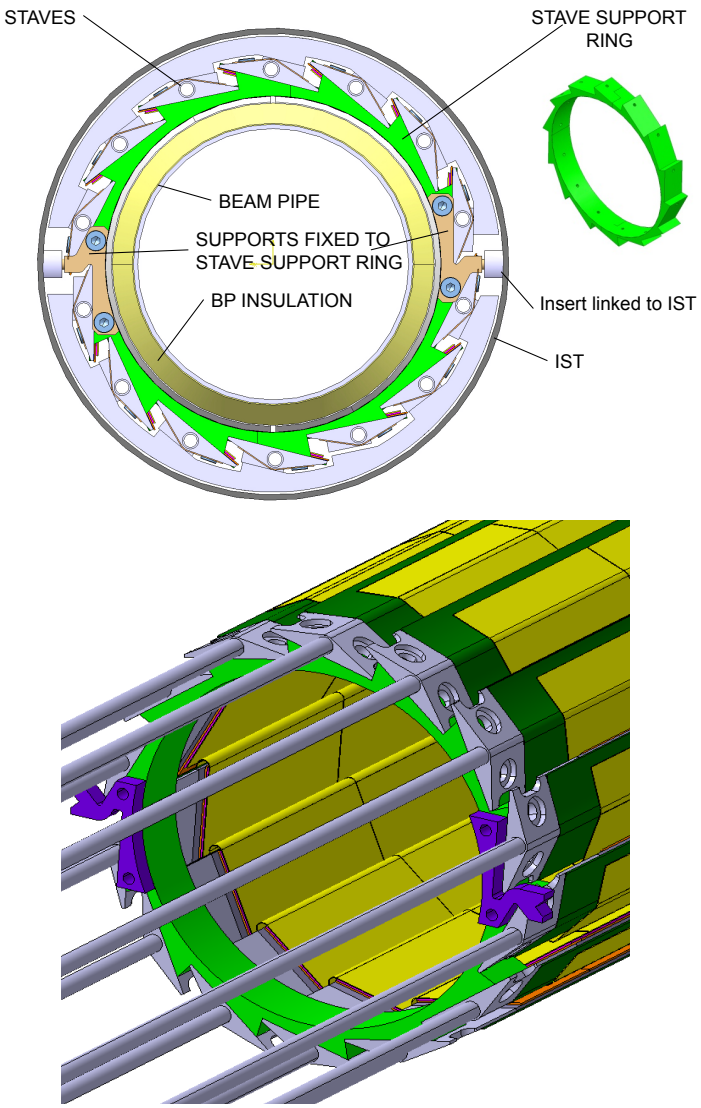


Figure 88. Top: front view of the stave support rings with staves, IST and beam pipe. Bottom: stave support ring with grooves (green) and two fixation shoulder-screw holes per stave end (screws and flex circuit not shown for clarity).

5.4 IBL Package Support and Kinematics

This section describes the positioning of the components of the IBL and beam pipe inside the IST. The mechanical stability of the IBL detector with respect to the existing Pixel detector is of vital importance, hence the IBL is positioned with respect to the IST, which in turn is positioned with respect to the Pixel detector. The IBL detector is decoupled from the beam pipe so that beam pipe movements do not cause alignment changes of IBL to the Pixel detector. This has to be achieved within the existing radial envelop constrains (see Fig. 5):

- Beam pipe outside envelope of 30 mm,
- IBL inside envelope of 31 mm,

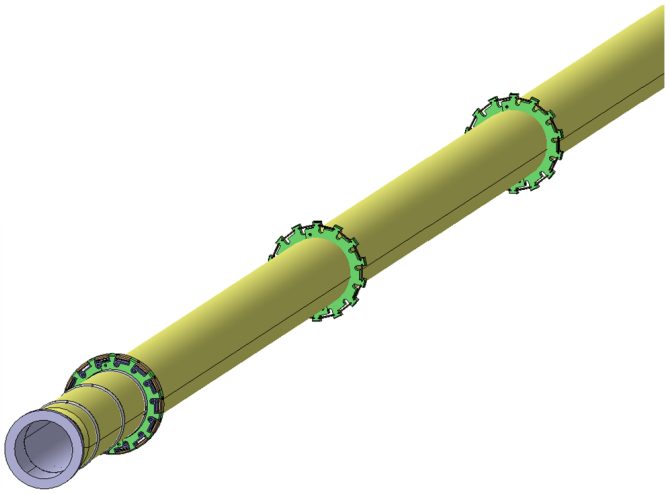


Figure 89. Services support rings shown around the beam pipe.

- IBL outside envelope of 40 mm,
- IST inside envelope of 42.5 mm,
- IST outside envelope of 43.5 mm.

The sequence of positioning is: (1) the IST is positioned with respect to the pixel package, (2) the IBL staves are supported with respect through stave support rings to the IST, and (3) the beam pipe is supported to IST and endplate. Figure 92 shows a schematic overview of the supports between IBL package parts. At the insertion of IBL package to the IST, the beam pipe and the IBL stave rings are supported independently, at the correct z-position, the stave rings lock into isostatic support points mounted in the IST inside surface. This support strategy is identical to the Pixel detector positioning inside the PST. Further studies of this support scheme are currently being done to adapt it to the geometry of the IBL and to compare it against other possible support schemes.

The beam pipe x and y positions are given by IST through gravity, in z the position is given by the end plate support, and rotation around x and y is constraint by the IST tube and around z is fixed at the end plate support. The IST position in x and y is given by the cruciform support and the wire system, the z position is given by the cruciform on side A (insertion side), the rotation around the x and y axis is fixed by the cruciform support and the wire system, the rotation around z axis is given by the cruciform support on side A.

The stave support ring position, and consequently the IBL stave position, in x and y is given by the IST, the z position is given by the IST (to one support ring only). The rotation around the x, y and z axis is fixed by the IST. The stave ends are supported by planar groves at the stave support ring. This over-constraints the staves, however their flexibility allows for that. The planar support groves fixes the stave radial and phi location with respect to the beam axis. The screw pin locks the z position on the stave support ring. The mid-ring constraints the staves in R and ϕ.

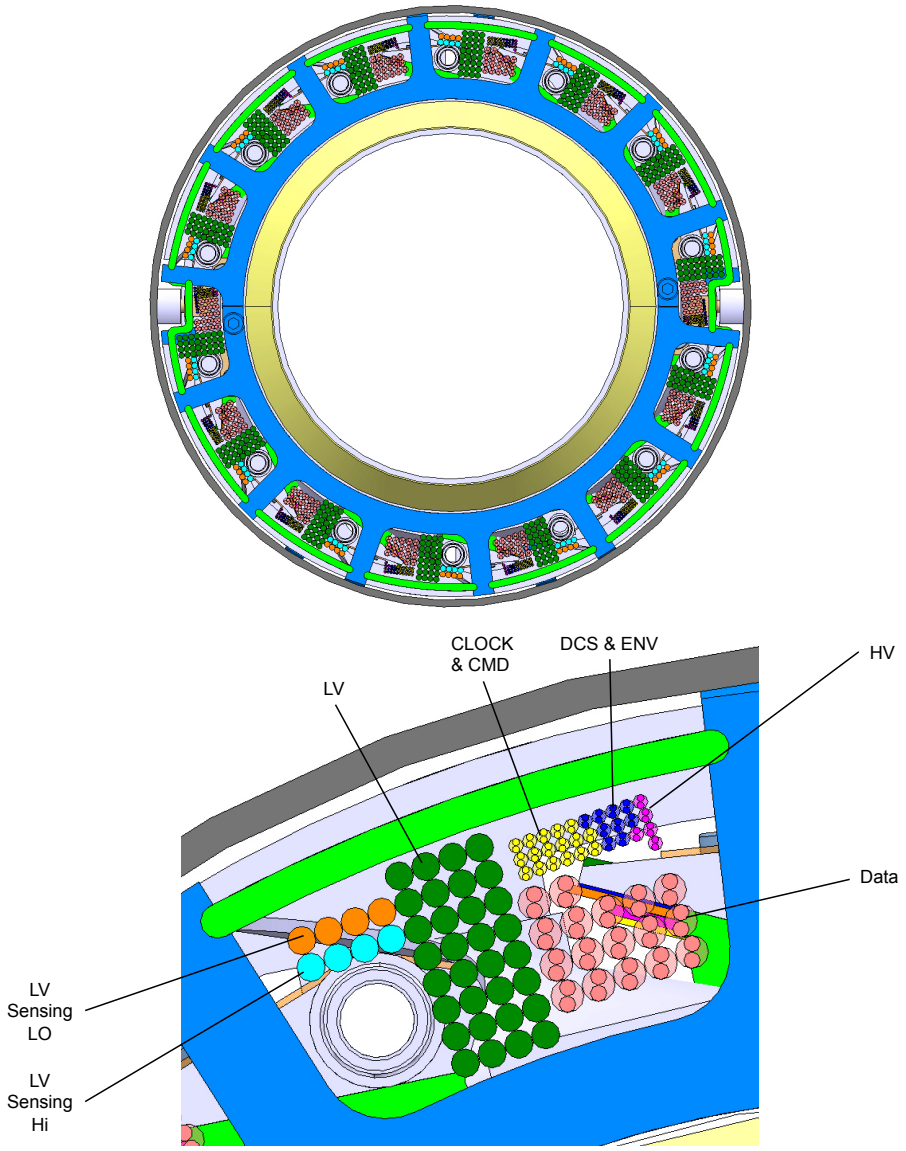


Figure 90. Top: front view of the services support ring with services around the beam pipe. Bottom: detailed view of one slot with services.

5.5 Finite-Element Analysis of IBL Mechanical Support Structure

The IBL integrated assembly features several elements that warrant investigation through Finite Element Analysis (FEA): the use of a mid-stave support ring that is independent of any other structural attachment, the support of the IBL/services/beam pipe assembly from an IST, the support of this IST from the current beam pipe wire system (which behaves as a preloaded spring element), and the presence of contact interfaces throughout the integrated package. The IBL system has been, and is being, analyzed in steps. First, the mid-ring support concept was investigated with a simple stave and ring model. This model, shown in Fig. 93 with a bi-tube stave design, illustrates that the mid-support ring functions well even without external fixation. In essence, the staves that are positioned "vertically" with respect to gravity form structural elements that are many times stiffer

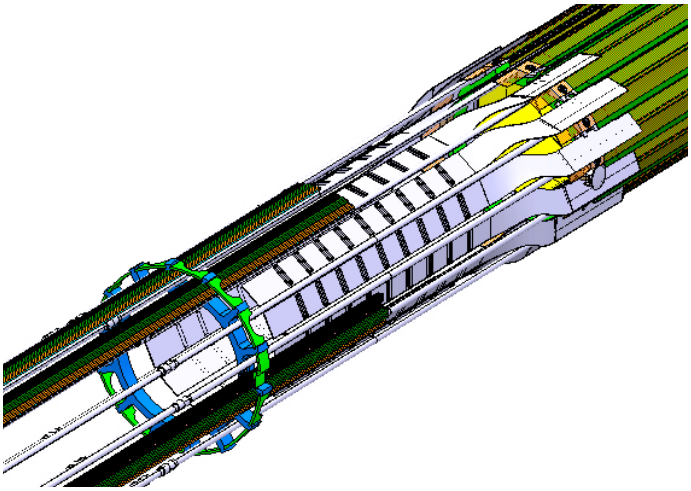


Figure 91. EoS transition region between staves and type 1 services. The EoS cards are shown in white.

than those in "horizontal" orientations. The stiffness of these vertical staves, through a support ring, increases the effective stiffness of the horizontal staves independently of any external anchor. The FEA analysis shows that the IBL overall stiffness is increased by a factor 2.5 with the addition of this independent mid-support ring.

The IBL package was also analyzed with an IST and full beam pipe model in order to deter-

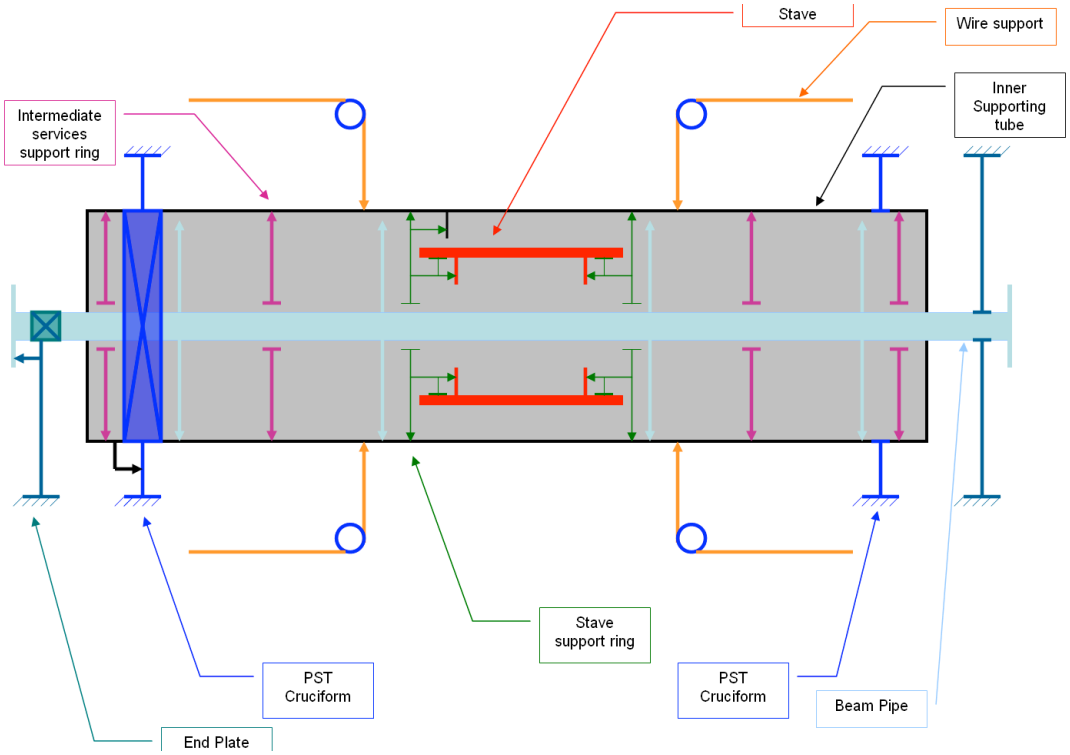


Figure 92. IBL package kinematics and positioning.

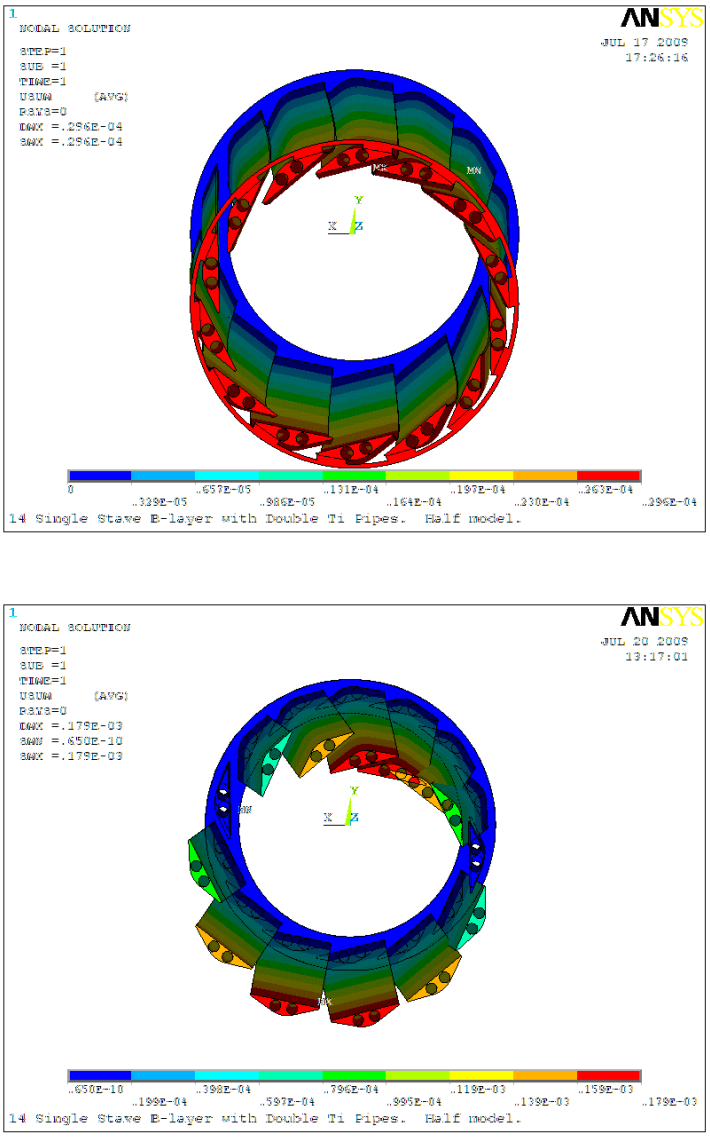


Figure 93. IBL with mid-ring support (top) and without mid-ring support (bottom), showing improvement in overall deflection.

mine the overall effect of wire support and distributed mass. The first iteration of the model, shown in Fig. 94, simplifies the wire supports (they are modelled as beam elements) and neglects contact elements. As such, it may be regarded as an initial step in the analysis process, but requires further development. The IST was analyzed assuming an aggressive laminate of 80% axial (0-degree) plies and 20% low angle (15-degree) plies in a 0.5 mm thick shell. Material was assumed to be carbon fiber with an equivalent fiber modulus of 840 GPa, which classifies as Ultra High Modulus (UHM). Total mass of the IBL package in this model (with added mass for services) is 15.4 kg.

The model shows deflections of less than 250 microns under gravity, mostly appearing in the large unsupported section of IST between the wire supports and PP1 (Fig. 94). Although a modal

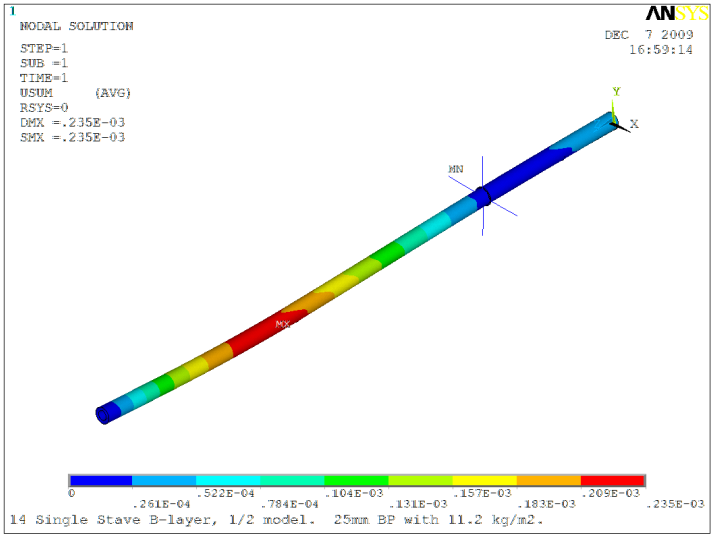


Figure 94. Overall system deflection from simplified model of the IBL, beam pipe, and IST. Total modeled IBL mass is 15.4 kg.

analysis has not yet been performed, this deflection under gravity would imply (with analogy to a simple harmonic oscillator) a fundamental frequency for the system of approximately 33 Hz. However, taking deflections calculated for just the IBL itself, would imply a fundamental frequency of almost 100 Hz for the detector elements. It remains to be seen how the overall system stiffness and local detector stiffness impact each other.

5.6 Integration and Qualification Mock-up

The integration mock-up in SR1 will be constructed during the prototyping phase for IBL supports and staves and equipped with dummy staves as well as full operational prototype staves when available. The goal of the integration mock-up is to

- qualify the stave support, commission and optimize mounting tools,
- survey the stave geometry after mounting with the SR1 CMM,
- support dummy staves during thermal tests, and
- support “stave-0” prototype staves during electrical and system tests.

The integration mock-up permits to carry out a trial assembly of the IBL staves, based on prototype components. The mechanical trial assembly will proceed in several steps: bare staves (no modules or services) will be mounted on support rings first, later this is repeated around a dummy beam pipe on the ITT using the Stave Mounting Tool. In the last step the stave mounting is exercised with prototype staves loaded with mechanical grade modules and full stave flex circuits with EoS cards. Once the process and tools are qualified, fully functional prototype staves with functional modules (“stave-0”) are mounted on the mock-up for electrical tests.

The integration mock-up consists of two stave support rings mounted to a dummy beam pipe for alignment and referencing under realistic conditions. Up to three stave locations are fitted with fully functional powering and readout services on both sides for electrical stave tests. The remaining locations are fitted with cooling and powering services to operate thermo-mechanical dummy staves. The mock-up will be enclosed to maintain a dry environment during tests.

Mechanical studies on the integration mock-up will allow to test the positioning of the staves during the stave mounting followed by a survey to measure the stave deformation in comparison with simulations. In addition, it allows to test access for stave mounting tools. The routing of services from stave to PP1 will be tested on the mock-up to check for interferences and envelop violation.

The thermo-mechanical dummy staves on the integration mock-up are operated with the evaporative cooling system working at final operation temperatures. The tests allow to compare simulation results of stave thermal management with measurements in realistic conditions. The measurements include temperature uniformity tests on the staves, and possibly, stave temperatures during beam pipe bake-out conditions.

It is planned to equip with up to three stave locations in the mock-up with functional electrical services to PP1. On those stave locations the “stave-0" prototype staves are mounted for electrical tests. During the electrical tests the analog performance of the modules is tested under final operation temperatures using the IBL test system in SR1. Those staves in the mock-up are integral part of the system test of the IBL off-detector system to qualifying powering, opto-transmission and IBL DAQ components.

5.7 Electrical Tests during Integration

The goal of the electrical tests is the verification of integrity of modules and services during the integration and, in a final step, the operation of the IBL package in its final configuration before installation.

5.7.1 Connectivity tests of internal services

After staves are mounted and cooling pipes are routed in their final location on service support and PP1 feedthroughs, their leak rate at operation pressure is remeasured.

After electrical services are routed on service support and clamped to feed throughs, their electrical integrity is verified. A “loop-back” card is connected at their EoS end and a test patch panel (TPP) on the PP1 end. The loop back card is equipped with resistors to mimic the power consumption of modules and NTC to test the power supply section of services. A TTC signal is send through TTC lines and looped back unto data lines to verify the functioning of TTC and data line. After the test is completed, the loop-back card is disconnected, the TPP remains at the PP1 connection for later tests.

5.7.2 Tests of stave during stave mounting

After each stave is mounted and the internal services are connected to the EoS card, each module on the stave is checked. The tests are carried out without evaporative cooling in the stave, hence are limited by power dissipation during tests which cause a module warm-up.

The tests include a digital test, writing and readout of register values, to verifiy the TTC and data communication with the module. A threshold scan can be performed on chip-groups within the limits of module warm-up. The threshold scan tests are performed with and without HV applied to module to test the integrity of the sensor bias connection.

5.7.3 Final tests of assembled IBL package

The aim of the final tests is to operate the completed IBL detector under realistic operational conditions, i.e. cooled by the evaporative cooling system for an extended period of time, to test its thermal and electrical stabilities.

For the purpose of the test, all staves are connected to the evaporative cooling system. The system is enclosed and flushed with dry air to maintain a moisture free environment around the detector. An interlock system connects cooling, detector and off detector system together to guarantee detector safety during this test. The dew-point of the air inside the enclosure will be continuously monitored for safe operation and the cooling temperature is chosen above the dew-point. This test requires significant engineering on the temporary feedthroughs of services through the test enclosure to ensure a hermetically closed environment around the IBL.

Two or more staves are connected at the TPP via test power supply and readout services to the off-detector system, which is installed in SR1 already as part of the IBL system test. This system test set-up includes a subset of final IBL components for powering, interlock, DCS, opto-data transmission and DAQ.

The first part of the tests consists of the adjustment of optical communication between modules and the BOC/ROD system through opto-panels (RX and TX tuning). Once communication is established the digital tests, with writing and reading back of registers, are performed. The analog tests, consisting of pulsing the FE-I4 internal calibration circuitry at fixed threshold and input charge, check that the chip front-end part is operational. A threshold scan measures the gain curve and noise of the chip through charge injection at variable amplitude. The test is done with and without bias voltage applied to the sensors to check the integrity of the sensor bias voltage connection.

6. Control, Readout and Off-detector Systems

The IBL will become part of the current ATLAS Pixel detector; however it needs its own, new services, readout and control systems. These systems must be integrated into the existing architecture and framework of the Pixel system. The first half of this chapter addresses the supply and control of the IBL; the IBL readout and steering are discussed in the second half. This reflects the two major areas of the Detector Control System (DCS) and the Data Acquisition (DAQ).

6.1 Power Supplies

Several power supplies are required for the operation of the front-end electronics and the opto-boards, and for the sensor depletion. Common to the design of all power supplies are: floating outputs, programmable output voltages, a hardware current limitation, individual interlock inputs, and communication via an OPC server [79] to allow for an easy integration into the DCS software [80]. Furthermore, the design of the power supply system is driven by the high granularity requirements; each detector module must be controlled and monitored individually. The front-end electronics of the modules in a half stave require one low voltage power supply, which is located in the USA15 counting room, to deliver the operation voltage for the chips (V_{vdd}: 15 V, 15 A). To protect the sensitive front-end electronics, regulation close to the load is necessary. As for the Pixel detector, this can be done by a regulator station located at patch panel 2 (PP2), 10 to 15 m from the loads. Its key component is the ST regulator LHC4913, which is developed in radiation-hard technology.

The alternative powering schemes being considered are a direct supply using linear shunt regulators, or DC-DC converters inside the front-end chips. Each solution implies different requirements for the power supplies, as discussed in Section 3.3. The need for a regulator close to the detector, located at PP2, is common to both of them. As discussed in Chapter 3 (Table 12), the maximum voltage, current, and the allowed voltage drop along the cables, indicate that DC-DC converters solution would be the scheme with the most relaxed requirements. However, until a decision on the powering scheme is made, the design of the regulator boards will be based on the most demanding scenario.

The high voltage (HV) or sensor depletion voltage (V_{det}) strongly depends on the choice of the sensor technology (see Section 3.2). The services will be able to stand up to 1000 V in order to cope with any of the options. As the power consumption also varies significantly with the sensor technology ($0.2 - 1.2$ mA per detector tile), it is still under investigation whether the primary HV is supplied per detector module or per half stave.

Based on the experience with the Pixel detector, the opto-boards have a compound supply cable, which combines the supply voltages for the receiver diode (V_{PiN}: 20 V, 20 mA), and for the transceiver chips and transmitter diode (V_{vdc}: 10 V, 1 A), a reset signal (RST), and a control voltage (V_{iset}: 5 V, 20 mA), which determines the operating point of the transmitter diodes. While the voltages with low power consumption can be supplied directly, V_{vdc} must be regulated at PP2.

6.2 External Services

The services for the IBL package need to be routed from the counting room in USA15 via several break points (patch panels, PP) to the detector. The routing itself is described in Section 7.4.1.

This section describes the external services between the counting room and PP1 and gives the requirements for these. The internal services have been already discussed in Section 4.5.

6.2.1 Design rules and standards

The following ground rules have been adopted for the design and the material selection of the Pixel detector services. The design of the IBL services is done in a comparable way. The main requirements are:

- Compliance with CERN safety regulations (TIS IS23 [81] and IS41 [82]).
- Thermal neutrality of Pixel detector and service bundles (minimize the heat dissipated to or absorbed from neighbouring structures).
- Use of standard connectors, where possible, for both cables and cooling tubes.
- Change technology of cooling tube and cable type only at the patch panels.

6.2.2 Services layout

The routing between the USA15 counting room and the IBL package is sketched in Fig. 95. Cables need to be installed for DCS, to supply the low voltage to the front-end chips and the opto-boards,

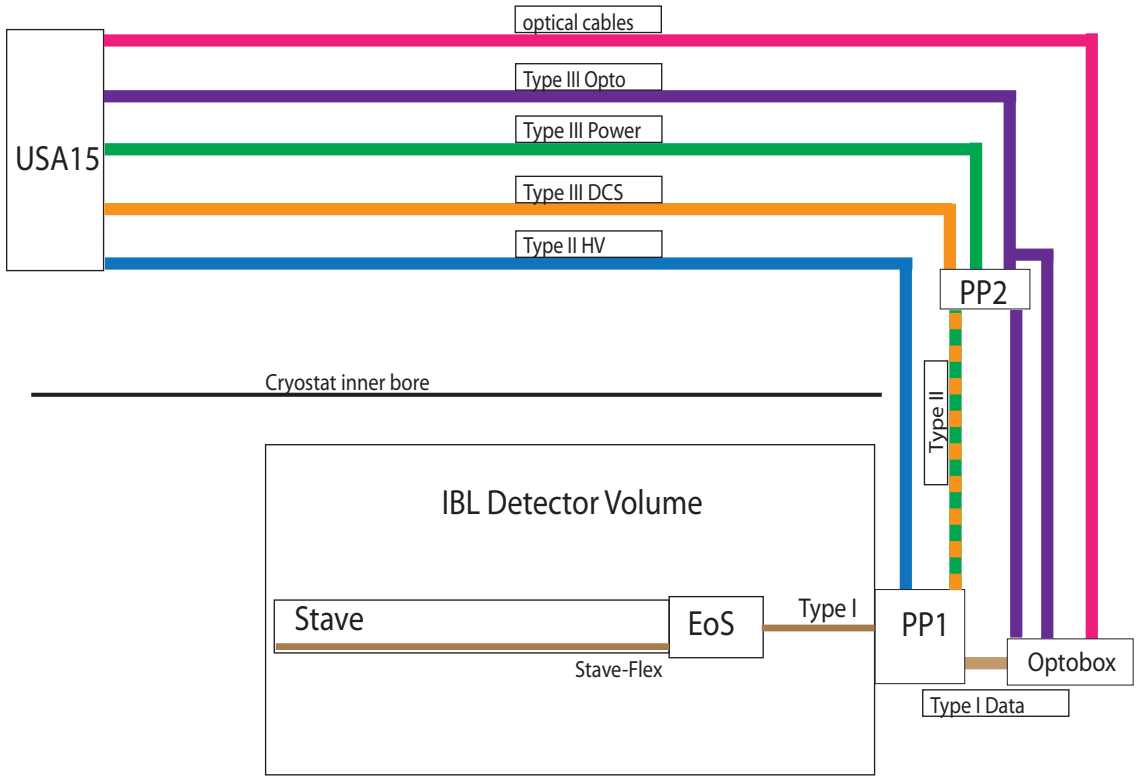


Figure 95. Schematic overview of the location and usage of services types.

and to supply high voltage to the sensors. Optical fibers are used for the data communication. The fibers and high voltage cables run without interruption between the IBL package at PP1 and the USA15 counting room. The low voltage services are split into type II and type III cables, with the regulator station at PP2 in between. The DCS cables will also be fed through PP2 therefore split up into type II and type III cables. (If there is a PP3, the cable between PP3 and USA15 is called type IV.)

6.2.3 Allowable voltage drops

The voltage drop (V_{drop}) for a device (cable, regulator, etc.) is defined by the voltage difference between the input and the output of the device. The design of the cable chain for the IBL is driven by the acceptable voltage drops, which are defined by the safe operation of the devices. The voltage drops are relevant for power cables, and to some extent the voltage regulators. They are estimated for the worst case routing. The limit for the cable voltage drop is determined by the maximum acceptable voltage for safe operation of the ASICs mounted on the module and on the opto-boards. For the different parts of the FE-I4 chip, the breakdown voltage is 2.1 V for the main chip, 2.5 V for the voltage regulator, and 4.73 V for the DC-DC converter. Transient voltages above this limit will destroy the devices in question. The voltage at the chip must never exceed the maximum value, which in the end depends on the chosen powering scheme. The maximum operating voltage for the front-end chip for continuous performance also depends on the powering scheme: 1.5 V is the maximum at the main chip, 1.7 V is the maximum for the regulator, and 3.4 V for the DC-DC converter, as listed in Table 12. The supply voltage for the opto-board (V_{vdc}) is 2.5 V for the chip operation, as mentioned in Section 6.1.

A conservative design requires that the cable voltage drop plus the desired power supply voltage at the ASICs can never exceed the maximum allowable voltage on the ASICs. This would guarantee that should the current drawn by a group of ASICs be reduced from full load to zero in a small time interval (smaller than the response time of the power supplies), no fatal voltage level could appear at the ASICs.

The supply voltages drawing a high current, resulting in a large voltage drop over a longer distance are regulated at the regulator station at PP2. The smallest drop of the voltage from the power supplies to the voltage regulators which can be realized is driven by several factors:

- The maximum input voltage that the voltage regulators can withstand; for the ST regulator LHC4913 (IBL current baseline) this is 14 V,
- the cost of power supplies (increasing with supply voltage),
- the cost of type III cables (increasing with smaller voltage drops), and
- heat dissipation in type III cables (increasing with larger voltage drops).

The total V_{drop} budget for the type III cables from USA15 to PP2 is along the full length, implying uniform power dissipation and cooling requirements per unit of length. Voltage regulators require sense wires to compensate the voltage drops in the power cables. To achieve precise voltage regulation function there are very tight requirements on the maximum allowable voltage drops of the sense lines.

Name	Region	Max. length [m]	VDD V_{drop} [V]	VVDC V_{drop} [V]
Type II	PP1 - PP2	13	1.10	1.30
Voltage Regulator Dropout	PP2		1.5	1.5
Type III	PP2 - USA15	80	2.5	2.5

Table 26. Voltage drops between PP1 and USA15.

For the ST regulator LHC4913 design, the requirements are the following:

- Sense line: very low current. There is no limit to the cable size in terms of V_{drop}, which is very small even with very thin wires.
- Sense return line: nominal current is 40 mA, maximum V_{drop} is 80 mV.

Table 26 gives the baseline nominal voltage drops (round-trip) for the different sections of the power lines. The contribution from the connectors is small and hence neglected.

6.2.4 Cable sizes

High power cables will be sized according to the voltage drop budget, but this does not constrain the size of the low current cables. Experience from the Pixel detector indicates that a minimum cross section corresponding or close to AWG30[3] should be selected. The conductor materials are nickel-plated copper for type II cables and tin-plated copper for cable type III (or IV). The foreseen breakdown of the services is given in Table 27. The purposes of the cables, and the numbers of wires and cables are given. The cross sections of the wires are inherited from the current Pixel detector as given in [83] and [84]. The listing is done for the worst case scenario in terms of wires needed, which is the parallel powering scheme. As soon as either serial powering or DC-DC converters can be used, the required number of wires and/or the cross section of the wires will relax. The table also gives the position of the cable start and end locations.

Type II and III cables have been sized with reference to conductor parameters from Raydex (UK) company wires, which are summarized in Table 28; intermediate cross sections also exist.

[3] AWG: American Wire Gage, defines the wire cross section. The diameter is given by: $d = 0.127\ \text{mm} \cdot 92^{\frac{36-\text{AWG}}{39}}$

Type	Signals	Location	Modularity Unit	Wires per Unit	Multiplicity per Cable	Number of Cables A-Side	Number of Cables C-Side	Purpose
II	LV, LV ret, Sense, Sense ret	PP1 to PP2	1 chain for 4 chips	2x AWG17, 1x AWG22, 1x AWG28	4	14	14	LV
III	LV, LV ret	PP2 to PP4	1 chain for 4 chips	2x AWG14	4	14	14	
	4 chains per half stave 1 cable per half stave							
II	HV, HV ret	PP1 to PP4/Iseg	1 chain for 2 chips	2x AWG28	8	14	14	HV
	8 chains per half stave 1 cable per half stave							
II	Vvdc, Vvdc ret, Sense, Sense ret	Optobox to PP2	1 chain per opto-board	2x AWG22, 1x AWG22, 1x AWG28	4	4	4	Optoboard
III	Vvdc, Vvdc ret	PP2 to SC-Olink	1 chain per opto-board	2x AWG18	1	14	14	
II	Vpin, Vpin ret, Viset, Viset ret, OptoRst, OptoRst ret, Topto, Topto ret	Optobox to SC-Olink	1 chain per opto-board	2x AWG26, 2x AWG26, 2x AWG26, 2x AWG26	1	14	14	
V	Topto, Topto ret	SC-Olink to BBIM		2x AWG26	4	7		
	1 chain Vvdc + 1 chain remaining optoservices 1 cable per opto-board							
II	Tmod, Tmod ret	PP1 to USA15	1 chain for 4 chips	2x AWG26	4	14	14	Tmod
	4 chains per half stave 1 cable per half stave							
II	Tpp2, Tpp2 ret	PP2 to USA15 1	chain per NTC	2x AWG26	4	2 to 4	2 to 4	TPP2
	8 chains per PP2 crate 2 cables per PP2 crate							
II	Env, Env ret	PP1 to PP3	1 chain per sensor	2x AWG26	4	14	14	Env

Table 27. IBL services Layout from PP1 to USA15. The most conservative assumption, without serial power or DC-DC converter power scheme, is shown. (Explanation: LV = low voltage; HV = high voltage; PP<nr> = patch panel counted from the detector position; Vvdc, Vpin, OptoRst = supply lines for the opto-board; Tmod, Tpp2, Topto = temperature monitoring lines for the module, PP2, and the opto-boards; ENV = environmental sensors, ret: indicates the return line.)

TYPE II CABLES				
Conductor AWG	Conductor strand [mm]	Conductor diameter [mm]	Conductor area [mm^2]	Max. resistance (Ω/km @ 20°C)
30	19/0.064	0.32	0.061	340.00
28	19/0.080	0.40	0.096	232.00
26	19/0.100	0.500	0.149	139.00
24	19/0.120	0.600	0.215	94.90
22	19/0.150	0.750	0.366	61.30
20	19/0.200	1.000	0.597	33.60
TYPE III CABLES				
Conductor AWG	Conductor strand [mm]	Conductor diameter [mm]	Conductor area [mm^2]	Max. resistance (Ω/km @ 20°C)
24	19/0.130	0.650	0.25	76.40
20	16/0.200	0.900	0.5	39.00
18	32/0.200	1.320	1	19.50
16	30/0.250	1.600	1.5	13.30
14	50/0.250	2.000	2.5	7.98
12	56/0.300	2.600	4	4.95

Table 28. Cable sizes for type II and type III cables.

6.3 DCS

The Detector Control System (DCS) monitors, controls and supervises the detector and related services aiming at stable operation of the detector system. In addition to guaranteeing reliable data taking, it also has to ensure the safety of hardware and personnel working with the system. At a lower level, the IBL DCS will handle parameters related to the detector modules, the opto-boards, the environment and the DAQ hardware. Fig. 96 gives an overview of the systems that relate to DCS.

To allow a common, coherent operation of the IBL and the Pixel detector, the DCS system of the IBL should be organized and built in the same way as the control system of the Pixel detector. This concerns the construction of the hardware as well as the design of the software. Besides the power supplies, which are already described in Section 6.1, various monitoring units and an interlock system are required. The construction of the custom made DCS hardware is based on the Embedded Local Monitoring Board (ELMB), the ATLAS wide front-end monitoring and control unit. Using the ELMB, the integration into the Pixel detector DCS software is ensured. Depending on the modularity of the primary power supplies, which most likely will supply a half stave, additional current monitoring units for the LV and HV are necessary to provide more detailed information per detector module.

The detector's environmental temperature and humidity are monitored. Numerous temperature sensors (NTCs) are spread over the whole detector volume to provide a detailed temperature profile. Sudden increases as well as slowly changing values are recorded and can be used to trigger

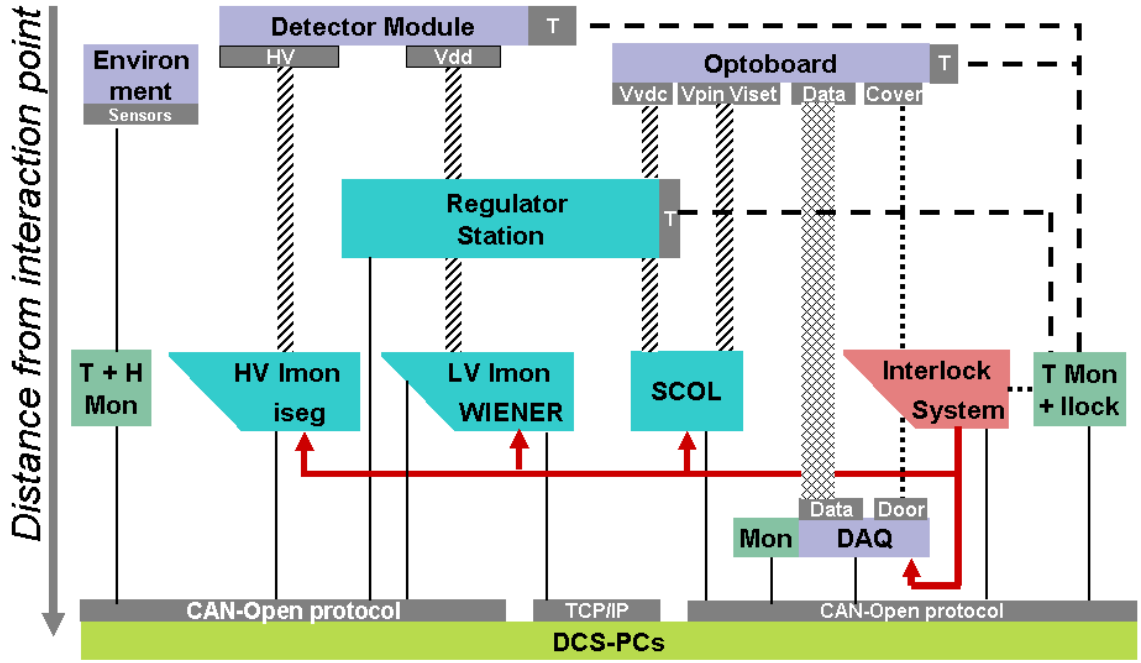


Figure 96. Overview of the detector control system of the IBL.

corrective actions. Furthermore, the detector modules, opto-boards, and the regulator station at PP2 are equipped with temperature sensors which are monitored by the DCS, and which in parallel provide inputs to a hardware interlock system. To protect against from damage from overheating, an interock signal is generated when a defined temperature limit is exceeded. The interlock system also protects people against the risks related to the infrared lasers of the optical links. The system collects signals from all interlock-protected devices and switches off the relevant power supplies. Additional signals from external systems such as the ATLAS Detector Safety System (DSS) and the Safe-For-Beam handshake are fed into the interlock matrix. In the other direction, the Pixel detector interlock matrix generates a signal as an input to the LHC bake-out system in case of overheating of the detector modules.

Unlike the current Pixel detector, all crates for the IBL should be located in the counting rooms, preferably in USA15. Concentrating all equipment in one counting room helps to avoid half filled crates and facilitates access and maintenance. Three racks should provide sufficient space for power supplies and DCS crates.

The DCS software provides a status display and an interface for issuing commands. Automatic corrective procedures protect the detector. Alarms are raised in case the detector is at risk. The integration into the ATLAS wide control system and the collaboration with the DAQ system are vital. The DCS data is archived for further debugging of the DCS itself and for offline analysis. Following the ATLAS wide standard, and as used for the Pixel detector, the control software will be developed using PVSS (Prozess–Visualisierungs- und Steuerungs-System) and the FSM (Finite State Machine).

The IBL DCS software consists of three layers. The bottom layer, the Front-end Integration Tool (FIT), establishes the communication with the different hardware units. It reads the values from the hardware into data structures, which follow the properties of the hardware devices. The next layer, the System Integration Tool (SIT), provides the mapping between the hardware and the detector, which is fundamental for the FSM. For all channels used in the mapping, the SIT initializes the archiving to the conditions database. To ensure a coherent operation of DCS and DAQ, the actual mapping between hardware channels and detector is stored in the connectivity database, which is read by the DAQ and the SIT. Both FIT and SIT were developed for the Pixel detector DCS and, as long as similar hardware is used, are implemented for the IBL in the same way. The third layer is given by the FSM. This is the tool to operate the detector. It gives the shifter a clear overview of the status of the detector and provides a set of commands which bring the detector safely into the correct operation mode. To ensure a coherent operation of the Pixel detector and IBL, the control system of the IBL is organized in the same way as in the Pixel detector. Detector modules, half staves, cooling circuits, and the DAQ partition are the units on which DCS can act. They define the hierarchical tree structure of the FSM. As the functionality of the Pixel detector and IBL are the same, the existing set of states and commands for the Pixel detector can be used for the IBL.

6.4 Readout Electronics

6.4.1 Readout driver

The Read Out Driver (ROD) is a board designed to interface the sub-detector specific readout components with the standard ATLAS DAQ chain, in particular with the Readout System (ROS) and the Timing, Trigger, and Control (TTC) system. The ROD receives timing and trigger signals from the TTC system and must propagate them to the front-end electronics. It must send the appropriate configuration to the connected front-end chips and receive the event fragments, compact them into a single ROD fragment, and send it to the ROS.

In the present implementation of the ATLAS DAQ, the ROD is a 9U VME board; the VME bus, however, is not used for the data path. Data from the detector is sent to the ROSes via an S-Link, an optical 40 MB/s custom link. VME is used to control and configure the board, and to download front-end chip configurations from the DataBase (DB). The existing Pixel detector (and SCT) ROD however makes an exception to this rule. Although in data-taking mode the S-Link is used for data output, in calibration mode data is transferred via VME bus. The calibration of the Pixel detector is performed by repeating relatively short (100-1000) series of events, recorded while injecting a known charge into each pixel, and with different settings of the front-end parameters (e.g. different thresholds or different pre-amplifier feedback currents). This sequence, called a scan, generates a very large number of events, but in general, only the histogram showing how many times each pixel has been fired for a given setting is important. For this reason, in calibration mode, the data stream coming from the Pixel detector is not sent over the S-Link, but processed in the ROD, where the relevant histograms are produced. At the end of the scan, the histograms are transferred to the DAQ system via VME for further processing and archiving. In the existing ROD design, the transfer rate over the VME bus is limited to 7 MB/s, and this limitation affects the 16 RODs in a ROD crate, as the bus must be allocated to one ROD at the time. For this reason,

as much data reduction as possible is performed directly on the ROD, using the four floating point DSP units.

When specifying the design of the DAQ chain for the IBL, the first open question was whether the existing ROD was sufficient or if a new one was needed. The existing ROD firmware could be modified to operate with the IBL module data format; however, the hardware of the board is designed to operate with a maximum of eight 160 Mb/s input links (from the modules) to one output S-Link, while, to respect the IBL natural modularity, sixteen 160 Mb/s links to two S-Links have to be handled. This consideration, together with the 7 MB/s bandwidth limitation on the VME bus already mentioned, and the obsolescence of the components, led to the decision to design a new ROD. The existing ROD can however be used at the beginning of the integration process to operate a limited number of IBL modules, so proceeding with the adaptation of its firmware is still important.

The second step was to identify the technology to use for the new ROD. Advanced Telecommunications Computing Architecture (ATCA) is an emerging standard, already widely used in high-end network applications, that appears to be a natural candidate for the replacement of the VME bus. Particularly appealing for high energy physics DAQ applications, is the possibility of dynamically allocating point-to-point high speed channels between the boards connected to the bus. The IBL community, however, felt that the change to the ATCA standard was too drastic given the IBL time-scale, and was afraid of the complete lack of backward compatibility intrinsic in this solution, compatibility that is considered important for a detector that will be an extension of the existing one. It was then decided to keep the VME standard as baseline, and keep studying ATCA as a solution for HL-LHC.

Keeping in mind the backward compatibility issues already illustrated, it is clear that the new ROD must be capable of operating with the new and with the old Back of Crate optical interface card (BOC, see Section 6.4.5), and conversely the new BOC must be capable of operating with the old and new ROD. The design of the new ROD therefore follows these guidelines:

- Maximum compatibility in the use of the J3 custom backplane, used to communicate with the BOC and the TTC Interface Module (TIM). In particular, the interface with the TIM must remain the same, while different mapping could be used for the new and old BOC.

- Modularity corresponding to sixteen 160 Mb/s input channels and two 160 MB/s S-Link output channels. One or two modules per board (so 2 or 4 S-Link output). Possibility to reduce to eight 160 Mb/s input links and one output S-Link in compatibility mode.

- 2 or 4 S-Links will be used to connect to the ATLAS TDAQ. The S-Link connection must be driven through the backplane to the BOC and be compatible with the old BOC design, which serves only one S-Link.

- Full data path implemented in one or two large FPGAs, to maximize the design flexibility and simplify the inter-communication between the data path components.

- Increase the output bandwidth for calibration histograms. This can be achieved using the full VME64 bandwidth, or using high speed links (e.g. Gigabit Ethernet) for calibration data. While the VME64 bandwidth (shared by the crate) would still impose significant floating

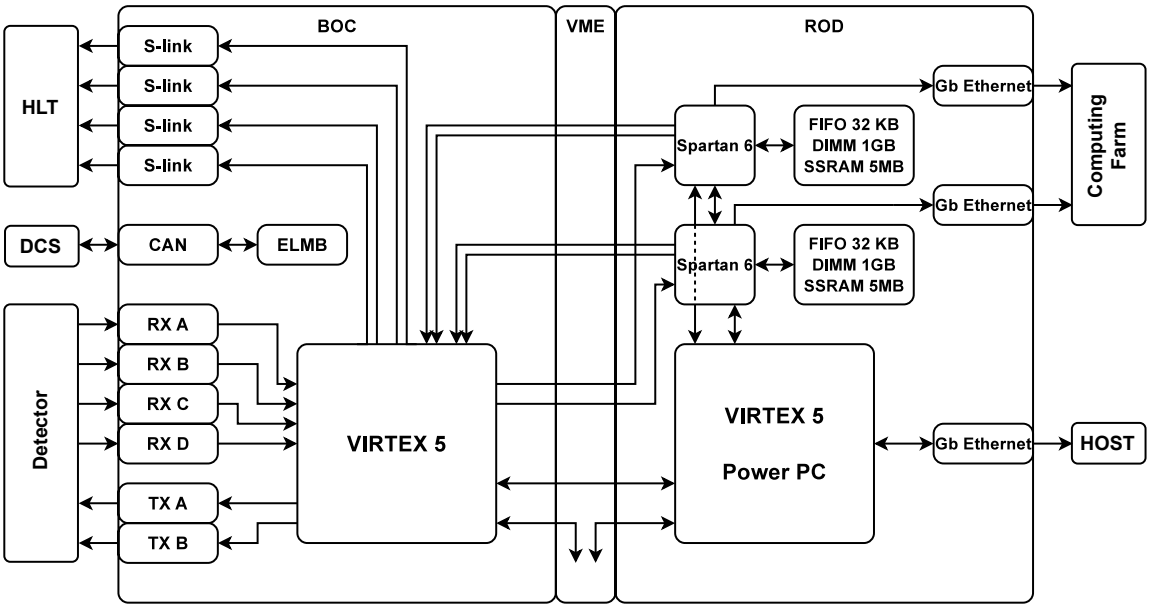


Figure 97. Off-detector readout system overview.

point capabilities on the ROD, a solution with 1 Gb/s link per ROD could make it convenient to extract raw histograms immediately and process them on commercial processors, in this way reducing or eliminating the need for DSPs on the ROD.

To reduce the amount of hardware to be installed in the USA15 counting room, the number of links to be handled from the detector is doubled on the readout cards. This would enable the card pair to handle two half staves and transfer the data to the ROS. A schematic overview of the readout card pair is given in Fig. 97.

6.4.2 TTC interface module

The TTC Interface Module (TIM) is a 9U VME board, located in each Pixel detector readout crate, that receives trigger (LVL1, ECR, BCR) and timing (Clock, Orbit) signals from the ATLAS TTC system and distributes them to the RODs via the J3 custom backplane within the crate. Given the decision to keep the VME as baseline for the IBL readout, the existing TIM should also be an appropriate solution for the IBL. The decision is then to find or fabricate the units needed for the IBL ROD crates.

6.4.3 Single board computer

The Single Board Computer (SBC) is a standard Intel based PC with a VME interface chip (Tundra Universe) mounted on a 6U VME card. It is used to control the ROD crate, load the FE configurations and, for the Pixel detector, extract via VME the calibration histograms and send them, over Ethernet, to the histogram server. No special needs are foreseen for the IBL from the SBC point of view. If the new ROD is equipped with Gigabit Ethernet output for the calibration histograms, part of the functionality of the SBC will be moved to more traditional rack mounted computers.

6.4.4 DAQ software

The DAQ software for the existing Pixel detector is a complex collection of C++ applications and libraries used in a distributed environment. The complexity of the code is not in the data-taking part (which is mostly handled by the ROD firmware and by the ATLAS TDAQ software), but in the calibration part, which required a custom treatment of the histograms and a sophisticated DB system. It is obviously interesting for the IBL community to re-use this code as much as possible, as this implies having, from the beginning of the development, a well established software framework for the analysis and the archiving of calibration data.

The structure of the software is outlined in Fig. 98. It consists of a set of drivers (called Action Servers) running on the ROD crate SBC, interacting with the ROD and the modules, a set of services, interfacing with the DB and archiving system as well as with the rest of the ATLAS TDAQ and with the DCS system, and a set of applications that can perform different tasks (data-taking, calibration, diagnostics) on a set of exclusively allocated RODs. The part of the code which is ROD/front-end specific is in the drivers. The rest of the code should be re-usable as it is. For the drivers, some support is already available to handle different RODs and front-ends with different command sets. Some more support for different scan strategies is already being added. In view of this, the existing code could be used from beginning of the IBL testing. Some care will be necessary to keep the IBL specific code integrated with the development of the rest of the software to avoid dangerous branching in the common part. Some specific development is also foreseen to simplify the use of the complex Pixel detector DAQ software in small laboratory installations.

6.4.5 Off-detector optical interface card, the IBL BOC

As discussed in Section 6.4.1, the interface of the optical link to the read-out electronics is on a separate card, the optical interface board called the Back of Crate card (BOC), which is paired with a ROD. A connection to the machine timing enables the BOC to provide the clocks needed by the on- and off-detector parts. The LHC clock connection is to the TIM in the VME crate. The BOC then derives the clocks for the front-end chips, for the ROD and for the card itself from the TIM. A capability to adjust delays and phases must be implemented to be able to adjust the detector timing to the bunch crossing. Command data for the front-end chips are received from the ROD and passed optically to the chips using the transmitter plugins (TX); data from the front-end chips is received via the optical receiver plugins (RX) and passed as a raw data stream to the ROD.

Further functions could also be implemented. To increase the number of channels to be handled by an off-detector ROD-BOC pair, a decoding of the incoming module data and an appropriate number of interface boards to the readout system (S-Link or RoBin) should be foreseen. The implementation of a real time data path could be realized and needs further investigation. Clearly, a high compatibility with the present Pixel detector must be kept and therefore the pin assignment and its usage must remain. Implementing the functionalities using FPGA chips gives the freedom to realize backward and IBL compatible firmware versions for the same hardware.

6.5 Opto-links

The transmission of the data from the detector and the commands to the detector front-end components is done via optical data transmission. The scheme will be very similar to the Pixel detector

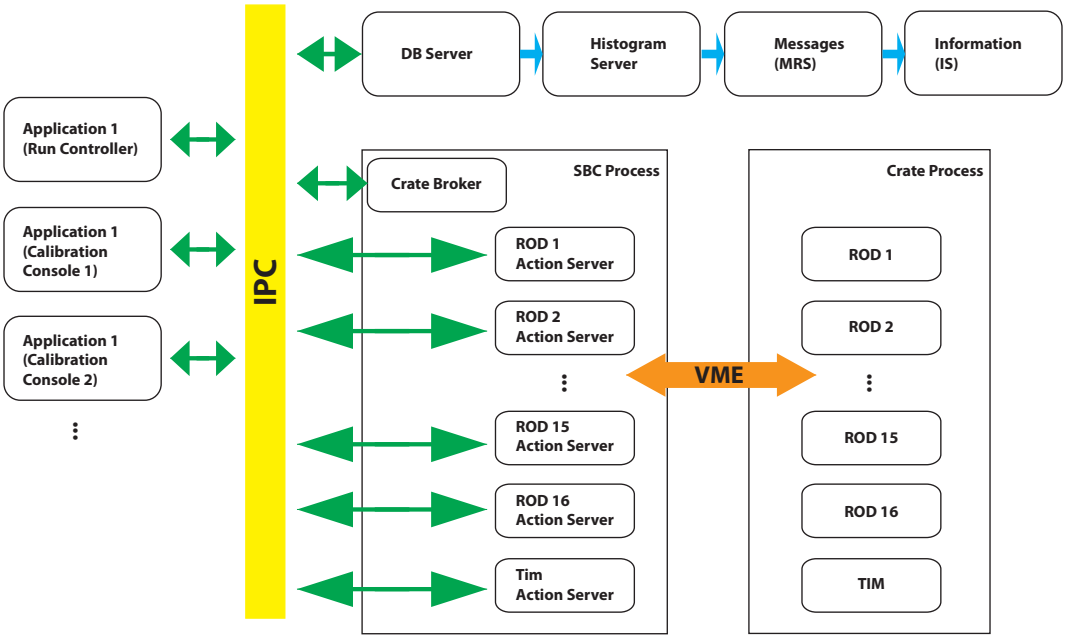


Figure 98. DAQ software structure.

design, consisting of arrays of optical components (PiN diodes and VCSELs). These are housed on the opto-boards on-detector, and on optical plugins off-detector. Optical data transmission has the known advantages of potential free transmission, low mass and no crosstalk between the different links. In the following sections, the different components will be described in more detail; the commissioning and calibration prospects are discussed in Section 8.2.

6.5.1 On-detector optical components

The architecture of the on-detector optical links of the IBL is similar to that of the current Pixel detector. The optical links of the Pixel detector are not mounted directly on the detector. Instead, the links are mounted on a patch panel (PP0) about 1 m from the interaction region. This solution simplified the construction of both the Pixel detector modules and optical modules (opto-boards). The proposed location for the IBL optical links will be further away, at about $z = 6$ m (see Section 4.5). Each opto-board of the current Pixel detector contains one PiN array and one or two VCSEL arrays. The dual VCSEL array opto-board is used for the B-Layer to accommodate the expected higher occupancy. Each B-Layer opto-board contains seven TTC links and fourteen data links because each half stave has either six or seven Pixel detector modules. Given that each half stave of the IBL will have sixteen FEs, the plan is to build an opto-board with eight TTC links and sixteen data links to serve half a stave with each pair of front-end chips sharing a TTC link. The system requires 28 opto-boards, for a total of 224 TTC and 448 data links. The optical package to house

Figure 99. MT ferrule.

Figure 100. An MPO connector.

each VCSEL or PiN array for the current Pixel detector was designed in a quite innovative way but there were several deficiencies:

- The VCSEL/PiN array was mounted on a Printed Circuit Board (PCB) in FR4, a poor heat conductor.
- It was difficult to solder the micro-leads ($\sim$100 μm) on an opto-pack to the traces on an opto-board fabricated with BeO, an excellent heat conductor. It was also difficult to clean off the solder flux due to the presence of other components on the opto-board, as dictated by the assembly sequence. Consequently, the remaining flux could mask a cold solder joint. This is a major source of failure in the optical links of the present Pixel detector.
- The opto-pack coupled to an MT ferrule, Fig. 99, which is the connector on the fiber ribbon. This unconventional usage of an MT ferrule required the use of a custom housing (connector) that was fragile and difficult to mount and dismount.

Over the past few years, a new opto-pack design [85] has been developed, that cures these deficiencies by implementing the following improvements:

- Replaced the FR4 opto-pack with BeO.
- Wire bonded the opto-packs instead of soldering them.
- Replaced the MT ferrule and custom housing by a commercial MPO connector and adaptor (Fig. 100).

These improvements should greatly increase the reliability of the optical links. Fig. 101 shows the design of the base of the opto-pack. The VCSEL or PiN array is wire bonded to the traces. The traces then bend around the corner of the base and connect by wire bonds to a driver or receiver ASIC.

As part of the R&D program to evaluate the radiation hardness of VCSEL and PiN arrays, a large number of opto-packs has been fabricated over the past few years. The precise alignment of the VCSEL array with respect to the guide pins is critical to achieve good optical power coupling. Out of 63 VCSEL opto-packs fabricated, 51 opto-packs have optical power in excess of 1 mW at 7 mA for all channels. Significantly more optical power can be produced at higher driver current (the vendor specification for the maximum current is $\sim$ 11 mA) and hence the optical power is quite adequate for the data transmission. The alignment for a PiN opto-pack is much less stringent

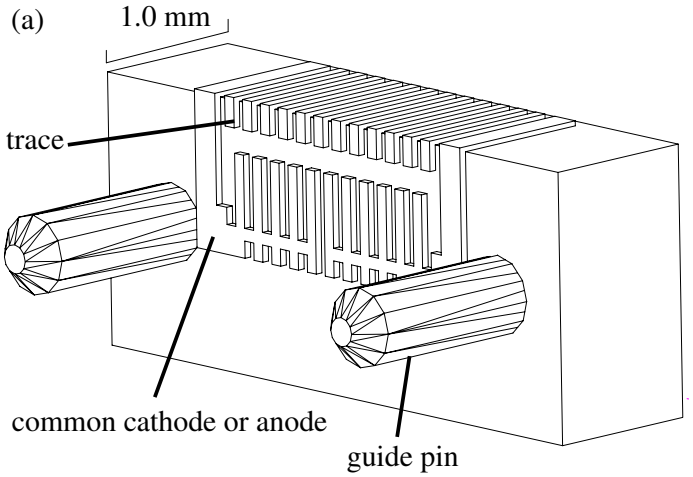


Figure 101. Base of a BeO opto-pack.

due to the large light sensitive area. To date, 46 PiN opto-packs have been fabricated. The principle of the opto-pack design and fabrication has been proven by this.

All material used in an opto-pack must be non magnetic and radiation hard. The guide pins are made of ceramic as in the optical links of the present Pixel detector. The two springs inside an MPO connector must also be non-magnetic. The MPO connector and adaptor have been irradiated to 70 Mrad with no sign of degradation in mechanical integrity. Over the past few years, the radiation-hardness of the VCSEL and PiN arrays has been evaluated as part of the R&D program studying the radiation-hardness of optical components for the LHC upgrades. The proposal is to use 10 Gb/s VCSEL arrays and 3.125 Gb/s PiN arrays.

The baseline plan is to use the VCSEL driver chip (VDC) and PiN receiver chip (DORIC) of the current Pixel detector [86]. The DORIC will decode the bi-phase mark encoded signal, Fig. 102, received at the PiN diode. The plan is to use the same 40 MHz clock to encode the data. The current VDC operates at 80 Mb/s and the plan is to operate at 160 MHz. The feasibility of the proposed operation using a spare opto-board with seven TTC and fourteen data links is under test. This will be followed with a new opto-board with eight TTC and sixteen data links.

The optical links of the current Pixel detector have been in continuous operation for about a year. So far, slightly over 1% of the detector modules that cannot be properly configured or read back might be attributed to optical link failures although some of the failures may be due to a break in the continuity between the optical and Pixel detector modules. Concerning failures seen in the optical links by now, some of them are probably due to cold solders on the micro leads on the opto-packs. These failures will be fixed with the new opto-packs that use wire bonds for the connection. It is not possible to pinpoint the other failures because the detector is inaccessible. Given these unknowns and the uncertainty in the future failure rate, it is prudent that the possibility of adding redundancy in the optical links is investigated. Commercial VCSEL and PiN arrays and fiber ribbons are available in 4 or 12 channels only. The four unused channels in a 12-channel array can be used as spares and the off-detector electronics should be able handle these extra channels. This requires adding a command decoder from the FE to the current DORIC and VDC for the

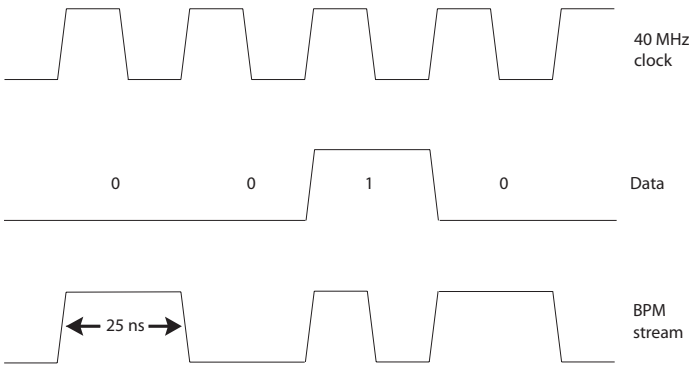


Figure 102. Example of encoding a data and clock stream into one BPM signal.

rerouting. Another feature to be added to the new VDC is to allow the individual setting of the VCSEL currents in an array. This should improve the operation margin over the current optical links where there is a single setting for the VCSEL current, resulting in large spread in the optical power in an array due to the natural variation in the power in an array and to imperfect alignment. The plan is to have a new prototype ASIC available early next year to test the feasibility of the improvement.

6.5.2 Off-detector optical components

The off-detector optical components are located in the IBL optical interface board (the BOC, see Section 6.4.5). Two different optical parts, for sending and receiving signals, are foreseen. Both are to be realised as pluggable boards. The transmitting part is the IBL TX-plugin and the receiving part the IBL RX-plugin, following the naming convention used for the Pixel detector.

The sending part (IBL TX-plugin) consists of a VCSEL array for sending optical signals to the detector and a chip to encode the clock and data signals into one stream. The encoding is a Manchester type scheme – Bi Phase Mark (BPM) scheme – which is already used in the present Pixel detector. The downlink operates at 40 Mb/s and is compatible with the present scheme. It is therefore possible to reproduce the existing Pixel detector TX-plugins. To configure or control the detector modules, signals are sent from the ROD to the BOC, on which clock and data are encoded into one stream per module. This is then converted from an electrical to an optical signal and sent to the module. The encoding scheme is sketched in Fig. 102 showing the clock and the data being encoded into one signal which is sent to the on-detector components. To be able to optimize the transmitted signal and accommodate irradiation and aging effects of the components, several adjustable parameters are foreseen: the light power, the signal duty cycle and the signal phase.

The receiving part (IBL RX-plugin) contains a PiN diode array and an amplifying part and receives the data coming from the detector at a bandwidth of 160 Mb/s. The data stream being sent from the detector is encoded using an 8b/10b scheme. This makes an automated threshold adjustment feasible and enables to use AC coupled receivers. The data are converted into electrical signals and fed through the BOC to the ROD, which builds events and sends the event fragments to the readout system. The PiN diodes are also arranged in an array and followed by a chip which amplifies the signals and drives them to BOC in an appropriate electrical format. The plugins are

to be developed and tested to be able to handle the dynamic range of the incoming signal amplitude correctly. A threshold for sampling the signals is to be set and should be adjustable to accommodate for different levels of the incoming optical power.The

The connection to the Readout System and therefore to the Higher Level Trigger System is realized the same way as in the Pixel Detector. S-Link connections will be implemented on the BOC card. To optimize space usage on the card, the S-Link interface will be embedded unto the BOC card. This way it is possible to serve up to 32 incoming FE-I4 connections. The data to be driven out via the S-Link interface are provided from the ROD to the embedded S-Link on the BOC. To serve also an Fast Trackfinder (FTK) for the trigger each S-Link will have 2 optical interfaces, one to be connected to the Higher Level Trigger System and the other one sends a copy of this data to the FTK farm. So in total up to 8 optical transceivers can be situated on each BOC card. Each S-Link has to deal with the data of 8 incoming data streams (128 Mb/s datarate and runs at 160 MB/s bandwith.

6.5.3 Fibers and connections

The connection between the on-detector optical components, the opto-boards, and the off-detector components, the TX- and RX-plugins, will be done by optical fibers. Since the lasers and PiN diodes are arranged in arrays, the fibers must be ribbonized to connect the two ends properly. The commercial standard for arrays is 12-way, so the natural choice of fiber ribbons would be 12-way as well, although the Pixel detector optical link is realised using 8-way arrays and fibers. The connection is to be made by continuous fibers, avoiding interruptions by connectors. On the off-detector side, at the IBL BOC, the connector choice can easily use commercial standards. A commercial standard fitting is also proposed for the opto-board end, i.e. an MPO connector, but under the constraints of being radiation hard and non magnetic. The fiber itself must be tested and validated to tolerate the radiation load at which it will be exposed over the operation time in the detector area.

6.6 Cooling Plant

The ATLAS SCT and Pixel detector are cooled by an evaporative cooling system using the fluorocarbon R218[4] refrigerant. The plant is based on a standard fridge cycle [87] [88] where the overheated vapour, coming from the boiling channel in the detector, is compressed by a compressor plant, and condensed in a heat exchanger (Fig. 103). The fluid, stored in the liquid tank, is distributed over 204 feeding lines to the detector local structures, where it evaporates due to the pressure drop induced by the capillary at the temperature set by the Back Pressure Regulator (BPR).

The choice of the coolant was based on its dielectricity, thermodynamic characteristics and its radiation hardness; C_3F_8 suffers marginal chemical dissociation under radiation. The nominal evaporation temperature at the end of the boiling channel is -25 °C, which corresponds to an absolute vapour pressure of 1.67 bar_a. The limitation of the evaporation temperature comes from the low saturation pressure of the fluid, which cannot be significantly reduced due to pressure drops along the return lines.

[4]Halocarbon R218: Octafluoropropane (C_3F_8)

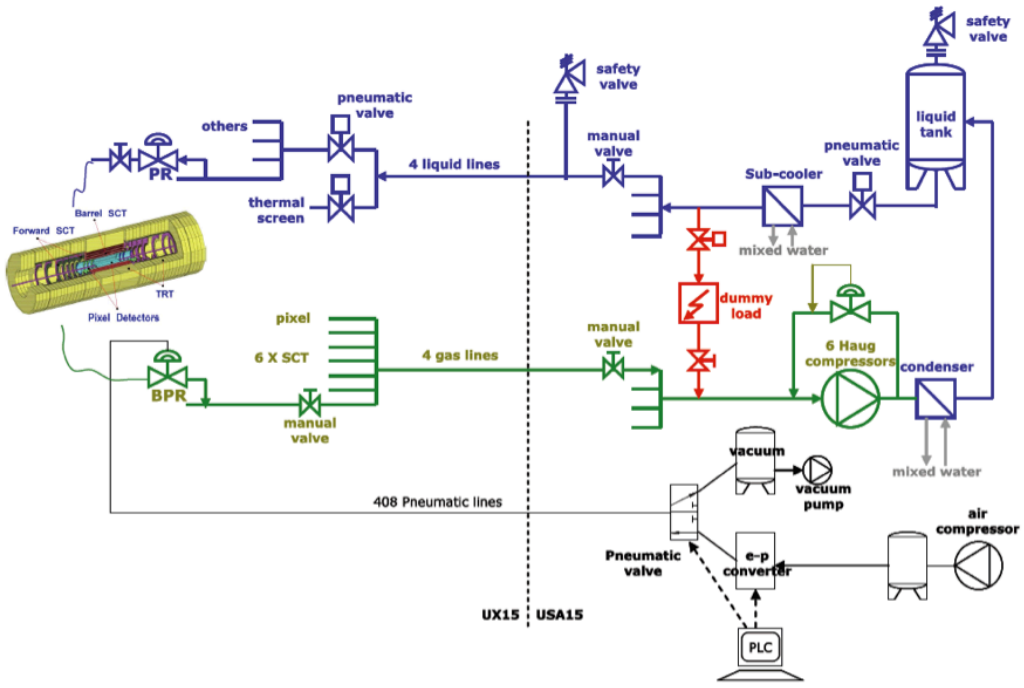


Figure 103. Schematic of the evaporative cooling plant of the ATLAS inner tracker. A more detailed P&I is available in [89] .

Although the experience obtained in designing, building and operating the plant is significant, the constraints related to the lower evaporation temperature and to the limited space for routing the cooling pipes, resulted in abandoning the fluorocarbon-based technology for a new cooling system based on CO_2 for the IBL.

The baseline technology is a CO_2 cooling system called 2PALC (2-phase Accumulator Controlled Loop) [90], which is already successfully used for the VELO detector of the LHCb experiment, Fig 104. The evaporation temperature is controlled by a two-phase accumulator which sets the evaporation pressure at the evaporator (detector). The coolant in the accumulator is in a saturated state and the set point is controlled by injecting or removing heat. The pressure at the accumulator is also the pressure in the exhaust line which is equal to the evaporation pressure considering negligible the pressure drops in the return line. The P-H diagram shown in Fig. 105 shows the saturation point set by the accumulator (labelled as point 1). A liquid pump raises the pressure up to the point labelled 2 in the figure. The pressure lift is used to set the desired flow rate through the loop. In the section 2-3, the liquid exchanges heat with the return line, and then it passes through a valve or a capillary (from 3 to 4). From point 4 to point 5 the coolant evaporates in the boiling channel of the detector, picking up the heat generated by the electronics. The saturated CO_2 passes then in the heat exchanger, which increases its vapour quality up to point 6. After that, the condenser takes the fluid to point 1, closing the thermodynamic cycle. Note that the condensation temperature is lower than the evaporation temperature. The fluid is therefore sub-cooled at the

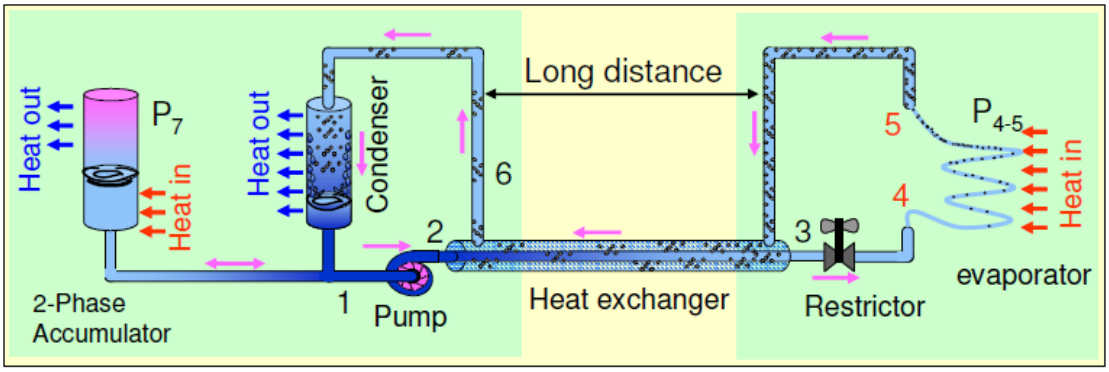


Figure 104. Schematic of the CO_2 2PACL system.

entrance of the pump to avoid problems due to cavitation.

6.6.1 Requirements for the IBL cooling plant

Chapter 4 covers the aspects of thermal management on the local structure of the detector in detail. The motivations supporting the requirements listed in this section can be found in that Chapter.

Cooling power and evaporation temperature

The cooling power is distributed on the detector over 14 boiling channels with a nominal cooling power of 100 W; the detector layout can be found elsewhere [91]. The nominal total power of the detector is therefore 1.4 kW. The cooling power of the plant has been set to 2.0 kW, which offers a safety margin of ∼40%. The heat load is meant to be removed from the structure at a maximum temperature of −30 °C. Since the pressure drop built up in the evaporation channel causes a thermal gradient along the axis of the pipe, the maximum evaporation temperature is

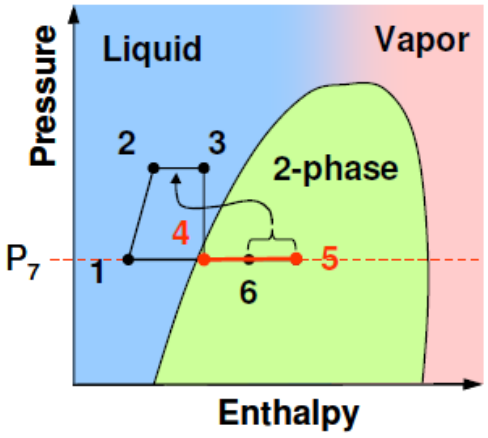


Figure 105. PH-Diagram for the CO_2 cooling.

Number of Loops	14
Evaporation T	-40 °C
MDP	100 bar
Nominal Power/Loop	100 W
Nominal Total Power	1400 W
Plant Design Cooling power	2000 W

Table 29. Main requirements for the IBL cooling plant.

considered to be reached at the inlet of the channel. At the exhaust, the value is lower and it has to count for the effect of the pressure drop. The Maximum Design Pressure (MDP) for the on- and off-detector pipelines is 100 bar.

Table 29 summarizes the main requirements for the cooling plant.

Modularity and temperature control

A common evaporation temperature is set for all the loops. Due to the limited radius of the detector layer [91], the thermal stratification in the detector environmental gas has a marginal impact on the sensor temperature and it does not justify a complex and discrete temperature control system at the level of single or multiple loops.

Leak tightness and reliability

The development of unexpected leaks of coolant is considered a serious safety hazard and a relevant operation failure. Besides, the CO_2 could become slightly activated making it important to minimise leaks. The importance of the cooling system commissioning and the adopted strategy is discussed in Section 10.2. Hereafter the general guidelines are collected:

- The piping and the connection of the plant should be designed and assembled following the standards for vacuum and cryogenic systems. Welding is always preferred, where possible, to flanges and seals.

- The leak rate of any bare piping section, vessels or equipment should be He-leak checked and tight at the 10^{-7} atm$\cdot$cc/s level. De-matable connections must be better than 10^{-5} atm$\cdot$cc/s.

The first *in situ* task for the cooling system of the IBL will be the bake-out of the beam pipe, that will reach temperatures above 200 °C. Details are given in Section 10.1.

6.7 Integration of Off-detector Systems with the Pixel Detector

The IBL needs to be fully integrated with the current, running Pixel detector. DAQ software and DCS software will be the same for the two detector systems. The strategy to reach this is twofold.

In terms of the detector control (DCS) the components of the two systems will be either the same or similar to facilitate the integration. The main component is the ELMB, which is widely used as measurement device in the Pixel detector and which is already implemented in the software control. Using the same software libraries and tools, including the ELMB based components is straightforward and only the IBL related datapoints must be generated. As for hardware, the IBL

supply devices should be very similar to the Pixel detector ones. For the low voltage, a similar or the same supply from the same vendor can be used. Experience from the Pixel detector using two similar devices of this type has shown good compatibility in control. The opto-board supply can be the same as in the Pixel detector, and the HV module depends certainly on the chosen sensor technology.

For the DAQ system, the hardware to be addressed is rather encapsulated in the low level structure. Since Inter Process Communication (IPC) is used to address the crate controllers, everything below is done such that different hardware can be managed on the same architecture. Implementing the read-out electronics using the VME architecture limits the new software development at the crate level. New data formats of the FE-I4 chips occur at the hardware level, and data and signals are compatible with the Pixel detector communication.

In this way, since both DAQ and DCS software are implemented in a modular way, the IBL can be integrated as an additional layer of the Pixel detector.

7. Installation

The Insertable *B*-layer will be installed on a new beam pipe inside the innermost layer of the current Pixel detector system. The present beam pipe (Phase 0, Ph0) shall be extracted and replaced with a support tube fitting just inside the present *B*-layer inner radius (without touching the *B*-layer). The new beam pipe (Phase 1, Ph1) equipped with the IBL detector will be then inserted into this support tube; the combination of the IBL and Ph1 beam pipe will be referred to as the IBL package. The Ph1 beam pipe shall have a smaller diameter than Ph0 to allow for safe clearances. Once in place the IBL will be supported from the support tube, not the Ph1 beam pipe. The Ph1 beam pipe will be mounted to the same support tube, but at different points.

The beam pipe extraction and insertion are inherently delicate operations due to both the fragility of the equipment manipulated and the limited space available. The IBL case presents two significant additional challenges: (1) the ATLAS detector was not designed for this operation and (2) there will be radiological activation of the working area and components. The Pixel detector and the Ph0 beam pipe were inserted int ATLAS as a package that was fully integrated on the surface, without the expectation that manipulation of the beam pipe as an independent unit would take place in-situ.

This chapter describes the UX15-cavern activities linked to the extraction of the Ph0 beam pipe, the installation of the Ph1 beam pipe and the the IBL detector, the installation of all external services for the IBL, and the requirements for radioprotection and safety associated with the installation steps. It reflects the current understanding of these operations, with the understanding that procedures will be adapted and optimized as development continues. The Ph0 beam pipe extraction will be defined and exercised on the surface and this will establish the shutdown scenario required.

The feasibility of such an extraction/insertion scenario and the associated tooling are not proven yet. A 1:1 scale mock-up of the relevant detector envelopes and interfaces is being prepared on the surface and will be used to validate and practice each step in order to arrive at a final sequence.

7.1 ATLAS Pit Configuration

The configuration of ATLAS is different from one end of the experimental cavern to the other regarding space availability and access to the ID. Fig. 106 shows sketches of the so-called *Large Opening* and *Standard Opening* configurations for sides A and C, respectively. Installation on side A is currently the IBL baseline, because the cavern access shaft on side A shaft is larger than on side C. This allows a wider range of crane movement in directions X and Z. Side A installation requires a *Large Opening* on side A and a *Standard Opening* on side C.

On side C, the layout of the *Standard Opening* is sufficient to grant worker and light tooling access to the end of the ID and the beam pipe (no crane access). The Endcap Toroid C is moved on the *Light Truck* by approximately 5.4 m along z, the Small Wheel is moved back, and the Endcap Calorimeter is moved by 3.1 m. In contrast, on side A the *Large Opening* requires the Endcap Toroid A to be moved back in z and then sideways on the *Light Truck*. The HF truck is then positioned along the axis of the detector so that it extends the support rails. The Small Wheel is moved back underneath the cavern access shaft and lifted to the surface. Finally, the Endcap Calorimeter is moved back.

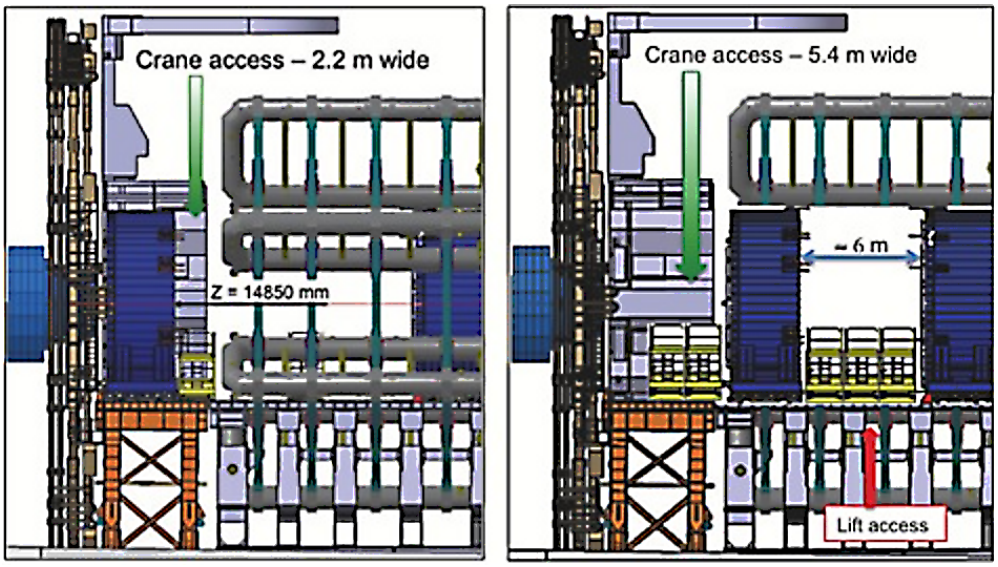


Figure 106. Schematic view of the *Large Opening* and *Standard Opening* configurations in the cavern, for sides A and C, respectively.

The estimated time to reach this opening configuration is 10 weeks. Once the IBL has been installed and connected, it should take also 10 weeks to go back to the closed (data-taking) configuration of the experiment.

7.1.1 Large opening configuration

In *Large Opening* configuration proposed for side A, the Endcap Calorimeter must be moved back by 11.5 m to allow crane access between the Endcap Calorimeter and the Barrel Calorimeter (Fig. 106). Access for personal and equipment is granted on dedicated movable platforms called *Minivans*.

A *Minivan* looks like a stiff bridge resting on the ATLAS rails (Fig. 115). It provides a platform area of 6 m by 1.8 m and withstands a load of 1.5 T. The *Minivans* are lowered from the surface to the ATLAS rails using the 20 T crane, then they are translated along the Z-axis towards the Barrel Calorimeter; as the *Minivan* is equipped with rollers, this movement is performed by 2 persons without any additional tooling. Up to 6 *Minivans* can be installed between the Barrel and the Endcap Calorimeters. Once installed, the *Minivans* offer a reasonably flat area of about 60 m^2, located 2.4 m below the beam axis. To allow convenient access to personnel, scaffolding must be built on a *Minivan*. An extension frame can be installed on the top of the *Minivan* to allow the detector insertion. The extension frame is as wide as the *Minivan* (1.8 m) but 4 m long instead of 6 m. It is 1.4 m high, so that the platform is 1 m below the beam axis.

Crane coverage on side A is large enough to ensure the full positioning on the *Minivans*. However, the Ph1 beam pipe plus IBL cannot be lowered in a straight line because of various obstacles on the way, like the cryogenic line of the Endcap Calorimeter or the service chain at the top of the Endcap Toroid. A detailed study is still necessary to check every conflict and to define precisely the path of the descend from the surface to the rails.

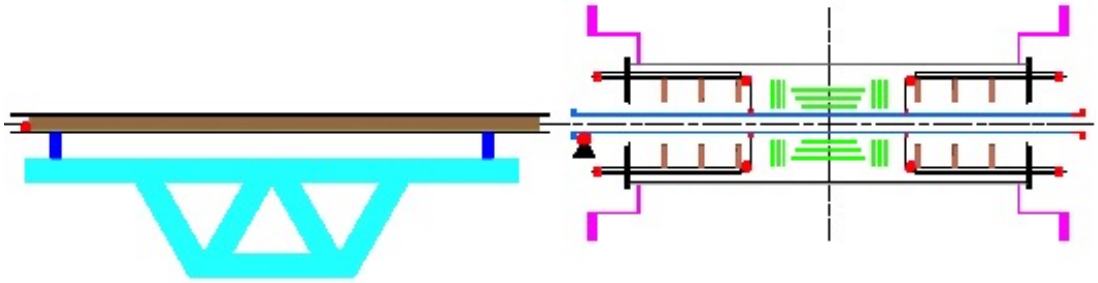


Figure 107. ID open, *Long Guiding Tube* on Extraction/Insertion table.

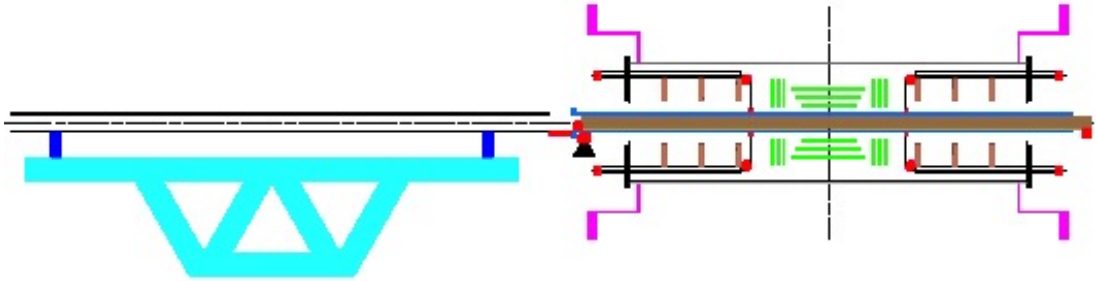


Figure 108. *Long Guiding Tube* inserted in Ph0 Beam Pipe.

7.2 Ph0 Beam Pipe Extraction

Preparation work consists of opening the ID ends, removing the external beam pipe sections, and freeing the beam pipe from services and bellows on sides A and C. A so called *Long Guiding Tube* is then inserted into the beam pipe and supported at both ends (Fig. 107 and Fig. 108). With the *Long Guiding Tube* in place beam pipe can be freed from the side C extremity flange (buy sawing off a section) and disconnected from the wire system and the cruciform supports that presently support it. The full load is then taken by the *Long Guiding Tube* (Fig. 109). The main technical problem is deflection (gravity sag) in the Pixel detector region. The *Long Guiding Tube* can not be a simple object to achieve the required sag control. Engineering design of a complex tool (active or pretensioned or both) is ongoing.

The operation of sawing off the flange is clearly not reversible, but it is necessary as the flange is too large to pass through the *B*-Layer. The extremity of the beam pipe to be cut is made of aluminum (Fig. 111). This main concerns are preventing projection of chips or dust and radioprotection considerations.

Guided by the *Long Guiding Tube*, the beam pipe will be pulled out onto the Extraction/Insertion table. An few clearance to the *B*-layer must be guaranteed during the extraction. Once extracted, the beam pipe will be packed into a *Shielded Carrier* to be evacuated from the cavern (Fig. 110).

7.2.1 Geometrical constrains

From the IBL perspective, the pixel environment is mainly defined by the current *B*-layer. Its

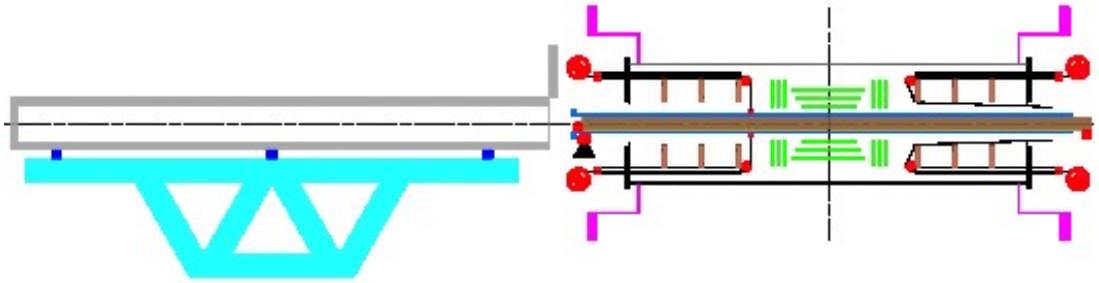


Figure 109. Shielded carrier on Extraction/Insertion table ready to take the Ph0 Beam Pipe.

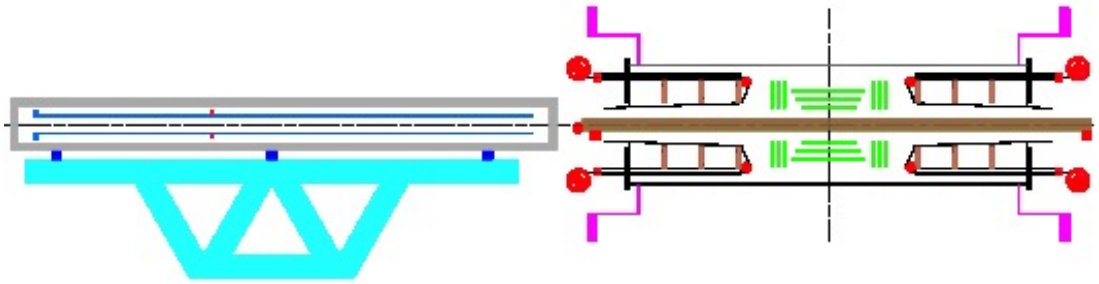


Figure 110. Ph0 beam pipe extracted in the shielded carrier.

geometrical envelop is shown in Fig. 112.

As for services, in the PP1 area many services are located in the vicinity of the beam pipe limiting the space in the area (Fig. 113). Nevertheless, a minimum of space is necessary to perform the mechanical work needed to disconnect bellows and rings, and later to extract the beam pipe. With

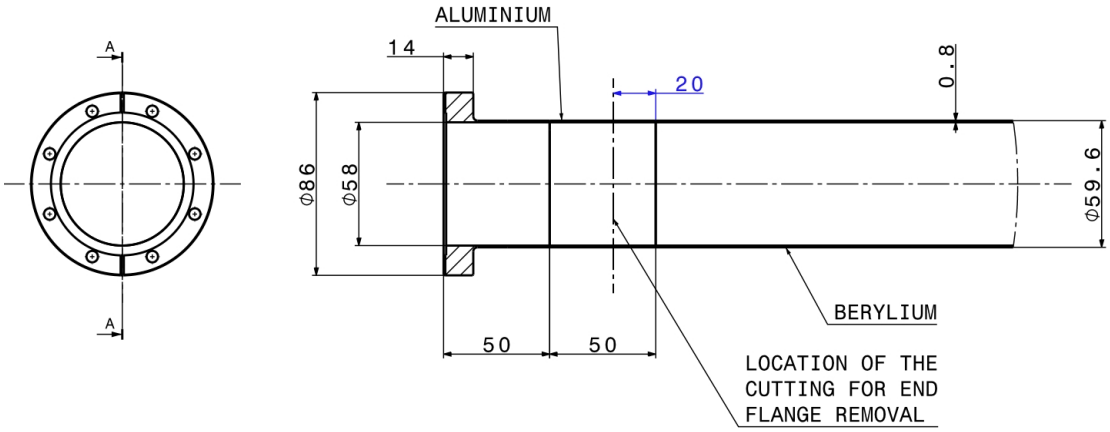


Figure 111. Extremity of the beam pipe where it is foreseen to be cut for its safe extraction.

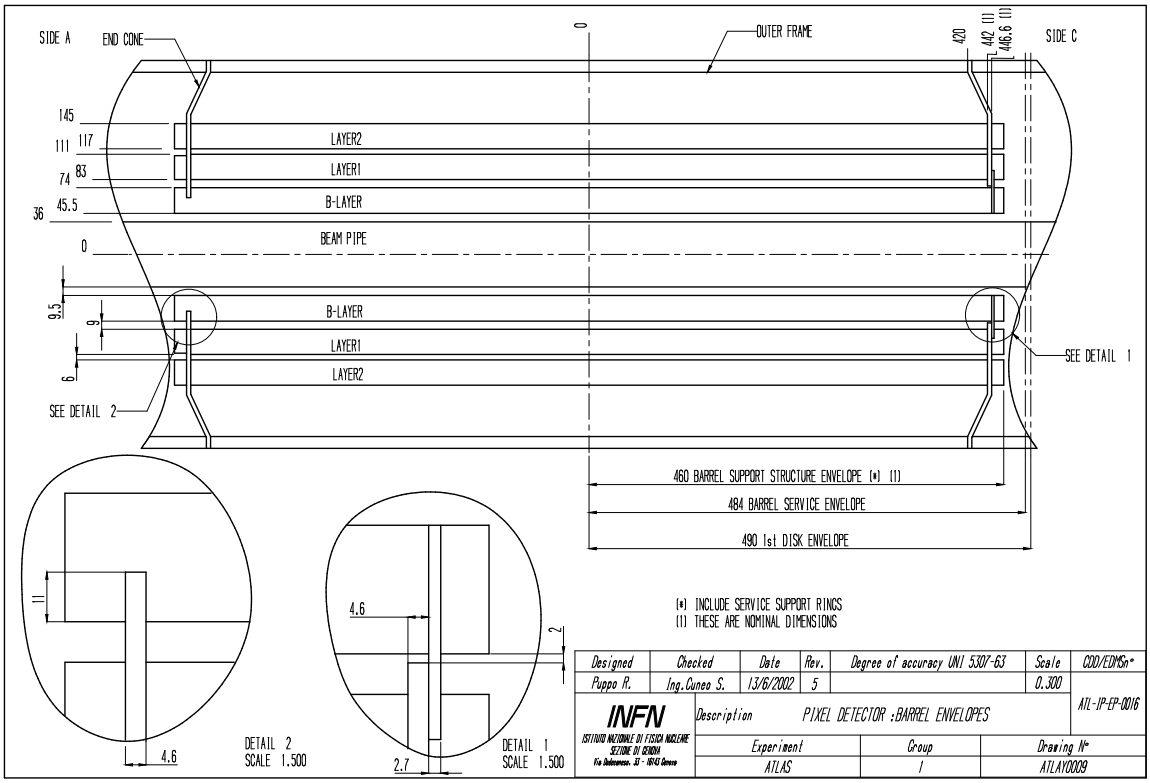


Figure 112. Geometrical envelop of the ATLAS Pixel detector.

precaution, services will be arranged to insert a cylindrical protection. This cylindrical protection will act as a working space limitation and will protect the services against any damage during the extraction and insertion operations.

7.2.2 Tooling

Wire removal tool

The current beam pipe is fixed at Z= $\pm$3400 mm by the cruciform support and at Z= $\pm$850 mm by a pre-tensioned wire system. These wire systems allow the adjustment of the beam pipe's central part. The pre-tension plays a dumping role in the dynamic behavior of the beam pipe. In order to remove the Ph0 beam pipe the wire system shall be disconnected from the beam. All disconnected wires shall be captured by the tooling to allow the support of the Ph1 beam pipe. The functions of the tooling are:

- Disassemble the collars supporting the beam pipe.
- Capture the wires to be re-used for the support of Ph1 beam pipe.
- Capture the different pieces of the collar to avoid any pieces left in the ID.

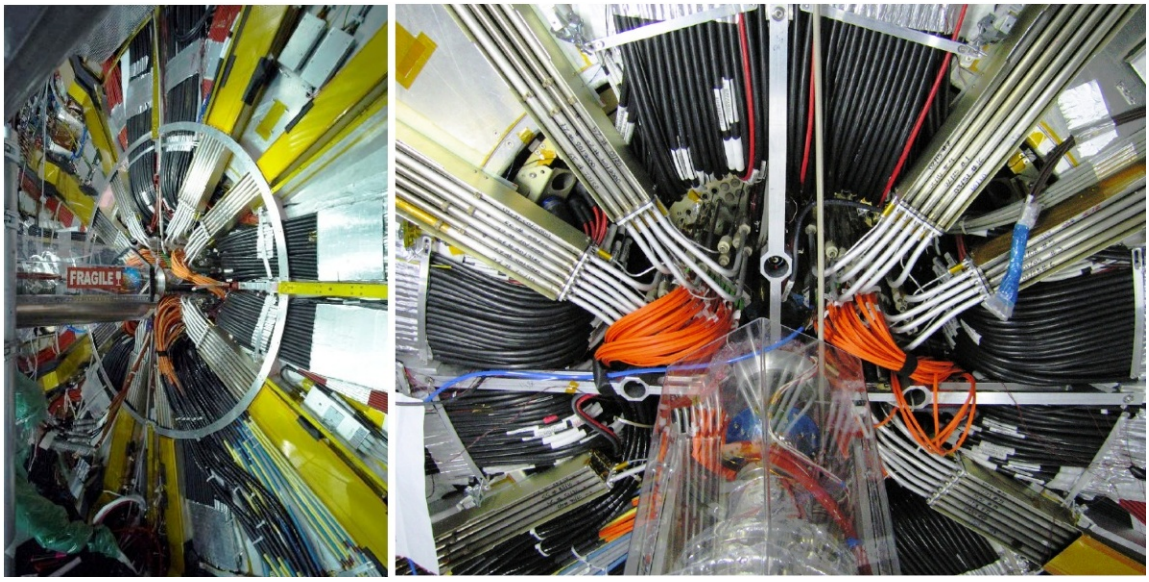


Figure 113. Pictures of PP1 services around Ph0 beam pipe on side A: full end plate view (left) and detail (right).

Many constrains have to be mentioned for the design of this equipment. A picture of an existing prototype is shown in Fig. 114.

- This tooling has to be operated remotely, as the wire system is not visible from outside the ID.
- The space available for the tooling insertion through the cruciform windows is limited to x mm of inner diameter and 92 mm of outer diameter.
- The introduction of the tooling will be guided by the outer surface of the beam pipe. This surface is made of wrapped aluminum. Despite the fact that the envelope was measured the current conditions of the aluminum is unknown.
- The working time for the intervention shall be limited since the working environment will be activated. Intervention time will be defined by the radioprotection experts.

Long guiding tube

An internal mechanism is being developed to actively compensate the saggita such that the *Long guiding tube* will have a constant vertical position in the IBL area (length of this area Z $\pm$400 mm). The position of the *Long guiding tube* in the pixel area shall within a range of $\pm$2 mm.

The function of the *Long guiding tube* is:

- To support the Ph0 beam pipe during its extraction and the *Inner Support Tube* during its insertion.
- To guide the Ph0 beam pipe and the *Inner Support Tube* such the gap between the beam pipe and Pixel *B*-layer is not smaller than 1mm.

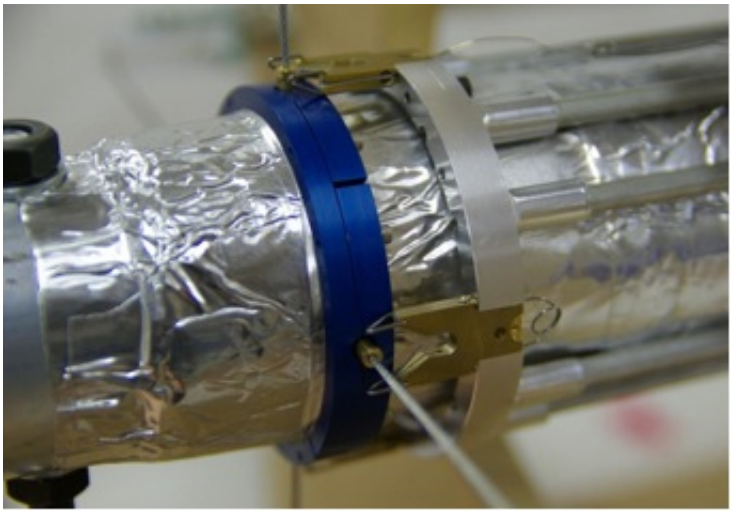


Figure 114. Picture of wire removing tool prototype.

- To embed the necessary equipment to control the saggita.

Many constrains have to be mentioned for the design of the *Long guiding tube*: its overall size shall be compatible with the inner diameter of the Ph0 beam pipe (58 mm) and its surface shall allow sliding the Ph0 beam pipe during its extraction and the *Inner Support Tube* during its insertion.

The feasibility of a tooling with such requirements has not been proven yet. Several engineering studies are currently run in parallel and most probably several prototypes will be used to better understand the mechanical behavior of such a slender pipe. The current idea is to develop a pipe with an internal displacement measurement system that can pilot actuators modifying the geometry to compensate the deflection in the pixel region.

Insertion/Extraction table

The so called *Insertion/Extraction table* (Fig. 115) will guarantee the movement, in and out of the ID, and the support of the following elements: *Long Guiding Tube*, Ph0 beam pipe, IST, and IBL package. This table will also allow the reception and delivery of the previously listed elements when brought/taken by the 20 T surface crane. This means that this table is movable both in rotation and translation to bring the previously listed elements in front of the ID. The *Insertion/Extraction table*, once in front of the ID, will be positioned thanks to geometrical surveys.

In addition to the functions already mentioned, the *Insertion/Extraction table* shall provide a constant speed during the Insertion/Extraction phases. The speed is linked to the reaction time of the *Long Guiding Tube* and will be defined when the design of the *Long Guiding Tube* is completed. Monitoring the extraction force would be an asset as it will detect any conflict or contact during the extraction/insertion phases.

Shielding and transport container

The function of the shielded transport container is to shield radiation from the Ph0 beam pipe as soon as it is extracted from the ID. It will also carry the beam pipe out of the cavern to be stored in the radioactive buffer zone. Depending on the final details of the tasks described above and their risk, the possibility to ask for the expertise of a specialized company is still open.

7.3 Preparation for Insertion

Preparation work shall start as soon as the Ph0 beam pipe is evacuated. The main task is inserting the IST, as shown in Fig. 116.

The IST will be supported and guided by the *Long Guiding Tube* during its insertion. The soundness of the Pixel *B*-layer shall be guaranty by keeping sufficient gap between the *IBL support Tube* and the *B*-layer (Fig. 117).

Once in place, the IST will be connected to the ID by a wire system and through the cruciform supports, as shown on top of Fig. 118). This wire system is presently used for the Ph0 beam pipe on both sides of the Pixel *B*-layer (Fig. 119 a) and at the extremities at the cruciform support rings (Fig. 119 b). A new wire system interface needs to be developed because the one used to support the Ph0 beam pipe does not match the IST dimensions.

At this stage the *Long Guiding Tube* can be extracted, supported on the IST (bottom of Fig. 118). Then the positioning process of the IST can take place based on survey measurements. The survey protocol needs to be developed in partnership with the CERN survey team and the pixel system community.

The IST is a 6600 mm long tube made of carbon fiber (Fig. 117). The inner diameter is 85 mm but the thickness is to be defined from a global calculation of the IBL package with the IST, but it cannot exceed 2 mm to keep the outer diameter below 87 mm. The IST provides support to the Ph1 beam pipe and the IBL during and after insertion and to protect the *B*-layer. The design of the IST shall also control the positioning of the IBL active elements through interfaces with the stave

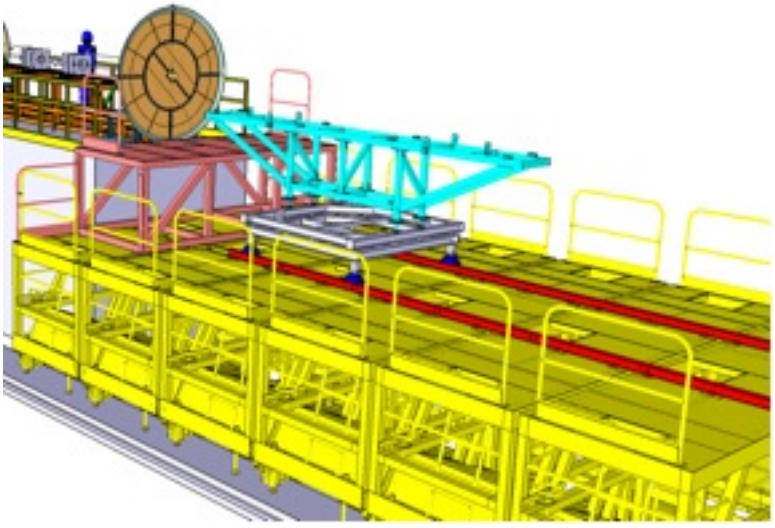


Figure 115. Simplified scheme of the *Insertion/Extraction table* with translation rails and rotation table.

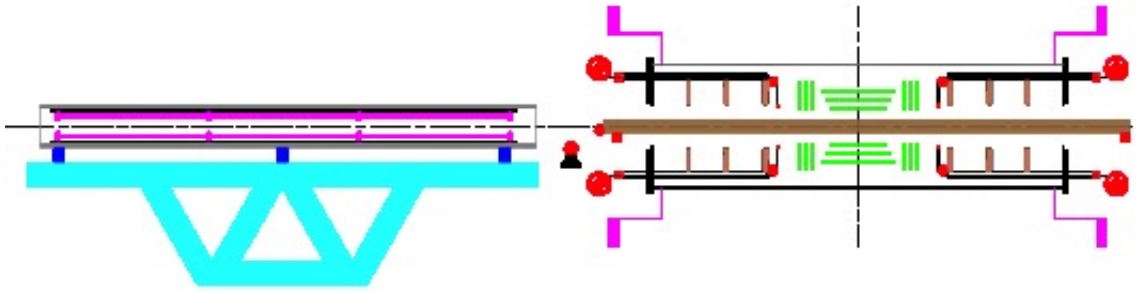


Figure 116. *IBL Support Tube* and space frame on the Insertion/Extraction table, ready for insertion.

support ring. The engineering development of this interface is ongoing, in parallel with technical discussions with industry.

7.4 IBL Insertion

In addition to the shielded carrier needed for the extracted Ph0 beam pipe, another special container is required to carry the Ph1 beam pipe together with the IBL package from the assembly hall to the *Insertion/Extraction table* in the cavern. This is very similar in nature and requirements to the Dummy Support Tube (DST) used to transport and install the present Pixel detector. At that stage, the interface between the IBL package and the *Insertion/Extraction table* will be the services support ring (Fig. 120).

The IBL package will be transferred onto the IST from the *Insertion/Extraction table* (Fig. 121). The IST supports and guides the IBL package during insertion. The final position and the isostatic

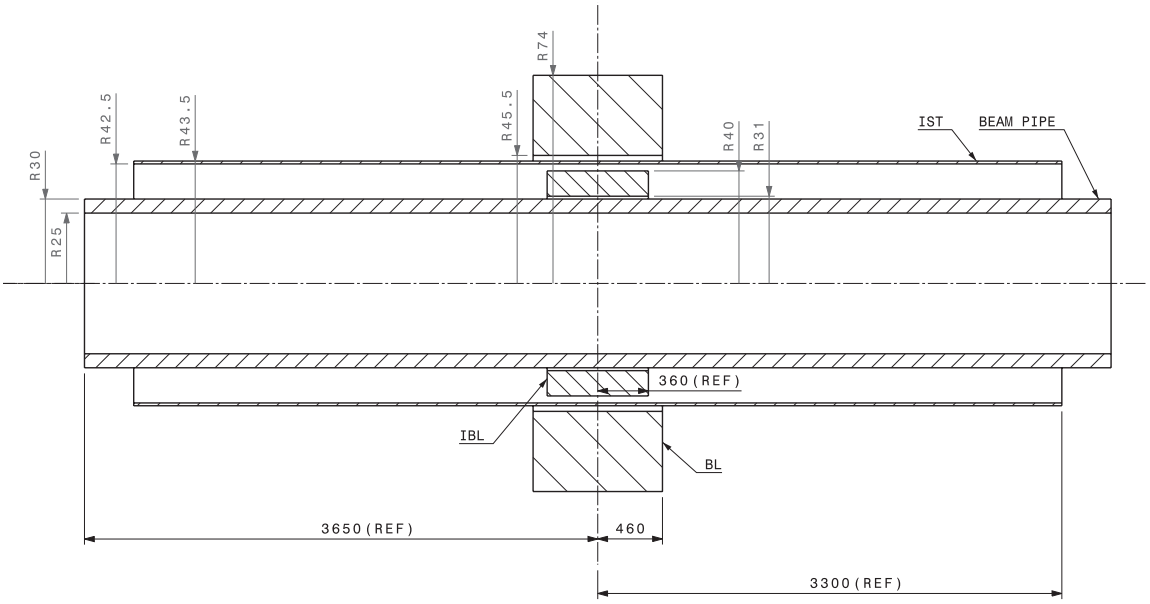


Figure 117. IBL envelop.

support will be guarantied by a mechanism embedded into the IST and stave support rings. This mechanism still needs to be designed and tested.

Once the IBL package is in its final position the services connection at PP1 can start. After commissioning the services, the ID can be closed and the access equipment removed.

7.4.1 IBL services

The IBL package contains the *internal* services that must be connected to their *external* counterparts after insertion. While the arrangement at the extremity of the beam pipe is not yet detailed, it is clear that internal services must extend beyond the Ph1 beam pipe at least on the side passing through the IST, in order to fit the radial envelope. A possible arrangement is shown in Fig. 122. The extra length of services shall be around 50 cm to allow them to reach the PP1 connection points after unfolding. The services folding and bending must be prototyped and validated.

The routing of the present pixel Type II services was very challenging due to limited space along the path from PP1 over the ID End-Plate (IDEP) and the cryostat flange up to the feedthroughs between the LAr crates. A number of additional cables have been later installed for the heaters of the evaporative cooling circuits. The result is that most possible paths for IBL services are 100% full. This means that the new services for the IBL will have to follow paths dictates by available space and these paths will not be straight. The detailed routing must be determined in advance, to prevent workers for spending extra time in the radioactive environment.

Based on the estimate for the cables and fibers given in Chapter 6 and taking a conservative estimate for the cooling pipes, cross sections of the order of 30 cm^2 and 10 cm^2 on Side-A and

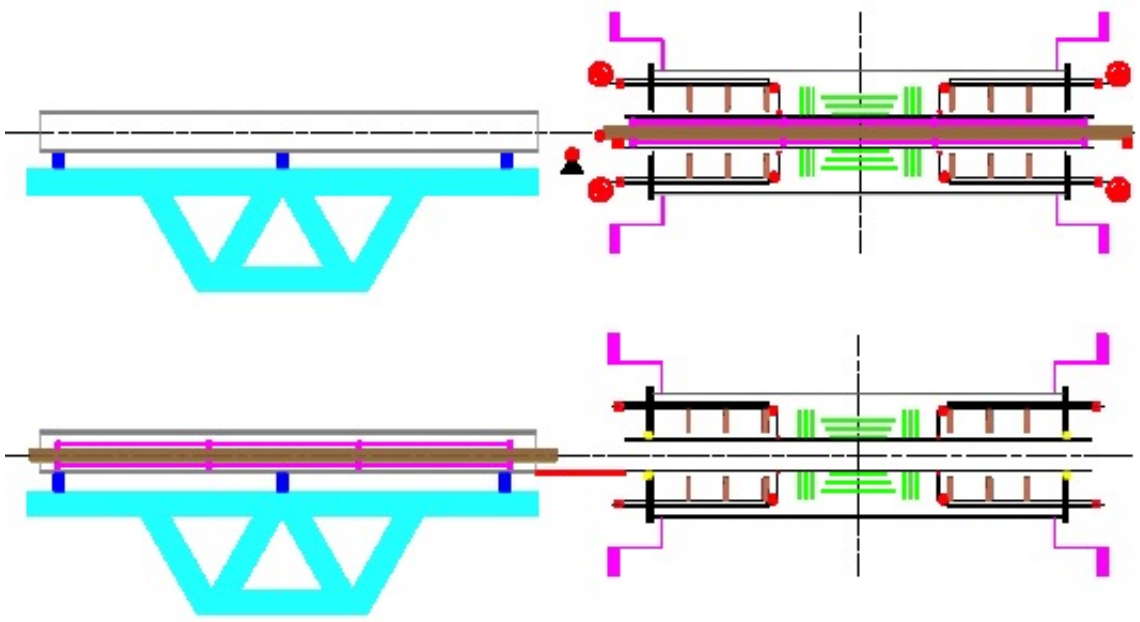
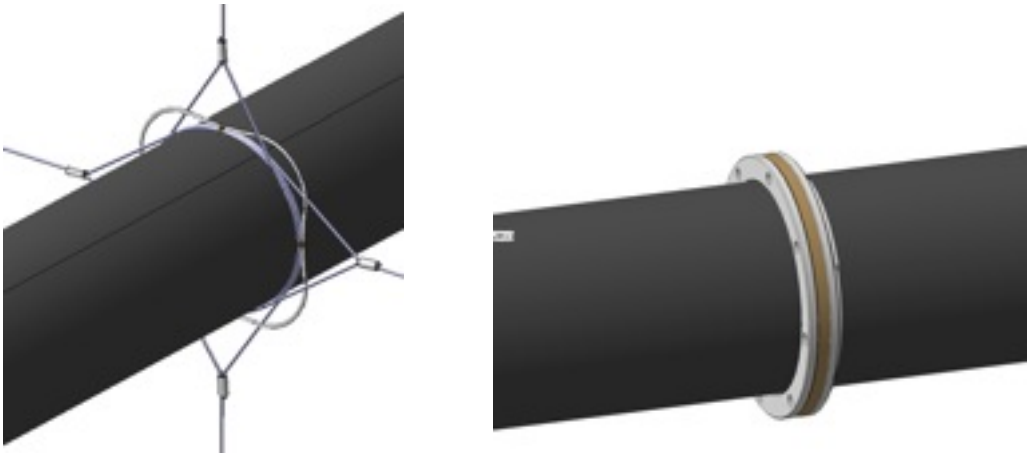


Figure 118. (top) *IBL support Tube* and space-frame inserted around the *Long Guiding Tube* inside the ID; (bottom) *Long Guiding Tube* and Space-frame extracted from the ID.



(a) Possible wire interface around the IST

(b) Possible interface at the cruciform ring

Figure 119. IST supports.

Side-C have been determined to be necessary to route the cables/fibers and pipes, respectively. For these estimates, a packing factor of 1.3 has been applied.

A study has been performed using metrology data from the last IDEP-open period in order to identify possible routing. This study includes the space constraints on the IDEP and the cryostat flange, as well as the feedthroughs and the PP2 regions. Most available space at large radius is on the lower part of the flange and corresponding feedthroughs, whereas at small radius space

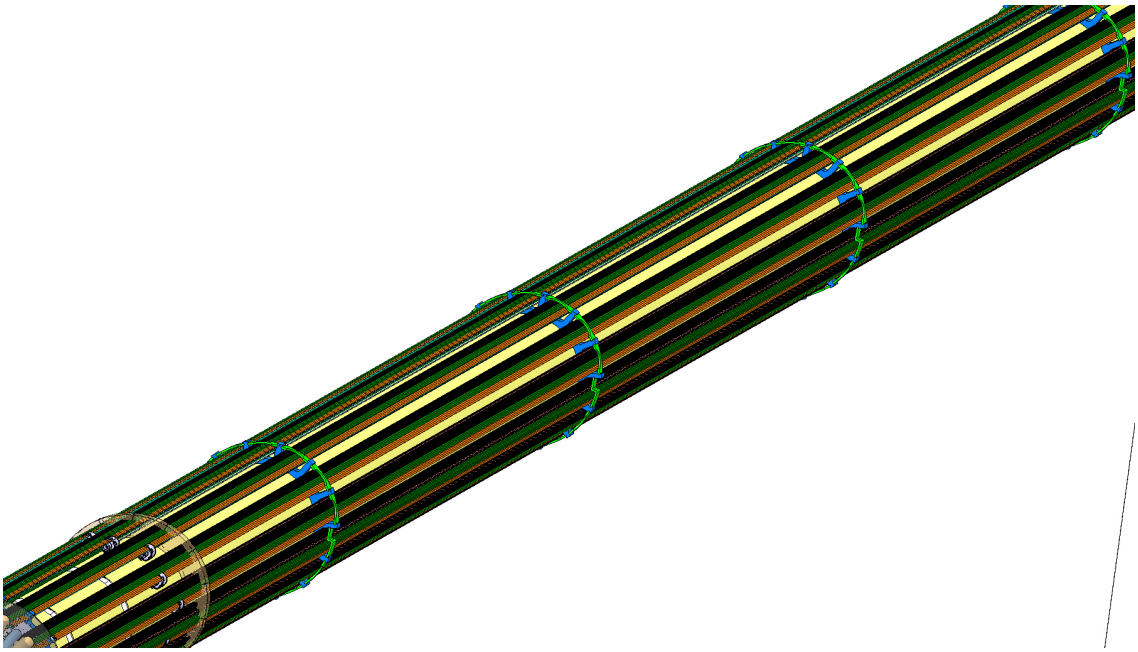


Figure 120. Services support ring, interface between IBL and the *Insertion/Extraction table* during the transport.

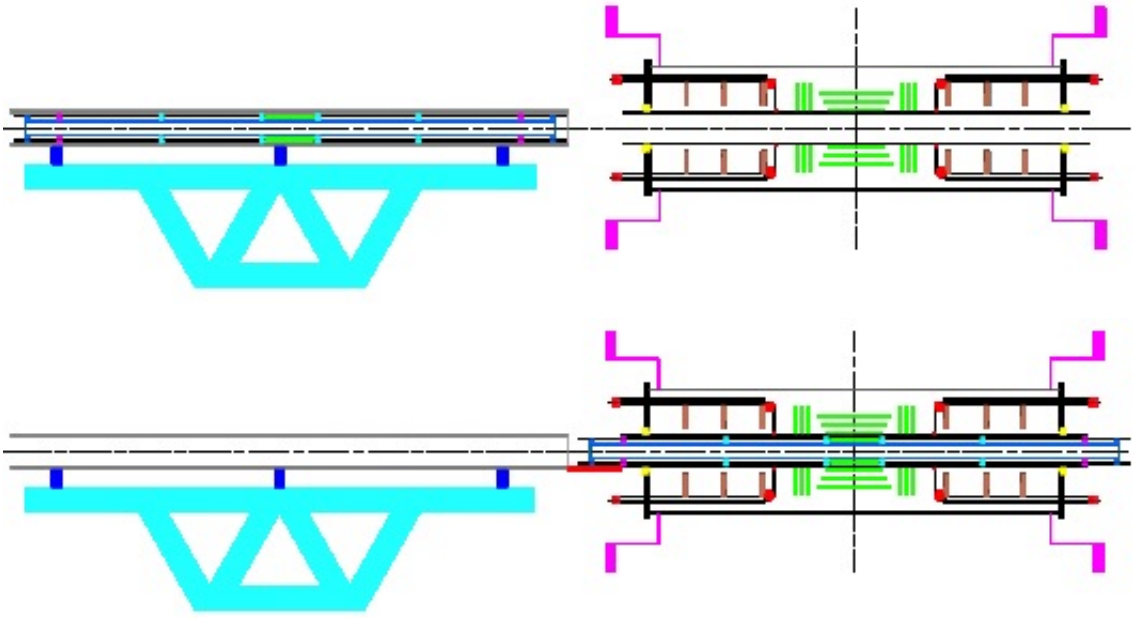


Figure 121. (top) IBL package on *Insertion/Extraction table* ready for insertion in the IST; (bottom) IBL package inserted in the IST.

restrictions are less severe on top, but crossing from bottom to top is impossible on the flange. In addition, the PP2 areas in sectors 3 and 7 do not allow new electronics to be installed, and there

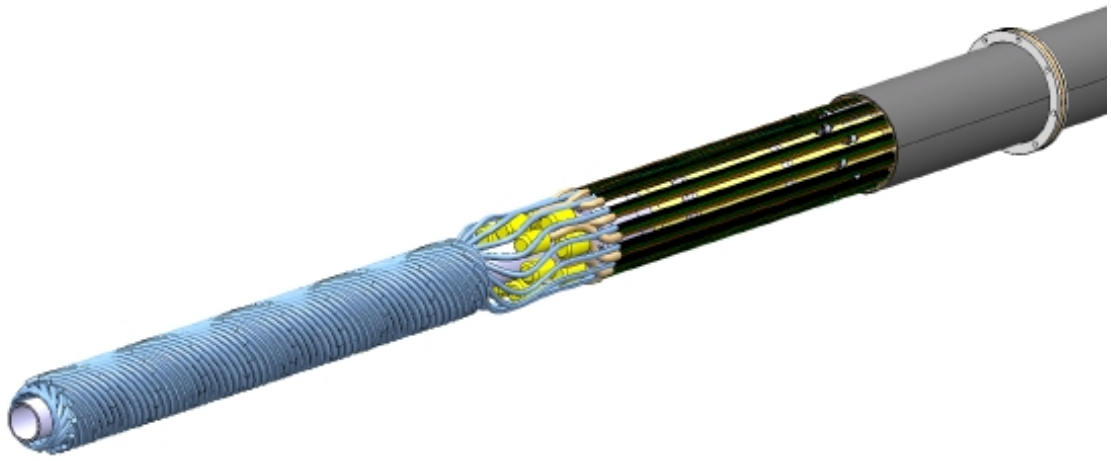


Figure 122. Possible arrangement of services at each extremity of the beam pipe during insertion.

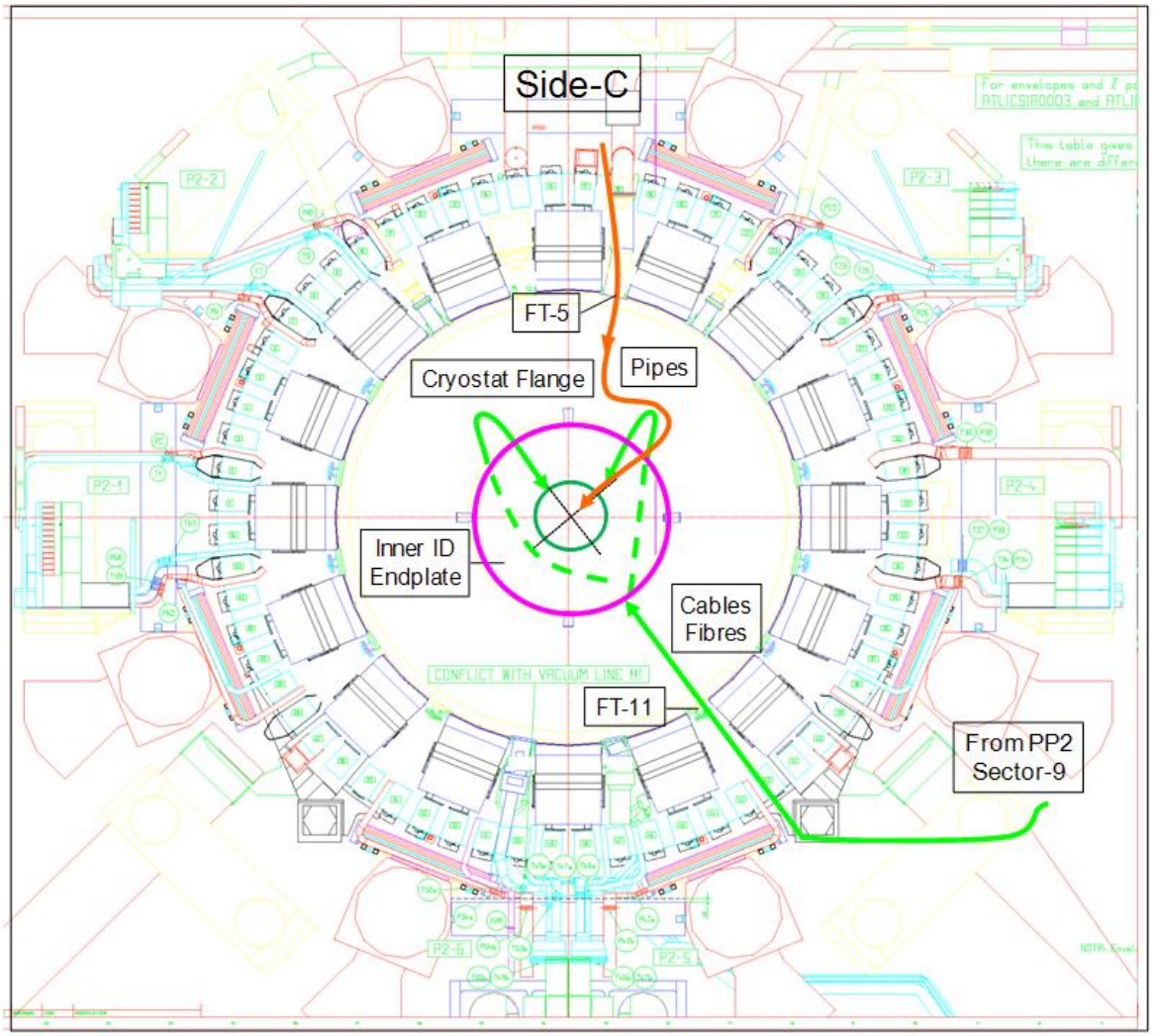


Figure 123. Cables/fibers and pipes installation on inner ID endplate and cryostat flange.

is a clear preference to bring the services to USA15 compared to US15 for accessibility reasons. Two routing scenarios could be identified respecting these constraints: one for the cables/fibers and another for the pipes, as illustrated in Fig. 123.

The cables and fibers will be installed from PP1 in two bundles on top of the inner IDEP up to openings in the cryostat chamfer region in sectors 3 and 7. From these openings they will continue behind the inner IDEP and join a chamfer opening in sector 11. The routing behind the inner IDEP has already been tried and validated. It continues on the cryostat flange in sector 11 straight ahead to feedthrough-11 and from there to PP2 in sector 9, following the existing Pixel cables. The installation from PP2 in sector 9 to USA15 is not critical and will go along existing cables. In addition, three potential positions for the Opto boards have been identified on the flange; the choice will depend on the final design of the box which will house the boards.

On the other hand, the pipes will be installed from PP1 on top of the inner IDEP to the cryostat

flange in sector 7. From there they will be routed to sector 5 and through feedthrough-5 along the Barrel up to Z0. They will continue to join the evaporative cooling rack on Level-7 (USA Side) and from there they will follow the existing pipes up to the CV room in USA15. This routing has been chosen because sector 5 is rather free and because it offers enough flexibility to accommodate the two cooling versions for which space is needed, in one case for manifolds and in the other case for heaters (see Section 10.2).

After the identification of the above routing, envelope measurements have been performed on the flange in order to quantify the available space and to validate the scenarios. With this information a 3D CAD model is being created to calculated dimensions for all the services. 3D maps of the endplate service, which were recorded the last time the areas were accessible, will be used to validate the models. Some of the routing has already been anticipated by re-arranging the existing cables in certain regions on the flange and by displacing electronics boxes on the inner IDEP.

In summary, a solution for the installation of the IBL services has been found. The solution offers the advantage that the routing on sides A and C will be the same. Furthermore, only few outer IDEP panels have to be removed, shortening the installation time. Part of the outer services installation could take place well in advance during earlier shutdown periods.

7.5 Mock-Up

The development of a pure mechanical full-size mock-up of the IBL environment is an ongoing activity. The elements like beam pipe, Pixel *B*-layer, wire suspension system, all services in PP1, cruciform, ID end plate, etc. will be represented in the mock-up. The mock-up will be used to validate the whole extraction/insertion scenario. It will also allow the test, optimization and validation of all extraction/insertion tooling. Practicing procedures on the mock-up will help minimize personnel exposure to radiation, and provide data for calculation of expected radiation exposure.

The elements in the mock-up are:

- ID end-plates (Sides A and C),
- services environment in the PP1 region
- environments around the beam pipe in its full length
- the beam pipe
- all beam pipe mechanical connections (bellows, support, wire system, rings, etc.), and
- adjacent envelopes of the Pixel *B*-layer and Pixel discs.

The working environment will be as close as possible to the cavern environment. As an example, it is planned to equip the mock-up with the same personnel access and working platforms as those that are going to be installed in-situ. The whole mock-up will be inclined by 0.7° as is the real detector. While reproducing the real constraints, the mock-up will at the same time allow witnessing the extraction/insertion operation in details. View points will be installed at several positions to allow demonstration of the operations to outside observers. The mock-up frame (Fig. 124) in already under construction. The frame will then be equipped with all accessories (services, wire suspension system, bellows, dummy beam pipe, etc.) during 2010 (Fig. 125).

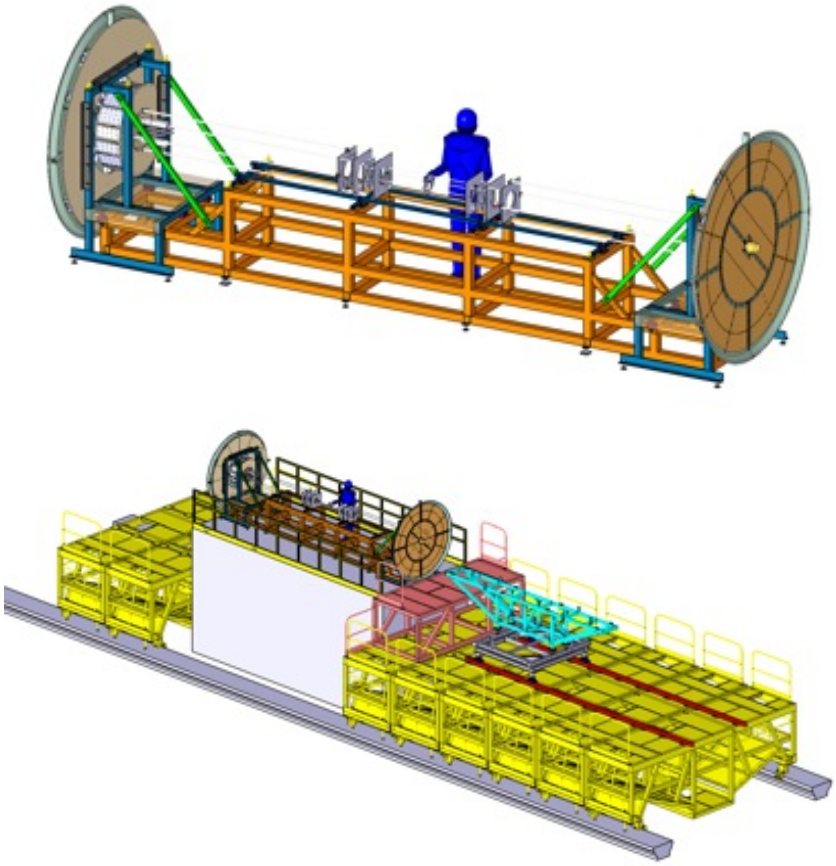


Figure 124. Different views of the mock-up.

7.6 Radioprotection and Safety

The installation activities will take place in areas that have been exposed, after some years of LHC operation, to a potentially significant radiation load. The levels of radioactivity from activated components close to the beam pipe will trigger radioprotection measures that can be driving constraints

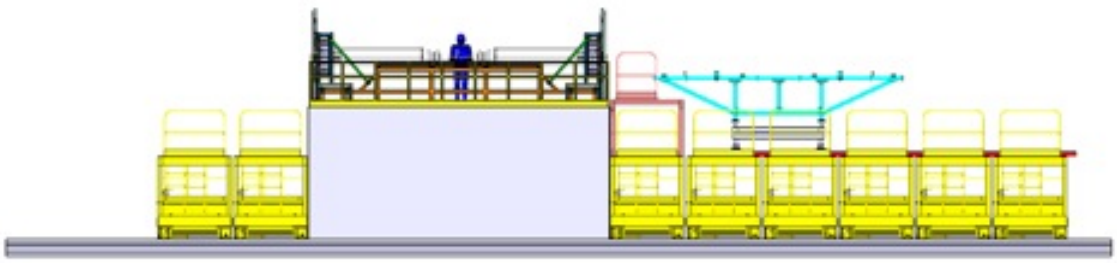


Figure 125. Full-size mock-up arrangement in building 180 to test and validate tooling.

for the work procedures. There is a radioprotection group within ATLAS Technical Coordination, which must work together with the CERN radioprotection (RP) group to assess the hazard and develop appropriate controls.

CERN RP regulations are reminded in the sections following, especially for what concerns the classification of areas and for the ALARA principle, which is basically the optimization of the doses received by the intervening personnel. The ATLAS safety strategy is to study and control all the ALARA aspects of the IBL installation from the design phase to its installation, and to develop the required necessary assisting tooling and databases.

7.6.1 CERN regulations and area classification

The CERN general rules for radioprotection are detailed in Safety Code F. The ALARA general principles are provided in the *Regles Generales de Sureté*. This regulation has been approved by CERN, the French and Swiss national nuclear authorities in a tripartite agreement. Table 30 shows the classification of ATLAS areas and their dose limits, using the following definitions:

- Low-occupancy areas: an individual spends less than 20% of his working time in these areas.
- Specific surface contamination: surface density of activity in Bq/cm^2.
- Specific airborne radioactive material (airborne radioactivity): activity concentration of gases and airborne aerosols, in Bq/m^3.
- CS, Guideline value of specific surface contamination: the specific surface contamination (in Bq/cm^2) which, according to model calculations, may expose a worker by ingestion or inhalation to an effective dose of 0.5 mSv per year or 0.25 μSv/h.
- CA, Guideline value for specific airborne radioactivity: inhalation of air with a specific airborne contamination of CA during 1 hour will lead to an effective dose of 10 μSv.

7.6.2 Evaluation of the radiation environment

The activation of the ATLAS detector has been calculated for 10 years of operation at $\mathscr{L} = 10^{34}$ cm^{-2}s^{-1} and 100 days of cool down. These calculations must be re-run using a highest expected integrated luminosity at the time of IBL installation. Calculations must also be validated

Area Classification	Dose Limit	*- Ambient Dose Equivalent Rate -* Permanent Work Places	Low Occupancy Areas	Specific Airborne Radioactivity	Specific Surface Contamination
Non-designated	1 mSv/y	< 0.5 μSv/h	< 2.5 μSv/h	0.05 CA	-
Supervised	6 mSv/y	< 3 μSv/h	< 15 μSv/h	< 0.1 CA	-
Simple Controlled	20 mSv/y	< 10 μSv/h	< 50 μSv/h	< 0.1 CA	-
Limited Stay	20 mSv/y	-	< 2 mSv/h	< 100 CA	< 4000 CS
High Radiation	20 mSv/y	-	< 100 mSv/h	< 1000 CA	< 40000 CS
Prohibited	20 mSv/y	-	> 100 mSv/h	> 1000 CA	> 40000 CS

Table 30. Area classification.

by measurements of actual activated components. Some measurements will be possible in the 2012 shutdown, but integrated luminosity at this time will be low. Additionally, material samples with remote extraction mechanisms have been placed in at several radii in the ID endplate areas. these samples can be removed, measured, and replaced during normal running years in order to monitor the actual activation and calibrate the predictions. By far the most active components are expected to be the beam pipe and flanges, and the end cap calorimeter. After the calorimeters are parked in the open configurations and the beam pipe sections outside the ID have been removed, the radiation levels in the work areas are expected to decrease by more than a factor of 2.

7.6.3 ALARA strategy

The ALARA principle aims to minimize the personnel exposure to radiation. The ALARA strategy must be integrated and applied at all phases of a project: design, installation, commissioning, maintenance and disposal. The general ALARA principles at CERN are described in the *Regles Generales d'Exploitations, Consignes Generales de Radioprotection*.

All activities related to installation will be reviewed and monitored by the ATLAS radioprotection team in collaboration with the activity responsible and the CERN RP group. The following steps will be followed:

- The dose rates are calculated and optimizations are proposed during the whole design phase.
- The potential sources of contamination are identified; if required, specialized companies will be contacted for advice or direct assistance.
- The activities are classified by CERN RP group in collaboration with ATLAS RP group.
- In parallel, specific radioprotection devices (such as shields and monitors) will be developed to assist the intervening persons to control in real time the exposure during the intervention.
- The removal/installation procedures and the developed tooling will be tested in the surface mock-up to predict the exact dose that each worker can receive. This will result in further optimization. The above radioprotection devices must also be tested and qualified.
- Before the start of work , final ALARA analysis and working authorization delivery.
- During the intervention period and for the most risky activities, the ALARA parameters will be reassessed on daily basis and if required working procedures will be corrected accordingly.

A radiological level of risk classification will be assigned taking the most stringent out of the following 5 criteria:

- Dose rate in the area of intervention
- Individual dose collected per intervention
- Collective dose collected per intervention
- Atmospheric contamination

ALARA Classification Criteria	Level 1	Level 2	Level 3
Dose Rate H (*)			
in the area of intervention	$H < 50\ \mu Sv/h$	$50\ \mu Sv/h < H < 2$ mSv/h	2 mSv/h < H
Individual Dose H_i (**)	$H_i < 100\ \mu Sv$	$100\ \mu Sv < H_i < 1$ mSv/h	1 mSv < H_i
Collective Dose H_c (***)	$H_c < 500\ \mu Sv$	$500\ \mu Sv < H_c < 10$ mSv/h	10 mSv < H_c
Atmospheric Contamination C_a	$< 5\ C_a$	$5\ C_a << 200\ C_a$	$< 200\ C_a$
Surfacic Contamination C_s	$< 10\ C_s$	$10\ C_s << 100\ C_s$	$< 100\ C_s$

Table 31. ALARA classification criteria. (*) Equivalent Dose Rate; (**) Estimated Individual Dose for the intervention or sum of the individual doses for the same type of intervention per year when they are repeated; (***) Estimated Collective Dose for the intervention or sum of the collective doses for the same type of intervention per year when they are repeated; C_a, guideline value for specific airborne radioactivity: inhalation of air with a specific airborne contamination of C_a during 1 hour will lead to an effective dose of 10 μSv; C_s, guideline value of specific surface contamination: the specific surface contamination (in Bq/cm^2) which, according to model calculations, may expose a worker by ingestion or inhalation to an effective dose of 0.5 mSv per year or 0.25 μSv/h.

- Surface contamination

The thresholds for risk level 1, 2, or 3 for each criterion are shown in Table 31. The entire IBL installation will be classified by the highest risk level of any single individual criterion. In case of level 3 classification, the RSO, the GLIMOS and the project leader must petition for approval from the CERN ALARA committee chaired by the LHC *Chef d'Installation*.

7.6.4 Material handling

Shielding must be designed to protect personal during their activities on the minivans on side A and on side C. Shielding is expected to be particularly effective for the VA beam pipe sections, the LAr Endcap Calorimeter, and around the pixel services. A shielded carrier for the extracted Ph0 beam pipe has been already discussed.

The beam pipe sections VI and VA, their associated services and supports, the entire ID, and part of the pixel services lie in the ATLAS "radioactive waste area". Manipulation of any material in this area must follow controlled procedures [92]. The CERN RP group assisted by the ATLAS RPE/RPA must be involved in all relevant steps of the beam pipe removal procedure. In-situ dose rate measurements, and when required contamination measurements, must be performed. After removal, the VI and VA beam pipe sections will be stored in a shielded box compatible with the insertion/ extraction table. This box can then be stored in a radioactive buffer zone in SX1 building. All material for storage or disposal must follow this procedure. The CERN Radioprotection group will take responsibility for disposal of material from the SX1 Buffer zone.

8. Commissioning Plan

This chapter covers the commissioning plan for the IBL in the ATLAS cavern. It comprises the commissioning of the cooling system when the IBL has been connected to it, the initial calibration studies to tune and understand the IBL performance in-situ, and early data-taking with random triggers, charge injection and cosmic rays.

Functionality and performance tests of the IBL will be done during its integration on the surface (ATLAS SR1 building), including cold operation with temporary services and cooling, as described in Section 5.10. During the connection of the detector to its final optical, electrical and cooling services in the pit, quick tests will also be performed to check the correct connections and functioning, in analogy to the tests performed for the present Pixel detector [93].

Based on the commissioning experience with the present Pixel detector [94], the following sections describe the procedures to measure the in-situ performance of the IBL detector before its operation with the rest of ATLAS. Tests carried out during integration and installation are also mentioned simply to give relevance to the new measurements that need to be performed in the commissioning period.

The chapter also describes the commissioning of the IBL as a new part of the Pixel detector, when the behaviour of the full system, IBL together with the present Pixel detector, will be checked. Furthermore, it will be verified whether the performance of the present Pixel detector is affected by the integration with the IBL.

8.1 Commissioning of Cooling

The commissioning of the IBL and its cooling system is divided in a few major steps:

- Qualification of the IBL thermal properties on the surface. This test was not possible for the present Pixel detector, but it is desirable for the IBL.
- Qualification of the cooling services standalone: this phase can be staged and some parts of the system can be qualified before the installation of the IBL.
- Connection of services at PP1 and subsequent leakage test to verify that connections are tight.
- Preliminary test of the cooling performance of each individual loop before the ID end plate (IDEP) closure (with temporary sealing).
- Final test of the thermal performance of the full system, IBL and present Pixel detector together, for default and end-of-life conditions.

This section covers the last item of the list above; in particular it describes the commissioning of the cooling system to assure the safety of the detector and the in-situ measurements of the thermal performance of the full system. The other items have already been described in the Integration and Installation chapters.

Detector safety

One of the most crucial tasks of the commissioning period is to verify that the detector goes to a safe state at all times when the cooling systems stops, in order to prevent overheating of the detector or its services. Ultimately the safety is assured by hardware interlocks such that if a module exceeds a maximum temperature limit (40 °C in the present detector services), its power supplies receive an interlock signal which switches them off. A similar precaution is implemented in the PP2 stations, where a temperature higher than 60 °C in the sensors on the crates causes a hardware interlock to the input power supplies. However more sophisticated safety procedures are implemented to avoid such extreme conditions. Furthermore, it is important to reduce the number of thermal cycles and to control their amplitude and speed, as past experience has shown that failures are often correlated with them.

As an additional protection layer, alarms in ATLAS are organised and propagated to the sub-detectors by the Detector Safety System (DSS). In case an alarm is generated from the cooling systems, electrical power, smoke detectors, cable or rack cooling, etc. a hardware signal is generated. DSS sends that signal to the concerned sub-detectors and safety actions are taken in due time in order to assure the safety of the sub-detectors. The correct propagation of the DSS alarm signals can be tested by artificially generating a fake signal and verifying that it is received by the Interlock Logic Unit of the IBL and correct actions are applied.

A software safety layer is also implemented that guarantees more flexibility with respect to the hardware implementation. In particular, a so-called cooling script is always running in the PVSS projects. It can switch off parts of the detector according to conditions in the Pixel detector (e.g. too high module temperature, but lower than the hardware interlock temperature setting) or in the cooling system (e.g. the state of the plant or of an individual cooling loop). The finalisation of the cooling script for the present Pixel detector has needed time and iterations in order to optimise the switch on/off procedures and minimise the amplitude of the unavoidable thermal cycles. The implementation should exploit the experience gained with the present Pixel detector.

Thermal performance

NTC sensors located on the modules will allow the thermal performance of the IBL to be checked. During the commissioning period it has to be demonstrated that the cooling system can dissipate the power produced by the detector and keep the modules in the desired thermal condition, both in nominal conditions and at the detector end-of-life. The module temperature and the module thermal figure of merit (i.e. the difference between the module and the coolant temperature over the module power) are the parameters to be monitored with respect to cooling system settings, module position along the local support, and module power. Figures 126-128 illustrate some parameters that were monitored during the commissioning of the present Pixel detector [95] to study its thermal performance. In a longer term study it will also be important to check that the thermal coupling between the electronics and the local support ensured by the glue between them does not degrade with time.

While the module temperatures are obviously the most interesting quantities to be checked for the detector, the temperature inside the Pixel package also has to be carefully monitored through the environmental sensors that are already installed in the services panels and the ones that will be installed with the IBL. Figure 129 illustrates the temperature condition inside the current Pixel package during commissioning in 2008.

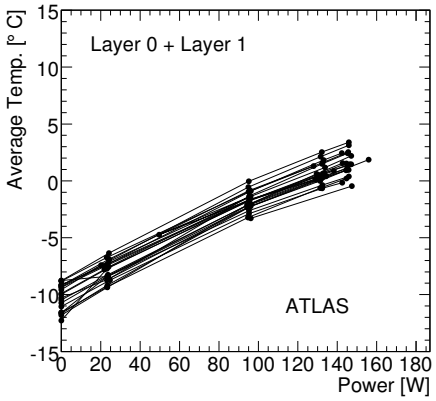
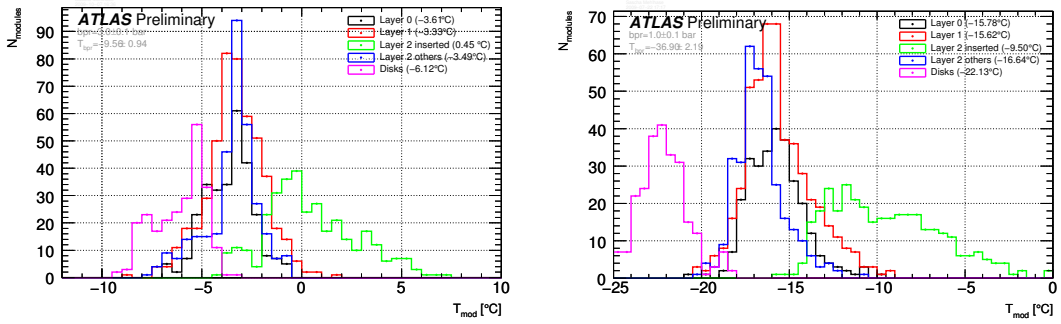


Figure 126. Average module temperature vs total module power for Layer 0 and Layer 1 bistaves (26 modules).

8.2 Calibration Suite for Commissioning

This section describes in a general way the calibration procedures for the Pixel detector including optolinks, front-end electronics, sensors and modules. The measurements described here are of two different types: the first type, referred to in the following as tunings, serves to determine and establish the best operational settings of the Pixel detector. The second type, referred to as calibrations, measures the properties of the detector and its electronics, either to check the performance of the tunings or to assess other interesting parameters. Of course, they also include the very basic tests to check the functionality of the detector components, such as opto-boards, modules and front-end electronics whose failures are the main source of inefficiency in the present Pixel detector. The results of the calibrations are then either used for the offline reconstruction or for a time (and radiation) dependent monitoring of the detector behaviour.

The IBL detector will have been qualified during its integration and system tests in SR1;



(a) Cooling system back pressure 3 bara and nominal power consumption ≈3.7 W per module

(b) Cooling system back pressure of 1 bara and maximum power consumption ≈5.3 W per module (end of life conditions)

Figure 127. Module temperature distributions for the parts of the present Pixel detector.

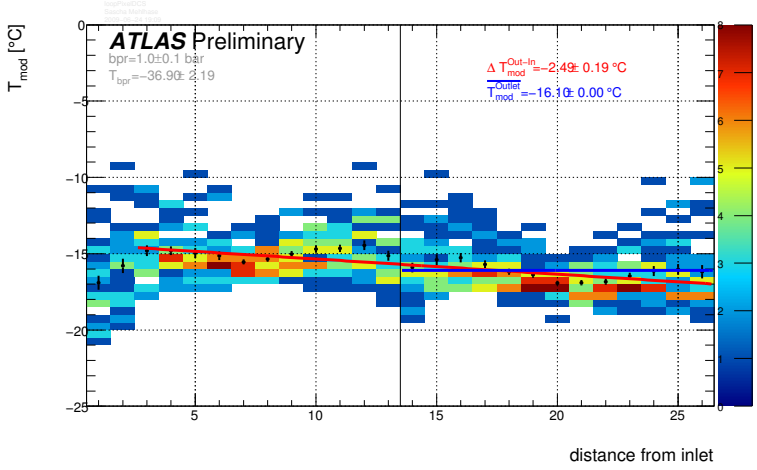


Figure 128. Average module temperature vs distance from inlet for Layer 1 and Layer 0 at cooling system back pressure 1 bara and maximum power consumption ≈5.3 W per module.

however during the commissioning in the pit, it will be important to finalise the tunings in the final environment and to measure the properties of the detector after insertion. It will also be important to check that the properties of the present detector are not being affected by the insertion or the presence of the new layer. The calibration scans will therefore involve the full Pixel detector.

Examples are given using the present Pixel detector, assuming that, even if the IBL on-detector and off-detector electronics are different, the tuning and calibration procedures will be similar.

8.2.1 Optical links and communication basic functionality

The data transmission between the detector and the counting room is achieved via optical links as described in Section 6.3. Therefore the calibration of the optical transmission parameters (optolink tuning) is the very first step in the overall calibration procedure. As the data transmission depends

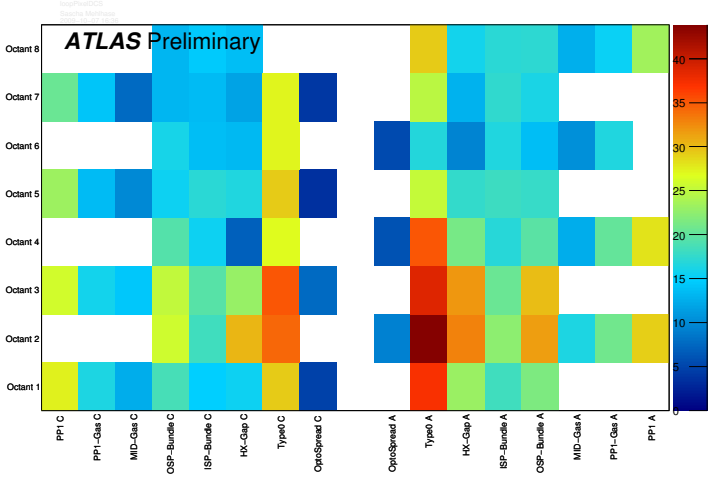


Figure 129. Average temperatures measured by sensors at PP1, the SQP bundles as well as at PP0 during a phase of stable running.

on both the fiber and the on-detector electrical services, the optolink tuning is specific to the pit commissioning and can not inherit settings from previous tests performed in SR1 with temporary fibers.

The optical links consist of TTC-links, which are used to send clock and command signals to the Pixel detector and data-links, to send data from the front-end chips to the readout crates. The typical procedure starts with basic functionality measurements, verifying the connection of the links and measuring the transmitted laser power, followed by the parameter tuning first of the TTC-link and then of the data-link. Finally, the correct tuning of the optical links is validated by doing several digital injections into the front-end chips and reading out the resulting hits.

- **Functionality measurements**
  Fiber integrity is verified during the services installation using an Optical Time Domain Reflectometer (OTDR) that checks light propagation along the fibers. After fiber connection to the detector, a measurement of the transmitted laser power for TTC and data-links can be obtained by measuring the currents of the PiN-diodes at the receiving ends. The power transmitted over the TTC-link is measured by sending a clock-pattern from the BOC-cards to the on-detector opto-boards. The detector control system is used to read the resulting current in the on-detector PiN-diode arrays, which measures the light power at the detector end. Vice versa, to measure the laser power of the on-detector lasers the on-detector chips are configured to send a loop-back clock signal on the data line to the readout crates. The current in the receiving off-detector PiN-diode arrays is read, measuring the light power at the BOC end.

- **TTC-link tuning**
  Clock and commands are sent on one line for two front-end chips on a Bi-Phase Mark encoded (BPM) stream. The BOC parameters of the TTC-links that have to be tuned are the BPM fine delay and the mark-to-space ratio (MSR). The fine delay of the BPM stream is used to account for the different fiber and cable lengths and to synchronise the clocks of each single module with the LHC bunch crossing clock. The BPM fine delay has been calculated and programmed in the BPM chips based on the different cable lengths for the individual modules. A further refinement of the fine delay settings is possible using collision data. The MSR defines the duty cycle of the clock which is reconstructed on the on-detector opto-boards. Ideally this duty cycle is 50%. A calibration scan has been developed to examine the reconstructed clock and choose the optimal value for the MSR. The laser power in the BOC is also an adjustable parameter but it is kept at its default value for the time being.

- **Data-link tuning**
  The transmission parameters that need adjustment are the sampling phase and threshold at the receiving end, and the laser power on the opto-boards. The Module Controller Chip (MCC) of the present detector is able to send either a half-clock stream or an event-like data stream. These data streams are checked in the BOCs for matching with the expected bit pattern. The bit-error-rate (BER) allows the error-free transmission range of the adjustable parameters to be accessed. A similar data streaming from the IBL on-detector electronics to the readout crates will be exploited to check data transmission. Figure 130 shows for the present Pixel

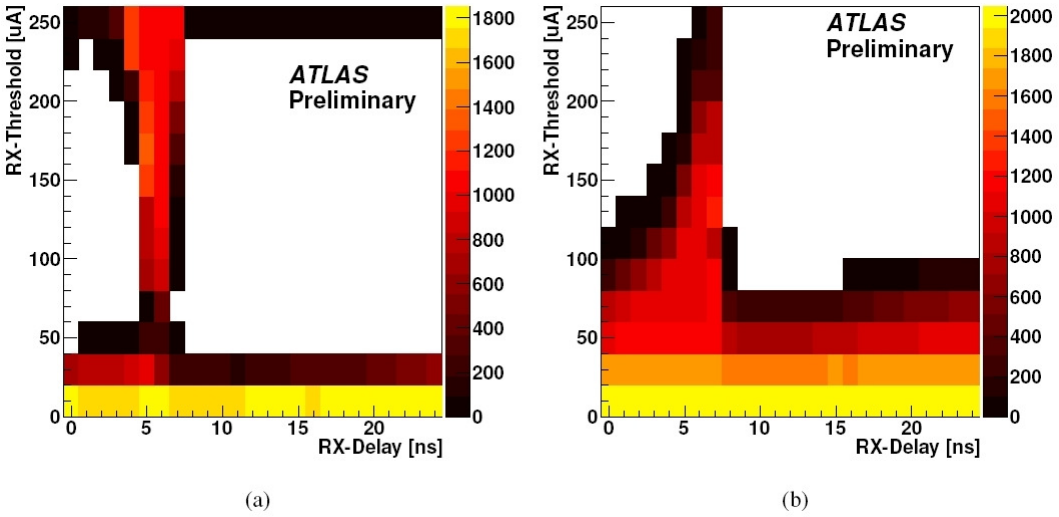


Figure 130. BOC scan in the present Pixel detector with (a) too low and (b) adequate laser power.

detector the result of a two-dimensional BOC-scan, in which the sampling threshold and the sampling phase have been varied. The colour scale encodes the number of bit errors, white meaning no error. In Fig. 130 (a), with (too) low light-power, one can see three different error regions: a vertical band, i.e. an error region independent of the threshold, which is caused by a sampling time during the data transition, an error region at too high thresholds, where 1 s are no longer correctly decoded, and an error region at too low thresholds, where the threshold is in the noise floor and 0 s are erroneously identified as 1 s. In Fig. 130 (b) the laser power has been increased, such that the upper error band is no longer within the range of accessible thresholds.

8.2.2 Detector electronics tuning and calibration

The main tuning and calibration of the detector electronics concern the threshold and the Time Over Threshold (ToT) that can be tuned on both a chip-by-chip and on a single-pixel basis. The IBL should be tuned after its integration, during the SR1 system tests. However a refinement of the tuning parameters after the insertion in ATLAS can be foreseen as the environment conditions will be different.

One of the most fundamental parameters of the pixel cell is the discriminator threshold, i.e. the charge above which a signal is considered a hit and passed on to the digital readout part. The threshold has to be low enough to allow an efficient hit detection, but high enough to suppress noise. The tuning procedure consists of adjusting first the chip-level DAC and then the individual pixel DACs that are devoted to change the discriminator threshold. The Pixel detector operated in 2008 and 2009 with the threshold set to 4000 e^- and a threshold spread of 40 e^- over the full detector (Fig. 131). This setting corresponds to a ratio of threshold over noise for normal pixels of 25 (Fig. 132) which guarantees a very low noise level in data-taking. It is also possible to operate the detector at a lower threshold such as $\approx$ 3000 e^-; however the noise increases and the tuning procedure becomes less automatic.

The ATLAS Pixel front-end electronics also offers the possibility of measuring the analogue pulse height, and thereby the charge deposited by particles, because the duration of the discriminator output pulse (ToT) depends nearly linearly on the amplitude of the preamplifier signal. The ToT information is stored together with the hit data in units of the bunch-crossing clock (25 ns). The ToT tuning procedure consists of adjusting first at the chip-level and then at the pixel-level DACs that are devoted to changing the shape of the discriminator output pulse in order to obtain a uniform response for a target injected charge (that is usually chosen to be the most probable charge released by a MIP crossing the detector at normal incidence). The dependence between the deposited charge and the ToT is then obtained from a calibration measurement using charge injections over a large range. The absolute scale of the ToT has to be chosen carefully because too short pulses would decrease the ToT resolution, whereas too long pulses (close to or longer than the trigger latency) would lead to hit losses. The ToT distribution obtained from analogue injections with a charge of 20000 e^- is shown in Fig. 133; it is centred close to the currently used target value of 30 BC and has a very small width of 0.7 BC. As the ToT tuning slightly affects the threshold, it is usually followed by a retuning of the threshold DACs.

The timing adjustment is also part of the calibration procedure and it follows the previously described tunings as it depends on them. The aim of this tuning is to limit the readout of any given triggered event in a single bunch crossing (25 ns) in order to reduce the pile-up. This requirement becomes even more important for the IBL where the occupancy will be higher than in the present Pixel detector. In order to reach the required hit detection efficiency in one BC, the optimisation of timing delays and phases is therefore crucial to achieve the best possible synchronisation within the Pixel detector. The calibration measurements use charge injections with varying charge and varying delays in the readout electronics. The exact calibration procedure to achieve the best syn-

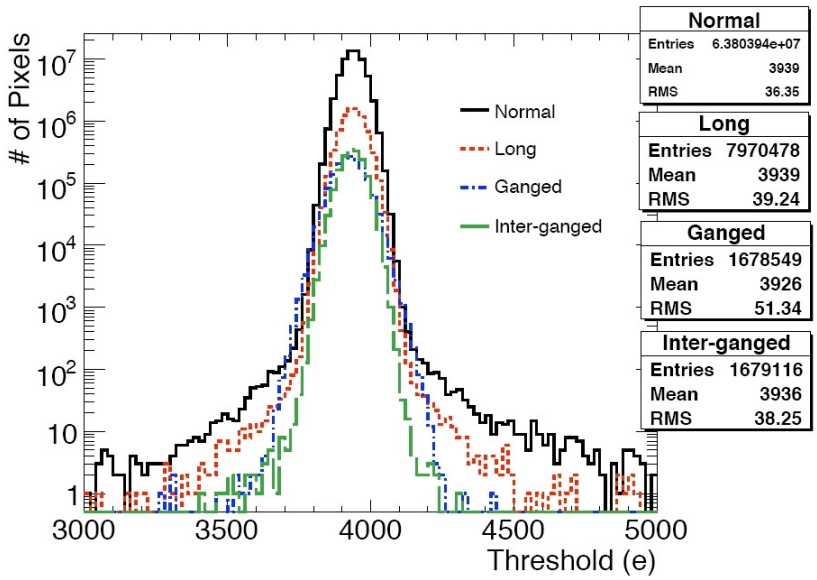


Figure 131. Threshold distributions for normal, long, ganged, and inter-ganged pixels during 2008 operation of the present Pixel detector.

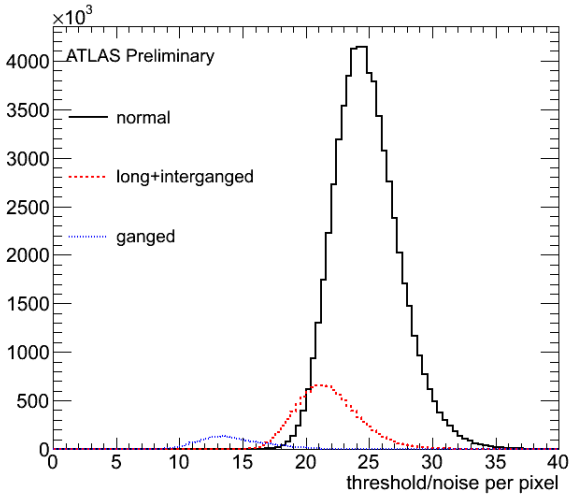


Figure 132. Threshold over noise distributions for normal, long, ganged, and inter-ganged pixels of the present Pixel detector during operation in 2008.

chronisation will be developed at a later stage when the FE-I4 electronics will be available. It will be different from the current one as some of the functionalities that are in the MCC will be moved to the Front-End readout.

Once the timing is optimised through the available parameters, including the optical ones described in Section 6.3, the timing performance is still be limited by the time-walk, i.e. the time needed by the released charge to cross a given threshold. As the preamplifier pulse for a low charge

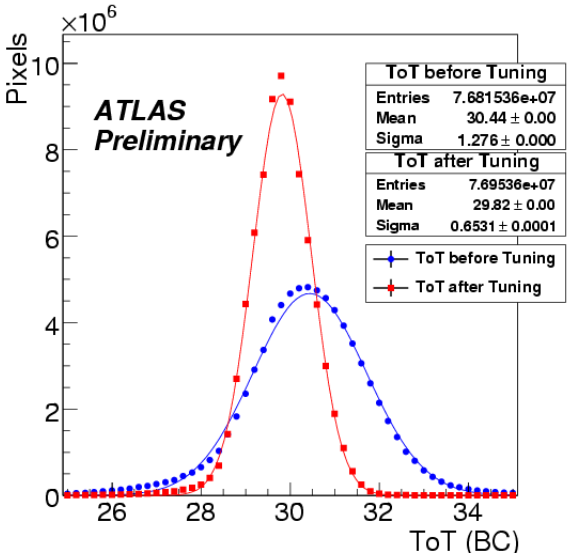


Figure 133. ToT distribution for the present Pixel detector with an injected charge of 20000 e^- with tuning performed during module production and the 2008 tuning after installation. After tuning, the mean value is about 30 BC with a spread of 0.7 BC.

deposition crosses this threshold later than the pulse for higher charge deposition, the time-walk can generate an inefficiency in detecting low charge deposits. For operation at the LHC, what is important is the measurement of the charge for which the delay is larger than 20 ns with respect to the delay for high charge releases, usually 100 ke^-, because these low charge deposits could be lost once the readout is set to a single bunch crossing readout mode.

8.2.3 Sensor and hybridisation characterisation

As part of the calibration procedure, measurements of sensor properties and bump connectivity will certainly be done in the SR1 system tests. However, after installation, a calibration will be repeated in order to check that no damage has been provoked by the mechanical actions on the detector and also to have a first reference of the IBL conditions to be monitored, in time and versus radiation, periodically.

- **Leakage current**
  The current can be measured both at the module level and at the pixel level. The measurement of the leakage current is important for two different aspects: firstly, since it is a direct function of the fluence, it can serve as a monitor of the radiation damage suffered by the sensors; secondly, a measurement of current versus bias-voltage can give information about the breakdown voltage and therefore the maximum operation voltage of the sensor. In the current ATLAS Pixel detector, two different possibilities for measuring the reverse-bias current are available. A first method uses the detector control system to measure the current of a single high voltage channel, with the drawback that since it is connected to six or seven modules, the measured current is the sum over many modules[5]. A second method uses the pixel front-end electronics to measure the leakage current of a single sensor pixel. However this method is very time consuming and it is not optimised for non-irradiated devices.

- **Depletion voltage**
  An important property of the sensors is the voltage needed for full depletion (depletion voltage). In the case of the ATLAS Pixel sensors, before type inversion of the silicon bulk, the n-in-n sensors deplete from the backplane and full depletion is necessary for successful operation of the detector. After type inversion, the depletion region starts to grow from the pixel implant side and in principle the detectors could also be operated only partially depleted. The standard way of measuring the depletion voltage after type inversion will require a study of the cluster size and charge collection of inclined tracks. Calibration measurements for non-irradiated devices have been optimised to measure the depletion voltage before type inversion. They are based on the measurement of the pixel capacitance that changes when full depletion is reached: they either measure the capacitive cross-coupling (cross talk) between neighbouring pixels or the noise in data-taking, which depends on the capacitive load to the preamplifier. Results for the present detector obtained with the crosstalk method during 2008 operation are shown in Fig. 134. As expected, the voltage required to fully deplete the sensor thickness is 50-60 V.

[5]The installation of more power supplies and the capability of reading the current at module level are foreseen with the higher luminosity in the coming years, so that the individual module current can be monitored.

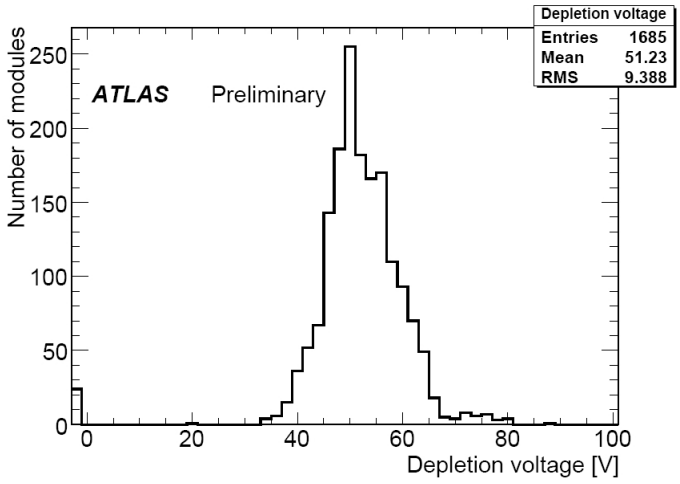


Figure 134. Depletion voltages determined with the crosstalk method for all scanned modules of the present Pixel detector during operation in 2008.

- **Bump connectivity**
  The bump connectivity between sensor and electronics pixel cells is constantly monitored during the module hybridisation and detector integration. It can happen that due to mechanical forces induced by handling or thermal cycles, connections are worsened. Monitoring of the bump connectivity is also important after installation in the ATLAS detector to be sure that no degradation is on-going. The bump connectivity of a pixel is qualified through a measurement of its noise and of the crosstalk with neighbouring pixels. Based on these calibrations, the estimated fraction of disconnected pixels for the present Pixel detector is 0.1%, in 2008. The fraction of disconnected bump bonds per module is shown in Fig. 135.

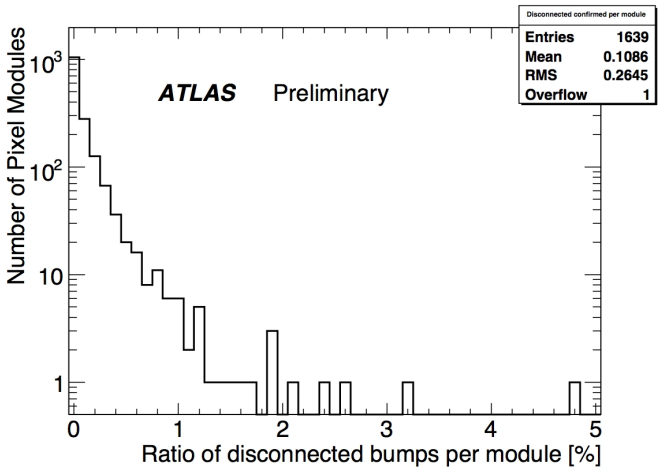
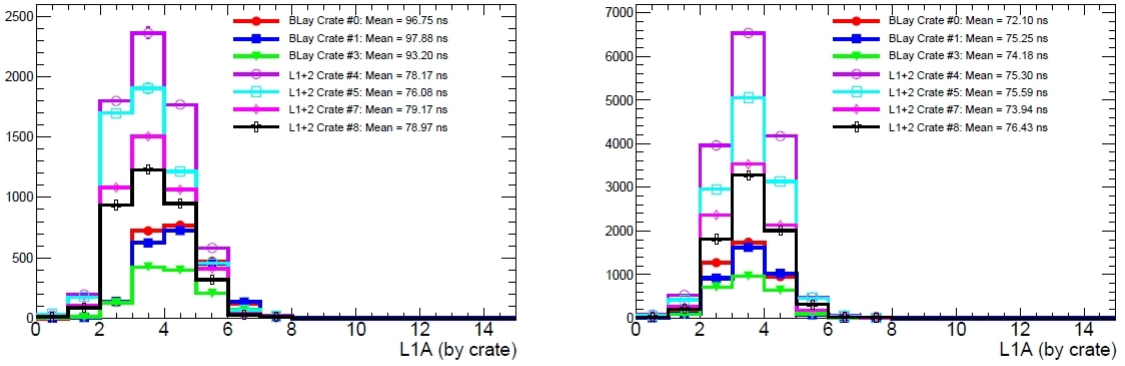


Figure 135. Fraction of disconnected bump bonds per module measured for the current Pixel detector in 2008. On average, about 0.1% of the bump bonds are disconnected per module.



(a) Read-out crate timing before adjustment (Run 91338) (b) Read-out crate timing after adjustment (Run 92057)

Figure 136. Mean relative bunch crossing (L1A) timing in 25 ns bunch crossing units for clusters on tracks corresponding to each one of the nine read-out crate. Clear shifts between crates in earlier runs suggested signal propagation delays that were later corrected.

8.3 Data-taking plan for Initial Alignment and Readiness Validation

The commissioning procedure before the operation with LHC beam is completed by data-taking, first using random triggers and then cosmic rays.

- **Data-taking with random triggers**
  Data-taking with random triggers is extremely useful as it tests the data flow through the complete read-out chain. In particular it can check the complete integration between the present Pixel detector and the IBL readout services and software. It is also important to stress that these kind of tests can be performed out of the global ATLAS partition as there is no need for any physical trigger source or for the Central Trigger Processor (CTP). Therefore the tests can be performed at any stage, even when ATLAS is running in a different status.

  Data-taking with random triggers might be used to measure the noise occupancy[6] and, if needed, to compute pixel masks to be applied online so as not to cause the read-out system to go in a busy state. Moving towards high trigger rates is also one of the standard commissioning tests. It stresses the read-out system and can spot unexpected problems.

- **Cosmic ray data-taking**
  The main aim of the cosmic ray data-taking is to prove the full compatibility of the new IBL detector with ATLAS combined data-taking, and to improve the knowledge of the position of the IBL detector with respect to the rest of ATLAS after installation. Since the active volume of the IBL is extremely small, cosmic ray rates of O(100 mHz) can be expected. The relative position of the IBL modules will be known precisely thanks to surveys done during the integration and installation phases, but their absolute position will have to be carefully measured once the detector is in its final position and at the operating conditions. Even with a

[6]During operation the noise occupancy is computed using devoted data stream in which the tracks occupancy is negligible.

reduced number of tracks, it will be possible to align the IBL volume to the ID sub-detectors. However, tracks from interactions will be needed to reach an alignment precision close to the other parts of the Pixel detector. Depending on how long the cosmic ray data-taking lasts, some other physical measurements could be obtained. With a sufficient number of tracks, timing studies will be possible, for instance to compute the readout crate delays. Figure 136 shows what was achievable with the current Pixel detector at crate level with reduced statistics in 2008 operation. Increasing the number of tracks will make possible studies of charge, cluster properties and the Lorentz angle.

9. Prototyping, Production Testing, System Testing and QA/QC Infrastructure

The first part of the chapter details the prototyping activities intended to developing the core parts of the IBL detector: the modules and the staves. Module and stave qualification programs are carried out to demonstrate their performance, suitability for the IBL, and readiness for production. The second part of the chapter is dedicated to an overview of the irradiation, test beam and system test activities planned in the IBL project.

9.1 Prototyping and Qualification of Modules and Staves

A dedicated module qualification program aims at constructing full IBL modules with three different sensor types: planar silicon, 3D silicon and poly-crystalline CVD diamond. The goal of the program is to demonstrate the functionality of the FE-I4 chip in combination with those sensor types, to qualify their radiation harness, and to evaluate their performance in test beams. Additionally, the module qualification program yields critical information about the manufacturing of IBL modules, the bump-bonding of thinned chips to sensors, and the production readiness for the different sensor types. Based on the results of the module qualification program and the sensor R&D, a decision on the sensor type used for the IBL will be taken.

The stave qualification program aims at developing carbon fibre staves with adequate mechanical and thermal performance. It is based on the mechanical and thermal evaluation of different stave designs and cooling pipes, with the goal to maximise mechanical stability, cooling efficiency of modules and minimising material. In parallel, manufacturing process for staves, cooling pipes, welding of pipes and fittings are qualified for production. The final step of the stave qualification will be the *stave-0* program during which two or more fully assembled staves are prepared with modules provided by the module qualification program. This allows to qualify the module loading procedure and test complete staves loaded with modules for an extended period of time in a system test together with off-detector components.

Table 32 gives an overview of the prototyping steps on modules and staves, which are explained hereafter.

9.1.1 Module qualification program

The purpose of the IBL module qualification program is to demonstrate the viability of the module design for IBL. This is in particular the validation of the newly developed FE-I4 chip bump-bonded to sensors of the three different technologies. For the chip, this means in particular the digital functionality, outlined in Section 3.3, the new control and data output, the powering options and the analog performance (noise, threshold dispersion, minimal threshold, gain).

The sensor technologies differ significantly in leakage current, input capacitance and signal. Results of tests carried out with FE-I4 chips with the different sensors types and the FE-I4 chip will give input to the choice for the production sensor. The tests include before- and after-irradiation comparisons, lab measurements (e.g. with γ-sources) and test beam measurements.

The second, important purpose of the IBL module qualification program is the demonstration of the production viability of IBL modules. Constructing a significant number of qualification modules allows to assess sensor and module production yields, quality (e.g. number of dead or disconnected channels, and their uniformity in terms of basic sensor parameters (leakage current,

Module

1. Prototype production of different sensor technologies & FE-I4 version 1 engineering run, followed by wafer tests and single chip tests.
2. Bump-bonding of FE-I4 chips with conservative thickness to different sensor types. Evaluation of single-chip assemblies in lab measurements, calibration, source tests and test beams. Comparative tests of irradiated and non-irradiated chip-sensor assemblies.
3. Bump-bonding tests with thinned chips (target thickness $\approx 100\mu$m) to demonstrate bump-bonding quality with thinned chips.
4. Bump-bonding and test of thin FE-I4 chips to sensors and assembly with module flex circuit for final IBL modules. Evaluation of modules in lab measurements, irradiation and test beam.

Bare stave

1. Qualification of cooling pipe in pressure and leak tests.
2. Qualification of cooling pipe welding techniques and transitions & design and qualification of PP1 fittings of cooling pipes.
3. Measurement of heat transfer coefficient for different coolants and cooling pipes.
4. Production of prototype CF staves with carbon foam and different diameter cooling pipes. Thermal tests of prototype staves with heaters to measure thermal figure of merit of stave. Comparison to FEA results on thermal performance.
5. FEA and measurement of mechanical deformation of prototype staves at different operation temperatures.
6. Irradiation and thermal cycling of prototype staves, pipes and connections.

"Stave-0"

1. Trial loading of stave prototypes with dummy modules to optimize module to stave contact, mechanical positioning of modules and module handling. Development and qualification of module loading tools.
2. Loading of modules from Module Qualification Program to final prototype staves. Qualification of mechanical positioning. Evaluation of module function before and after loading.
3. Thermal and electrical tests of staves in integration mockup in SR1.
4. System tests of staves with off-detector components (DAQ, DCS, power supply system).

Table 32. Overview of planned IBL prototyping steps for modules and staves.

signal collection). The FE-I4 chip is the largest chip to date in HEP, so another important aspect of the qualification program is the development and demonstration of reliable bump-bonding for thinned chips of this surface.

From the engineering run of FE-I4-V1, approximately 300 good FE-I4 chips are expected out of 16 wafers. However 6 wafers may be kept partially processed (metal mask changes), not thinned or not bump-bonded or be used for bump-bonding qualification. For this reasons not more than approximately 160 chips are to be used in the module qualification program and single chip tests.

For the module qualification program, up to 60 FE-I4s are expected to be used for single-chip and double-chip modules with planar sensors, 60 FE-I4s for modules with single-chip 3D sensors and 40 FE-I4s for modules with single-chip CVD diamond sensors. Table 33 gives an overview of modules to be constructed with different sensor types. Approximately 50% of modules will be

Module Type	Sensor Type and Layout	Manufacturer	Number of Modules
3D	2E active edge	A	total
	2E active edge	B	60 single chip
	2E active edge	C	
Planar	n-n	D	total
	n-n slim edge	D	60 single chip
	thin n-p	E	plus 30 double chip
Diamond	pCVD	F	total 20 single
	pCVD	G	or double chip

Table 33. Overview of planned IBL qualification modules. The table gives the preliminary number of modules that will be constructed with different sensor types, from different vendors (called A, B, C, etc.), and the number of modules.

made to final IBL specifications (i.e. thinned chips and module flex), hence giving a reasonable estimate for production yield and module construction reproducibility; the other half will be used for initial tests with sensors and for chip qualification. The sequence of qualification will be measurements in the lab (chip analog and digital tests, tuning of thresholds, power and source tests), followed by irradiation of some modules and test beam studies of selected modules, to measure efficiency, signal response uniformity, spatial resolution and sensitivity along sensor edges.

The first qualification modules are expected during second half of 2010 for lab-measurements. A sub-set of them will be used for irradiation and test beam studies. Results of those measurements, expected during the first half of 2011, and production experience with qualification modules will allow choosing the sensor technology and the final FE-I4 design to be used for IBL module production. In addition to the electrical performance of the modules, criterii like production consistency, reliability, long-term experience and possible gains for engineering/system simplification need to be take into account for this decision.

9.1.2 Stave prototyping program

The stave prototyping program aims at developing staves as light-weighted local support for modules, with good thermal conductivity for module cooling, and showing small deformation (see Section 4.2).

The prototyping of the staves focuses on three areas: i) the cooling pipe, ii) the joints between pipes (Ti welds and CF/Ti transitions), and iii) different stave designs (number of pipes and pipe cross sections). A detailed overview and test specification for stave components and completed staves, without modules, have beeb given in Section 4.2. As the IBL detector has relatively few staves, the current plan foresees qualifying 100% of all staves in all tests, excluding destructive tests and irradiation tests.

Titanium pipes with an ID of $\approx$2 mm are considered the baseline cooling tubes for the IBL. In parallel, carbon fibre pipes are also being developed and qualified because they show advantages in terms of material budget and CTE. However, this development is considered more appropriate for applications at HL-LHC than for the timescale of the IBL. Pipes are qualified in pressure tests,

leak tests and thermal cycling: they are pressurized at 150 bar, which is 1.5 $\times$ the maximum design pressure for a CO_2 cooling system; the leak rate specification is 10^{-7} atm.cc/s; thermal cycles, in the range of -50°C to +30°C, are carried out while the pipes pressurized to detect leaks induced by the thermal stress.

As transitions between pipes, two types of transitions need to be qualified: welds and permanent Ti joints. They must also qualified on tests as above. In addition, burst tests, pull tests and microscopic analysis of sectioned samples will be carried out.

One particular test relevant for CF pipes and its transitions is the qualification against micro-cracks. Strain induced in the CF pipes can lead to micro-cracks and leaks. This can be increased by irradiation. Un-irradiated and irradiated samples of ply laminates (0/90/90/0) are submitted to pull tests in which the micro-crack density as function of the applied strain.

Titanium pipes and welds will be qualified by the CERN EN/MME-MM group in metallurgic analysis to relevant ISO standards (e.g. ISO 13919-1 for Ti welds). TID, electron beam and laser welding techniques will be investigated. The heat transfer between coolant and pipe is measured for Ti and CF pipes on pipe samples with C_3F_8 and CO_2 cooling system.

Completed local supports, i.e. assembled CF staves with cooling pipes, will be qualified in thermal qualification procedures. In those tests the different stave prototypes will be equipped with heaters instead of modules. The heaters will apply a controlled thermal load to the stave and the evaporation temperature set through the back-pressure. The temperature of the heaters will be measured. The staves are cooled either with a C_3F_8 or CO_2 cooling system. The main measurement is the measurement of the stave “thermal figure of merit", i.e. a measure of the stave thermal resistance as introduced in Section 4.2. This allows to cross-check the FEA calculations for the stave heat resistivity for all different stave designs. Table 34 lists a subset of different prototype staves that have been constructed to measure the thermal properties of the different designs. The stave configuration given in the first line is the IBL baseline.

The stave prototypes, some of them assembled with stave flex circuit prototypes, will also be subjected to thermal cycling tests and irradiated with neutrons up to doses of 300Mrad and 1Grad (see Section 9.2.1). We have carried out FEA studies to assess the deformations that can be expected as function of cooling temperature. To validate those simulations, we will measure the shape of the prototype staves as function on cooling temperature on a CMM.

	Pipe ID/OD [mm]	**Omega Thickness [μm]**	**Foam Density [g/cm^3]**	**X/Xo [%] Bare Stave with Coolant**	**X/Xo [%] Full Layer (+Mod +Flex)**
Ti 2 mm pipe, light foam	2.0 / 2.2	300	0.25	0.57	1.166
Ti 3 mm pipe, light foam	2.8 / 3.0	300	0.25	0.66	1.276
CF pipe, heavy foam	2.4 / 3.0	150	0.55	0.48	1.056
CF pipe, light foam	2.4 / 3.0	150	0.25	0.36	0.956

Table 34. Stave prototypes for thermal measurements.

9.1.3 Stave-0 qualification program

The goal of the “Stave-0" qualification program is to construct two or more fully functional IBL staves to its specification for mechanical, thermal and electrical performance. This qualification program is expected to be a major activity during 2011 to gain experience and validate the procedure for module loading, and to test completed staves thermally and electrically. The staves will be mounted in the integration mock-up (see Section 5.6) in SR1 for thermal and electrical tests.

Beyond the performance tests to validate the IBL stave design, an important aspect of the stave-0 program will be the development of the off-detector system and IBL control and data acquisition system. The availability of fully functional staves early in the project allows to qualify the prototypes components for stave powering (LV, HV, patch panel, DCS, interlock) and DAQ (opto boards, BOC, ROD). The setup will also be used as development platform for firmware and software needed in the IBL control and DAQ. The present Pixel system is replicated in SR1 already. Installing a full functional “slice" of the IBL system will also help to integrate the IBL to the existing Pixel system, already at the development phase.

The stave-0 prototypes will be constructed from prototype location supports (CF stave with cooling pipes) and modules, which were constructed during the module qualification program. The necessary module loading will be done according to the specifications procedures foresee for the final staves (see Section 4.4). This allows to gain experience with and optimize the tools and train personnel. After modules are loaded, their electrical performance is validated (sensor leakage current, module analog and digital operation).

The stave-0 prototypes will be operated with the evaporative cooling systems, CO_2 as well as C_3F_8, which are installed in SR1. This allows to cross-check the module thermal performance as function of different cooling conditions. This test will also verify the integrity of the thermal contact between modules and staves and test the stave thermal figure of merit on final IBL staves. The mechanical precision of the module loading of 10μmand completed staves is verified in an CMM survey . During the construction of the stave-0 prototypes, precise record of the weights of all components used in its construction will be kept. The material and weight of all individual components, the total overall weight and the precise dimensions of all "as-produced" parts will allow the comparison of the radiation length of the as-built IBL stave with respect to the design value.

The electrical tests of the stave-0 prototypes focus on the multi-module operation. Overall stave tests, as described in Section 5.7, will be carried out to compare single-module tests with measurements after module loading (e.g., sensor leakage, analog and digital module performance, noise, thresholds in multi-module operation). Operating multiple modules simultaneously on the complete stave with the prototype stave flex, EoS cards and internal services allows to test for coherent effects (e.g. cross-talk between modules, deterioration of noise or minimal operation threshold). The stave-0 tests will also allow the qualification of the finally chosen chip and stave powering scheme and grounding, as mentioned in Section 3.3 and 6.1, with close to final components (stave, EoS, internal services).

9.2 Irradiation and Test Beam Programs

Components of the IBL inside the IST or near PP1 need to be qualified to radiation doses of 300

Detector component	Irradiation Type	Dose [Mrad] or Fluence [1MeV n_{eq}/cm^2]	Facility
Module			
Sensor	p	1, 3, 5 $\times 10^{15}$	CERN PS
	n	1, 3, 5 $\times 10^{15}$	TRIGA
	mix n + p	2.5 + 2.5 5 $\times 10^{15}$	
FE-I4	γ	50, 100, 200, 300 Mrad	
Module	p	1, 3, 5 $\times 10^{15}$	CERN PS
	n	1, 3, 5 $\times 10^{15}$	TRIGA
	mix n + p	2.5 + 2.5 5 $\times 10^{15}$	
Stave			
CF Pipe	n	5 $\times 10^{15}$	Milano
	γ	1000 Mrad	LBL
Omega	n	5 $\times 10^{15}$	Milano
Foam	γ	1000 Mrad	LBL
Stycast	γ	1000 Mrad	LBL
Epoxy	γ	1000 Mrad	LBL
Ti stave sample	n	5 $\times 10^{15}$	Milano
	p	5 $\times 10^{15}$	CERN PS
CF stave sample	n	5 $\times 10^{15}$	Milano
	p	5 $\times 10^{15}$	CERN PS

Table 35. Overview of planned irradiations for different IBL components. The table gives ionizing radiation doses in Mrad and non-ionizing radiation as fluences of 1 MeV neutron equivalent per cm^2. TRIGA refers to the TRIG reactor / Slovenia, CERN PS to the CERN Proton Synchrotron irradiation facilities.

Mrad or fluences of 5×10^{15} 1 MeV neutron equivalent per cm^2 non-ionizing energy loss. Un-irradiated and irradiated modules will be tested in beam tests to measure their performance as tracking detectors.

9.2.1 Irradiation of IBL components and assemblies

The different components used in the construction of the IBL will be qualified in a number of irradiation tests at different facilities. The specific tests that are carried out after irradiation to assess any possible deterioration of the components are described in the relevant chapters for modules, staves and off-detector components. Table 35 summarizes the planned irradiation for components and assemblies together with the dose/fluence, type of irradiation and facility where the irradiation will be carried out.

9.2.2 Testbeam

The goal of the IBL test beam effort is to test the tracking and signal performance of IBL modules. It initially focuses on the qualification modules with different sensor types, which are constructed during the module qualification program of 2010. Several modules with different sensor types are

tested simultaneously in beam tests, in order to be able to assess their performance under identical conditions. A particular focus is the test of modules which are irradiated to 5×10^{15} 1MeV n_{eq}/cm^2. The measurements to carry out on non-irradiated and irradiated modules include:

- Efficiency inside a pixel cell and at sensor edge,
- efficiency and spatial resolution as function of incident angle in the typical IBL angular range,
- signal as function of sensor bias voltage,
- signal to threshold comparison,
- time-walk and in-time efficiency studies with nominal and detector-tuned FE settings, and
- tests in magnetic field.

These studies require a reference telescope for track reconstruction. The EUDET telescope [7] comprises 6 layers of monolithic MIMOSA pixel sensors as reference system for tracking. It reaches a spatial resolution of around 3 μm. The telescope includes mechanics for the DUT to allow for translation and rotation, it also includes trigger logic and a DAQ PC. The DAQ system is C++ based and modular enough to allow inclusion of the FE-I4 readout. An effort to integrate the ATLAS Pixel TurboDAQ system with the EUDET DAQ has already started. Data from reference and FE-I4 are merged offline. The IBL beam time is requested together with the EUDET Telescope for beam lines SPS H6B and/or H8 and the electron test beam at DESY.

The IBL specific infrastructure for the test beam includes a FE-I4-compatible readout system for several modules, e.g. based on the USBPIX system. The operation of irradiated module in the test beam requires the detector cooling to reach $\approx$ -25°C to avoid thermal run-away and the enclosure of the modules in a moisture-free environment. The angle-depended measurements require the DUT to mounted on a rotation stage which can provide an angle scan in the typical range of -10° to +30° with respect to the sensor vertical in ϕ.

9.3 System Test Goals

The different components of the IBL package must be tested in certain stages. Testing during the prototyping and production is considered basic; but there are many components which need to work together, therefore testing components interacting with each other is madatorym as well as their integration in a big set-up very close to the final package in ATLAS SR1. Apart from the on-detector part containing the modules and their services up to PP1 and the cooling, many other (off-detector) components will be connected to this. One can separate them into a few groups:

- Powering and services
- Detector control and monitoring
- Detector readout

[7] Eudet telescope user information at http://www.eudet.org/e13/e21/e727/

For the powering and services issues, all the power supplies and the connections to the detector – cables, passive and active patch panels, and regulators – need to be integrated into a test bench. The powering scheme is to be evaluated and the characteristics of the devices (max. voltages / currents, voltage drops, switch on and switch off behaviour, regulation capabilities, ...) are to be tested and qualified using dummy loads instead of detector components first, and integrate the powering system into a more complete system later on.

The detector control and monitoring contains all the DCS hardware and software. The used sensors and readout cards need to be tested and calibrated. There are many single components in this area providing functionality for temperature, voltage, and current monitoring and for interlock safety. All this is first a single test bench for itself and should be increasingly extended with time. The steering and control software needs to be developed using the original hardware as a test bed. A certain overlap with the powering and services area is to be mentioned.

The readout of the detector is primarily not connected to the powering, servicing, and controlling of the detector itself. The connection for the data transmission, the optical link, is to be tested first to characterize the different components, as they are the optoboard, the fibers, and the off-detector optical interface boards. Beside testing the range of operation settings and the interplay of the different control parameters, the data transmission quality can only be tested using the full chain. The electronics in the counting room, the ROD and the optical interface board should be connected to modules to qualify their functionality. Since there will be a single chip or single module testing with USBPIX cards first, the final detector operation and multi-module testing should be done using a final or close to final readout system setup.

The system test setup will connect to the “Stave-0" prototypes during multi-module test. This test will provide results about the stave functioning as well as functioning of the overall off-detector system for powering and readout. During these tests the stave-0 prototypes is implemented in the IBL integration mock-up (see Section 5.6).

To be able to test the pure functionality of the ROD an electrical connection to the modules should be preferred. Afterwards, the whole chain is tested with the already qualified optical link included into the test setup.

The complete lab testing and calibrating of the modules must also work using the final readout system and a complete test chain is needed for this. This chain is to be used in beam tests as well to qualify the data taking functionality of the system.

Certainly the different components of all areas need to be investigated separately first and the integration should be done in meaningful steps. Furthermore, all these areas can and will be handled separately first, but need to be integrated into a bigger and closer to final test bench at a certain point. Also here, a meaningful integration of the different components is important.

9.4 Common Infrastructure

This section summarizes the general equipment needs for testing and QA, at different stages of IBL construction. Table 36 gives an overview of the equipment needed for the testing on various IBL components at different moments of construction with a reference to specification and description. The table focuses on common equipment needed throughout the project.

Detector Component	Measurement	Equipment
Module		
Sensor	IV/CV:	probe station with T-controlled jigs
FE-I4	wafer tests:	probestation and card, USBPIX system
	single chip test:	single chip test card, USBPIX system
Module	module tests:	USBPIX system
		climate chamber
		$\beta\gamma$ source test setup
Stave		
Bare stave and pipe	pull tests,	
	pressure tests,	
	leaktests:	He-leak check equipment
	deformation:	CMM
	thermal cycling:	climate chamber
	thermal figure of merit	Fluoro-carbon & CO_2 evap. systems
Stave with modules	single chip test:	USBPIX system
	multi-chip test:	eBOC system
		evaporative cooling
System & Beam tests		
	power tests:	DCS and interlock
		internal services
		temp. power cables
		LV, HV system
	readout tests:	eBOC system
		VME DAQ infrastructure
		ROD, TIM, LTP
	opto system:	BOC
		temp. test fibres
		opto powering
	stave operation:	cooling system (evap.)
		dry-air supply system
		environmental enclosure

Table 36. Common equipment needed during testing of IBL components.

9.5 IBL Maintenance and Repair

The IBL has the same system layout as the present Pixel detector and it will be operated as part of the existing system. In general, the same maintenance and repair considerations apply to the two systems, therefore only the significant differences between them are listed.

One aspect of the system design was to enhance the overall system reliability and serviceability. This means in particular to minimize the number of inaccessible components. The IBL detector package inside the IDEP contains only the detector modules and some humidity sensors as active

components. In particular all opto components have been removed from the detector package and placed outside of PP1. They are therefore accessible for maintenance during an ATLAS opening without accessing the detector or PP1 area. The heater system of the present Pixel and SCT evaporative cooling is also seen as a critical system part with the potential to disrupt operation. The choice of a CO_2 cooling system allows to design the cooling system without active components inside the detector, the ID endplate area or the muon system. This is expected to lead to a significant increase of reliability and availability of the IBL detector in operation.

The replacement of the beam pipe or access inside the detector system, e.g. to repair or replace staves, requires the removal of the beam pipe together with the IBL. The IBL and beam pipe support tube, i.e. the IST, will stay in place and can be used as support for the installation of a new beam pipe and/or detector. The deinstallation is the reverse procedure of the installation, as described before, starting with the steps of beam pipe and IBL installation. The removal of only the beam pipe, i.e. the IBL stays in place and connected, is impossible due to the envelops restrictions of beam pipe flange and inner IBL radius, as well as the very tight integration of services around the beam pipe.

The replacement of a single, or all staves, is considered significantly faster than in the present Pixel detector. The IBL is a single layer and staves are mounted directly around the beam pipe. Their services do not overlap in different layers. Hence dismounting of staves is considered simpler and faster because the detector is not integrated into halfshells and global supports, is not connected to layered services and has not opto panels inside, unlike the present Pixel system.

10. Critical Integration Issues

This chapter discusses integration issues that are considered critical for the IBL project, and are linked to either the final performance of the detectors (e.g. material), integration aspects of detector and beam pipe (e.g. bakeout) or operation (e.g. cooling or powering). Their technical implementation proposed has been discussed in more detail elsewhere in this document, while this chapter reviews and highlights the critical aspects of these four detector issues. Note also that two material options have been developed for the local cooling pipes. The two options are taken into account when discussing some of the integration requirements, and will finally allow to include the argumentation that has led to choosing Ti as material for these pipes.

10.1 Bake-out Requirements

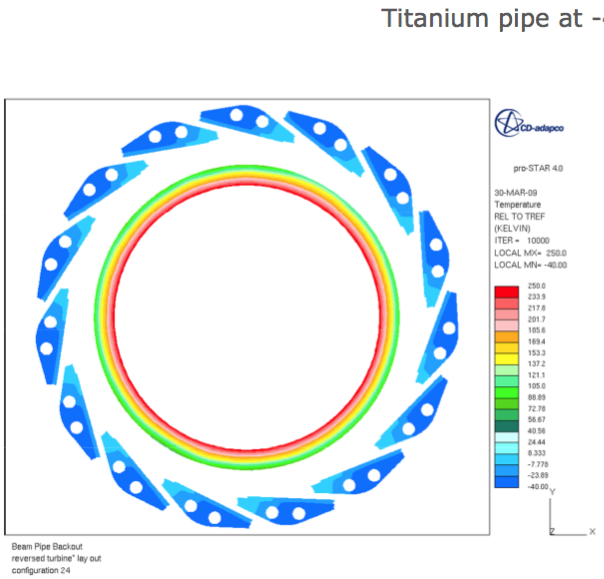
The control of the dynamic vacuum, i.e. the actual vacuum with beam circulating, is critical for the operation of ATLAS and LHC. Due to the high bunch intensities, residual entrapped gas can be released from the beam pipe walls causing pressure bumps. In the cold beam pipe regions (most of the machine), a beam screen is used to collect all residual contamination and give a vacuum better than 10^{-11} Torr. In ATLAS, the distance between ion pumps to remove residual gas is high, which leads to a poor pumping efficiency in the centre of ATLAS. In addition, the beryllium beam pipe section (VI) in the middle of ATLAS is coated with NEG (sputtered non-evaporable getter film), which traps residual gas. The NEG material must be activated to degas all entrapped gas, this is done by heating the beam pipe. This so-called 'bake-out' requires temperatures above 200 °C. After this, the NEG will have a very high pumping rate (leading to excellent vacuum also in the Interaction Points), but it saturates easily (the pumping rate goes way down after a single monolayer), so the system must be clean before the NEG activation. The bake-out is carried out with the IBL detector already installed around it. Hence the IBL detector system must be cooled during the bake-out process, so that the sensors, modules or staves do not exceed 40 °C. The IBL is cooled with its detector cooling system and all electronics are switched off.

The heating of the VI beam pipe is carried out through kapton heater foils, which will heat the pipe to 200-250 °C with a power dissipation of up to 200 W/m. The actual temperature and duration depends on the number of bake-out cycles. The numbers given here apply to the first cycle and the presently installed beam pipe. The beam pipe is wrapped in a thermal insulation foam and a shielding foil. The outer surface of the VI package, the foil, is expected to reach a temperature of up to 100 °C. The first successful bake-out of the present beam pipe has been carried out in July 2008. We currently assume the same bake-out procedure for the next, new beam pipe with the IBL installed around it.

During the bake-out it is critical that the detector cooling cools the staves to prevent excess temperatures on the IBL. In the present system, in case of a cooling failure the power supply to the beam pipe heaters are interlocked. The same mechanism will be implemented for the IBL.

The procedure for the beam pipe bake-out consists of the following steps:

1. Prebake-out tests. It is very difficult to calculate the thermal behaviour of the Pixel package under bake-out conditions; therefore a set of measurements at reduced VI temperature, where risks are small and controllable, will be carried out in order to extrapolate to the expected



	Tmax	Tmin
PIPE	-8.9°C	-40°C
FOAM	-2.6°C	-39.8°C
BUMP-BOUNDING	0.4°C	-19.5°C
FE-CHIP	0.4°C	-23°C
ADESIVE LAYER	0°C	-32.7°C
SENSOR	-0.3°C	-19.3°C
AIR-GEL	250°C	63°C
NIDROGEN	113°C	-39.5°C

Figure 137. FEA simulation of the temperature distribution in the IBL package, for a configuration with titanium cooling pipes and an evaporation temperature of the cooling system of -40 °C.

behaviour at full temperature. This will include measurements of basic time constants and ΔT of IBL staves relative to beam pipe temperatures. The tests will include turning off single IBL cooling loops and following the temperature evolution of the affected staves, as well as turing off the full detector cooling at reduced VI temperatures.

2. Bake-out Phase 1. The temperature of the beam pipe sections which are not NEG coated are brought up to 250-350 °C with a ramp rate of about 30 °C/hr, then kept at temperature for 22 hours, then ramped back down again. During this period, the NEG-coated parts are kept at about 130 °C.

3. Bake-out Phase 2. The temperatures of the NEG parts are brought up to 200-220 °C. The ramp rate is about 50 °C per hour, and the time at full temperature is again about 22 hours.

4. Bake-out Phase 3. The complete beam pipe cools down for a fraction of a day, and final vacuum quality measurements are done.

While there is experience with the bake-out process with the present Pixel system and beam pipe, the actual temperatures on the new package are driven by the IBL geometry and the new beam pipe specifications. To obtain a first overview of the temperature distribution and the thermal load on modules and sensors, the influence of convection and radiation have been assessed in a thermal FEA simulation. The results presented here are based on a layout with 15 staves, a sensor radius of 37 mm and absence of IST. The study is constantly updated with the most recent baseline IBL geometry. Figure 137 shows the temperature distribution for a configuration with titanium cooling pipes and an evaporation temperature of the cooling system of -40 °C. The simulation yields a maximum sensor temperature of -0.3 °C, that is well below the engineering limit of 40 °C and in a temperature range where the anti-annealing behaviour of the silicon sensors is not significantly

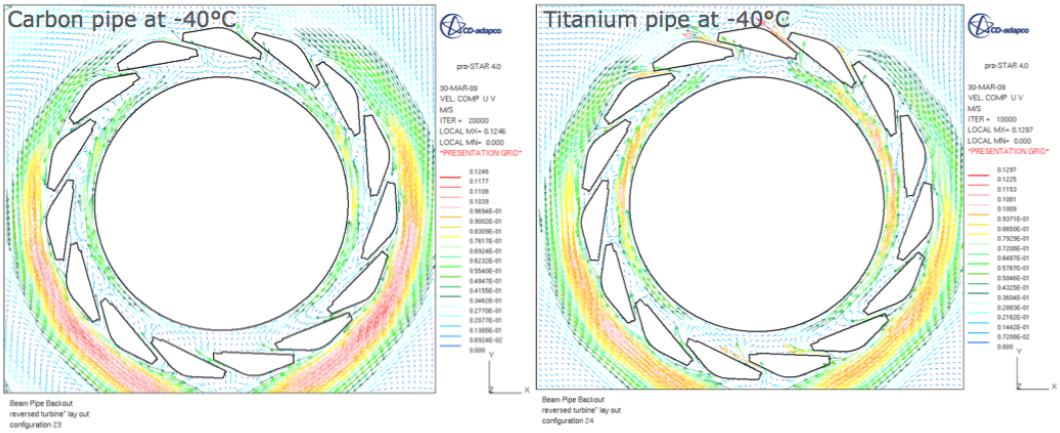


Figure 138. FEA simulation of radiation and convection for configurations with titanium (right) and carbon fibre (left) cooling pipes and an evaporation temperature of the cooling system of -40 °C.

effected in case the bake-out needs to be carried out with irradiated sensors, i.e. after significant operation of the IBL.

Due to the high temperature gradient during the bake-out, the proximity of beam pipe to sensors, and the tight packing of staves and services, radiation and convection have a significant impact on the heat transfer process. The FEA simulation for radiation and convection for the two cooling pipes studied for the IBL is shown in Fig. 138. The simulation yields, for the selected Ti pipe, a maximum heat load to the sensors of 2.25 W/cm due to convection and 0.31 W/cm due to radiation. For carbon fibre pipes, it yields a maximum heat load to the sensors of 1.81 W/cm due to convection, and 0.34 W/cm due to radiation. From the simulation it appears that there is sufficient cooling capacity to remove the static heat load during bake-out and protect the detector.

In order to verify the FEA simulation and obtain temperature measurements on staves, a 1:1 scale mock-up of a beam pipe section, prototype staves and IST is being constructed. This set-up will be operated under realistic conditions with detector cooling on prototype staves. One critical point to be assessed with the mock-up is the system reaction and temperature distribution for a finite-time cooling interruption. A cooling interruption will interlock the heating, however the beam pipe remains hot. A study will be carried out to asses if the stored energy in the hot beam pipe can be removed quick enough to avoid serious damage to the detector through over-temperatures.

10.2 Cooling Issues

The goal of the detector cooling system is to remove the dissipated heat from sensors and FE-electronics. In particular, the sensor temperature is of critical importance. The target temperature for operating the IBL sensors is approximately -15 °C, in order to minimise effects of reverse annealing on the sensors and to avoid thermal runaway.

The main parameters to influence the sensor temperature are the dissipated power in the sensor, which depends on radiation and operation voltage, the thermal conductivity of the stave, characterised by the thermal figure of merit of the stave (Section 4.2), and the evaporation temperature of the detector cooling system. Planar sensors put more stringent requirements on the stave thermal

management than the two other sensor types under consideration; 3D sensors operate at lower voltage and CVD sensors at lower leakage current after irradiation. This section focuses on the most severe requirements, as defined by the planar sensors with operation voltage of up to 1000 V.

The radiation fluence expected for IBL is shown as a function of sensor radius in Fig. 2. The fit to the simulation gives a parametrization as shown in Eq. 10.1:

$$\Phi(r) = (\frac{493}{r^2} + \frac{25}{r}) \times 10^{14} \tag{10.1}$$

For an inner most sensor radius of 31 mm, the estimate yields an expected fluence of 3.3×10^{15} n_{eq}/cm^2 without safety factors, for an integrated luminosity of 550 fb^{-1}. Considering safety factors, IBL sensors will be qualified up to 5×10^{15} n_{eq}/cm^2. Figure 44 (right) indicates that at 1000 V operation voltage, a sensor power dissipation per unit area of ≈200 mW/cm^2 normalised to -15 °C can be expected for annealed sensors, and ≈500 mW/cm^2 for non-annealed sensors. It appears prudent to assume that sensors will anneal throughout the IBL lifetime due to warm-up periods during detector maintenance. A procedure for beneficial annealing during shutdown periods can be implemented as part of the IBL operation protocol. For the sensors, it is therefore assumed a maximum power dissipation per unit area of ≈200 mW/cm^2 normalised to -15 °C.

Below, the results of an iterative calculation of the sensor temperature as function of the sensor operation parameters and the stave design, as presented in Section 4.2, are discussed. The sensor operation temperature and power dissipation is calculated by iteration. The stave thermal figure of merit, Γ_{total} [Kcm^2/W], is used in the calculation of the sensor temperature as

$$T = T_{coolant} + \frac{\Gamma_{total}}{A_{sensor}} * (P_{sensor} + P_{chip}) \tag{10.2}$$

where A_{sensor} is the sensor active area, P_{sensor} is the sensor power, and P_{chip} the maximum chip power of 1.5W. The current is scaled to the sensor temperature T according to Eq. 10.3, where $T_0 = -15$°C is the reference temperature.

$$I = I_0(\frac{T}{T_0})^2 \exp\frac{E_g(T - T_0)}{2k_B T T_0} \tag{10.3}$$

A constant sensor voltage of 1000 V is used in the calculation of the sensor power. 50 iterations are made to estimate the sensor temperature and its power dissipation per unit area. Each iteration checks the condition of thermal run-away, and if true, the calculation is interrupted. Table 37 summarises the parameters used in the calculation. The total stave thermal figure of merit consists of three components: the heat transfer between coolant and pipe inner wall, the glue layer to modules and the stave construction. The former two are assumed constant, while the later is being varied according to stave design.

The sensor temperature and thermal run-away for different cooling pipe options and different coolant evaporation temperatures are compared at default operation conditions (maximum chip power of 1.5 W and sensor bias voltage of 1000 V). Figure 139 (a) shows the sensor temperature as function of sensor power dissipation per unit area at -15°C for two different stave designs studied: single CF tube and single titanium pipe. The curves correspond to the different values of Γ_{stave} given in Table 37: for single CF pipe 19.3 Kcm^2/W and for single Ti pipe 4.5 Kcm^2/W. The values

Parameter	Value
Chip power [W/cm^2]	0.397
Chip Area [cm^2]	2.01 $\times$ 18.8
Sensor Area [cm^2]	2.01 $\times$ 16.8
Module Glue Interface [Kcm^2/W]	1.25
Heat transfer coolant to pipe [Kcm^2/W]	4.42
Γ_{stave} for CF pipe [Kcm^2/W]	19.3
Γ_{stave} for Ti pipe [Kcm^2/W]	4.5
Coolant temperature [°C]	-30 (C_3F_8) or -40 (CO_2)
Sensor bias voltage [V]	1000

Table 37. Parameters used in the calculation of sensor temperature.

for thermal figure of merit are taken from FEA simulations (see Γ for the total stave figure of merit in Table 19). The sensor power at -15 °C at which thermal run-away occurs are 2020 mW/cm^2 for Ti pipes and 560 mW/cm^2 for CF pipe for a coolant evaporation temperature of -40 °C (solid lines). At an evaporation temperature of -30 °C (dashed lines in the figure) the thermal run-away points worsen to 1040 mW/cm^2 for Ti pipes and 220 mW/cm^2 for CF pipes.

Figure 139 (b) shows the same curves assuming 30% worse thermal figure of merit for the staves. This is a prudent assumption to allow for unaccounted thermal impedances at interface layers, which may occur during production, or variation of thermal conductivities of components used in the assembly. With this safety margin, the thermal run-away occurs are 1730 mW/cm^2 for Ti pipes and 370 mW/cm^2 for CF pipe for a coolant evaporation temperature of -40 °C (solid lines). At an evaporation temperature of -30 °C (dashed lines) the thermal run-away points further worsen to 860 mW/cm^2 for Ti pipes and 140 mW/cm^2 for CF pipes.

The low figure of merit for a stave with one Ti pipe results in the best cooling power with significant margin against thermal run-away and lowest sensor temperature. For CF pipes, a coolant temperature of -40°C is required to meet the acceptance criteria for stable thermal operation of planar sensors at a sensor power dissipation per unit area of $\approx$200 mW/cm^2 normalised to -15 °C. For the operation of non-annealed planar sensors at 500 mW/cm^2 at -15 °C, Ti pipes in combination with CO_2 cooling provide an ample margin against thermal run-away and production variation of stave thermal conductivity. For the choice of IBL detector cooling, the minimisation of stave radiation length and the available experience in plant construction, service, installation and operation, have also to be considered. C_3F_8-based cooling is currently used for the ATLAS SCT and Pixel systems, while CO_2-based cooling is currently used for the VELO LHCb detector [90]. CO_2 allows to reduce the pipe-diameter in the stave and can provide lower evaporation temperature. These considerations led to choose CO_2 as a baseline coolant for the IBL, as well as the use of Ti pipes as there is more production experience available for Ti pipes, and they reduce the thermal figure of merit for the staves.

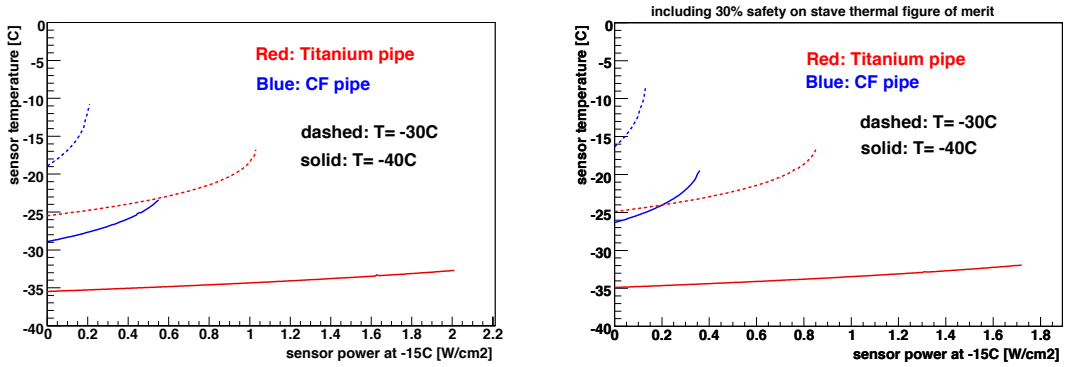
The envisaged operation of the IBL CO_2 plant foresees an evaporation temperature of -40 °C and a mass flow per stave in the range of 1.5 to 2 g/s. Currently, measurements are being carried on prototype staves using Ti pipes of 2 mm inner diameter, equipped with silicon heaters that provide

the heat flux expected from the sensor and chip power dissipation of the final stave for the above configuration. The heaters are equipped with temperature sensors to measure the temperature of the stave along its length. The CO_2 measurements are currently done at two laboratories in parallel. Preliminary results are given hereafter.

Figure 140 (left) shows the measured input and output temperature and pressure of a prototype stave with a 2mm ID Ti cooling pipe, in comparison to the NIST data expected values in a temperature range of interest for the IBL detector. The arrows indicate the set points of the CO_2 blow-off cooling test plant ranging from -25 °C to -40 °C evaporation temperature. Figure 140 (right) shows the measured silicon heater temperature, which corresponds to the sensor temperature of the final stave, along the stave without heating. Slight pressure drops ($\Delta P \approx 200$ mb equivalent to 0.5°C) can be seen.

Figure 141 shows the measured silicon heater temperature along the stave for different power densities and at different evaporation temperature set points in cold operation. For FEA simulation and cooling design, a dissipated heat of sensor and chip of 0.72 W/cm^2 is assumed. All, except one measurement (heater 10), show a uniform temperature which is approximately 9 °C above the evaporation temperature for a power density of 0.63 W/cm^2 and a mass flow of ≈1.5 g/s.

The same measurement was carried out in a second laboratory for verification. Figure 142 shows the measured silicon heater temperature along the stave for different power densities at room temperature operation with a CO_2 mass flow of 2.14 g/s. In the figure, the heater power density is given at the inner surface of the cooling pipe. A module power dissipation of 0.72 W/cm^2 corresponds to a power density of 2×10^4 W/m^2 at the inner pipe surface. This measurement also shows a total temperature difference between evaporation temperature and heater temperature of approximately 9 °C, which is higher than the expected temperature difference from simulations. This total temperature difference is built up by two main contributions: i) the heat transfer between



(a) (b)

Figure 139. Sensor temperature as function of sensor power dissipation per unit area for two different stave designs: single CF tubes (blue), single titanium pipes (red) and two coolant temperatures: -40 °C corresponding to an expected evaporation temperature for CO_2 (solid lines) and -30 °C corresponding to the lowest evaporation temperature for C_3F_8 (dashed lines). Figure (b) includes a 30% safety margin in thermal figure of merit.

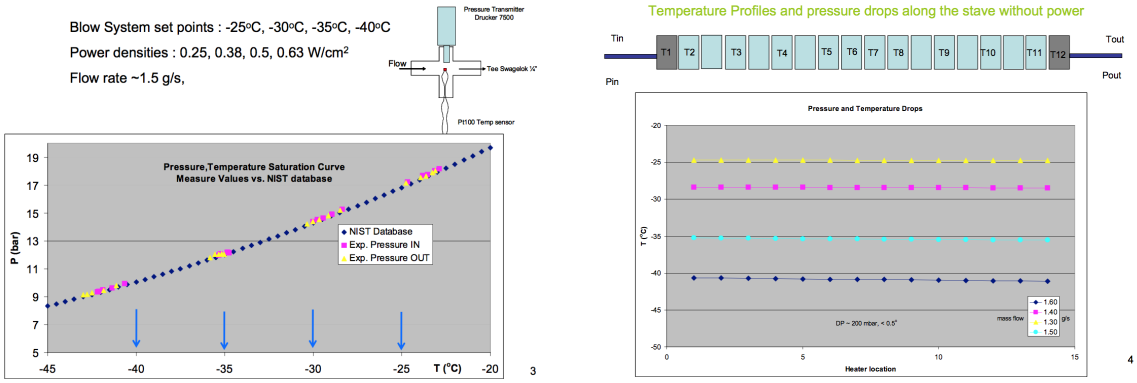


Figure 140. Left: Measured input and output temperature and pressures of a prototype stave with a 2 mm ID Ti cooling pipe in comparison to the NIST data expected values. Right: Measured silicon heater temperature along the stave without heating for four different evaporation temperatures.

coolant and inner pipe surface, and ii) the temperature gradient across the stave cross section. The first contribution (HTC) may be negatively effected by convection of coolant inside the pipe and separate measurements are currently ongoing to measure the heat transfer coefficient for Ti pipes and CO_2. The second contribution can be negatively effected by interface layers in the stave construction which present additional thermal barriers and are not properly taken into account in the simulation.

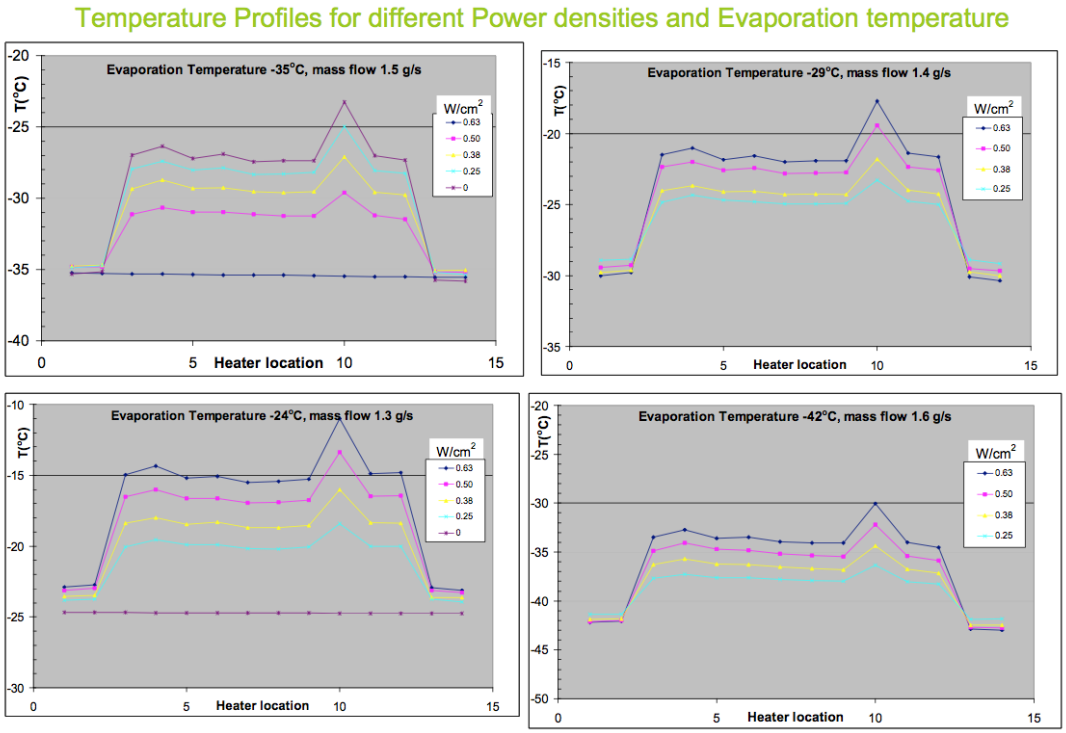


Figure 141. Measured silicon heater temperature along the stave for different power densities and at different evaporation temperature set points (cold operation).

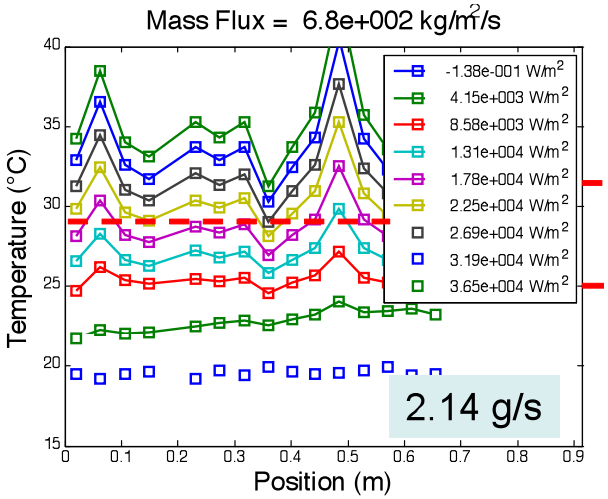


Figure 142. Measured silicon heater temperature along the stave (2 mm ID Ti pipe) for different power densities (room temperature operation).

10.3 Powering

The maximum allowed voltage on the chip internal network, the linear regulator or DC-DC converter, requires to minimize voltage drops between PP2 and the chips (see Section 4.5). In case of a sudden current drop to zero, the voltage must not exceed the maximum voltage as given in Table 12. This, in turn, forces the use of a large conductor cross section for power supply lines in type I and type II services, and wide conductor traces on the stave flex circuit. In particular, the conductors on flex circuit and type I services negatively effect the radiation length of the detector system. Additionally, the space for type I services feedthrough at the end of the IBL package is severely limited by the radius of the beam pipe flange and inner diameter of the IST.

The use of direct powering would only allow a 0.6 V voltage drop on the combined path of type 0/I/II, while voltage regulators on FE-I4 would allow voltage drop of 0.9 V. Having 1-to-2 DC-DC converters on FE-I4 could tolerate a drop of 1.33 V. Direct powering is ruled out by space constraints inside the IBL package and the beam pipe flange. Therefore, the use of linear regulators is the current IBL baseline. The feasibility of this assumption still needs to be demonstrated through measurements on the FE-I4 chip. Table 38 shows the voltage drop for the current baseline conductor cross section on type 0/I/II services, and the required cross sections to fulfil the most stringent voltage drop requirements. The cross sections of services, the service routing and voltage drops will be subject to further optimisation once measurements on the powering options of the FE-I4 are available.

10.4 Material and Weight Summary

The material and its weight considerably influences the physics performance of the IBL through the material's radiation and interaction length. Furthermore, the weight of the detector and its services plays a crucial role in the design of the detector support and dimensioning of support components. This section presents a top-down estimate of components weight, based on the current layout and material choices for the IBL.

	PP2 (V)	AWG Type2	Resistance Type2 (Ohm/km)	Length Type 2 (m)	PP1 (V)	AWG Type1	Resistance Type 1 (Ohm/km)	Length Type 1 (m)	PP0 (V)	Flex voltage drop @ 2A (V)	Chip (V)	Voltage Drop (V)
IBL baseline conductor cross sections	2.67	17.00	16.60	24.00	1.71	15.00	16.22	8.00	1.40	0.20	1.20	**1.47**
required cross sections to fullfill the most stringent voltage drop requirements	2.01	12.00	5.20	24.00	1.71	15.00	16.22	8.00	1.40	0.20	1.20	**0.81**

Table 38. Voltage drop on the combined supply lines from PP2 to the FE-I4 chip.

Table 39 gives the expected weight of services between PP1 and EoS for each side of the IBL detector. It takes into account the known mass of services for cooling, power and readout. The net estimate gives a mass of 10.7 kg for the services on each side of the IBL detector. Taking into account a 30% uncertainty, e.g. mass of cable insulations, a nominal weight of 14 kg for services on each side of the IBL between EoS and PP1 is considered.

Table 40 gives the expected weight of the beam pipe including heaters and insulation foam. Beam pipe services, e.g. cables to the heater, are currently not included. The estimated weight of the beam pipe excluding services is 4.9 kg. The weight of each stave is estimated to be 79 g per stave, leading to a total weight of 1.106 kg for 14 staves.

Table 41 gives an overview of the weight of all components to be inserted to the IST and to be supported by the IST. The IST itself will weigh 3 kg approximately.

Table 42 shows the contribution of diverse components to the IBL radiation length, calculated for the stave with the single Ti pipe of 2 mm outer diameter and considering the omega thickness of 300 μm, foam density of 0.25 g/cc, a 90 μm thick FE chip and 250 μm thick sensor. The bare stave (CF, carbon foam and pipe) contribute 0.56%; the stave loaded with modules and flex account 1.26%. Adding the contribution of the IST (shielding foil not included), the total for the IBL is 1.54%.

Material	Service nature	Service function type	Service function type	Function description	Characteristics NEW	OD	ID	Area	Density	Length	Weight side A	Weight side C	Side A	
													EoS	NUMBER at side A
	CABLES													
parallel bundle	E	L	L	Pixel module LV supply	[2x (4xAWG21)+ 1 xAWG20 + 1xAWG30]								4	56
ALU copper clad 15%Cu+85%Al				LV power supply	4xAWG 21 (eq AWG 17 Cu)	0.72		0.41	3.66	4.00	0.10	0.10	16	224
ALU copper clad				LV power return	4xAWG 21 (eq AWG 17 Cu)	0.72		0.41	3.66	4.00	0.10	0.10	16	224
ALU copper clad				LV Sensing thick	AWG 20	0.81		0.52	3.66	4.00	0.03	0.03	4	56
ALU copper clad				LV Sensing thin	AWG 30	0.25		0.05	3.66	4.00	0.01	0.01	8	112
Twisted Pair	E	H	H	Pixel module HV supply (VDET)	(2xAWG36)								7	112
Cu				HV power supply	AWG 36	0.13		0.01	8.90	4.00	0.00	0.00	8	112
Cu				HV power return	AWG 36	0.13		0.01	8.90	4.00	0.00	0.00	8	112
Twisted Pair	E	Dcs	Dcs		(2xAWG36)								8	112
Cu				Pixel module temperature monitoring DCS-IN	AWG 36	0.13		0.01	8.90	4.00	0.00	0.00	8	112
Cu				Pixel module temperature monitoring DCS-Return	AWG 36	0.13		0.01	8.90	4.00	0.00	0.00	8	112
Twisted Pair	E	Dcs	Env		(2xAWG36)								8	112
Cu				Pixel temperature monitoring ENV.:	AWG 36	0.13		0.01	8.90	4.00	0.00	0.00	8	112
Cu				Pixel temperature monitoring ENV Return:	AWG 36	0.13		0.01	8.90	4.00	0.00	0.00	8	112
Twisted Pair	E	Signal	Signal OUT		(2xAWG28) twisted								16	224
Cu				FE Chip signal OUT	AWG 28	0.32		0.08	8.90	4.00	0.05	0.05	16	224
Cu				FE Chip Signal OUT-Return	AWG 28	0.32		0.08	8.90	4.00	0.05	0.05	16	224
Twisted Pair	E	Signal	Clock		(2xAWG36) twisted								16	224
Cu				FE Chip CLOCK	AWG 36	0.13		0.01	8.90	4.00	0.01	0.01	16	224
Cu				FE Chip CLOCK-Return	AWG 36	0.13		0.01	8.90	4.00	0.01	0.01	16	224
	T			Outlet evaporative cooling system	Ti pipe								0	7
SS				Services Cooling		4.30	4.00	1.95	7.80	4.00	0.00	0.00	0	0
SS				Stave cooling		4.30	4.00	1.95	7.80	4.00	0.00	0.03	0	7
	T	Ev, P	Ev, P	Inlet Evaporative Cooling	Ti Pipe								1	7
SS				Services Cooling		2.00	1.50	1.37	7.80	4.70	0.00	0.00	0	0
SS				Stave cooling		2.00	1.50	1.37	7.80	4.70	0.03	0.00	1	7

0.382 **0.387**

1 stave **0.769**

14 staves **10.766**

.+30% **13.996**

Table 39. Voltage drop on the combined supply lines from PP2 to the FE-I4 chip.

Number of units	Parts of Sub-assembly	Number of units for parts of sub-assembly	Material	Volume (m^3)	Density (kg/(m^3))	Mass of one unit (kg)	Mass of all the units used (kg)	Mass of 1 sub-assembly (kg)	Mass of all sub-assemblies (kg)
1.00	Be Section	1.00	Beryllium	0.00	1840.00	1.67	1.67		
	Adaption for Section	2.00	Al: 93.7%; Cu: 6.3%	0.00	Al: 2700; Cu: 8930	0.19	0.38		
	Flange	2.00	AA2219 - T6			0.10	0.20		
	Foil Heater	6.00	Kapton			0.09	0.53		
								2.78	2.78
1.00	none	1.00	Polyimide	0.00	1420.00	0.11	0.11		
									0.11
1.00	none	1.00	Aerogel (pyrogel)	0.01	170.00	1.37	1.37		
								0.00	1.37
1.00	none	1.00	Al 105241	0.00	2750.00	0.18	0.18		
								0.18	0.18
4.00	Split Spacer	4.00				0.03	0.10		
								0.10	0.42
								ESTIMATED TOTAL MASS:	4.87

Table 40. Mass estimate for IBL beam pipe.

Component	Weight [kg]
14 IBL staves	1.106
10 support rings	0.150
2 sealing rings	0.040
2 service support rings	0.600
2 beam pipe heater connectors	0.200
IBL services both sides	13.996
Beam pipe	4.870
Total weight	**20.962**

Table 41. Weight of all components to be inserted to the IST and to be supported by the IST.

Component	X/X_0 [%]
Omega (300 μm)	0.168
Light Foam (0.25 μm/cc)	0.091
Ti pipe (2.2/2.1 mm OD/ID)	0.221
Adhesive (100 μm)	0.030
Coolant (CO_2)	0.049
Sub-total Bare Stave	**0.56**
Flex	0.180
FE chip (90 μm)	0.096
Bump-bonding	0.058
Sensor (250 μm silicon)	0.267
Module Adhesive	0.030
Module Flex with passive components	0.070
Stave Total	**1.26**
IST (55 μm CF)	**0.28**
IBL Total	**1.54**

Table 42. IBL radiation length [%].

11. Project Management and Organization

11.1 Collaboration and Management Structure

The organization chart of the IBL is shown in Fig. 143. The composition and role of the different bodies are explained hereafter.

11.1.1 IBL collaboration

The IBL collaboration is organized according to the ATLAS collaboration rules [96]. 42 institutes are signing the IBL interim-Memorandum of Understanding (i-MoU) [97]. The i-MoU is foreseen to be replaced by a final Memorandum of Understanding (MoU) when the sensor technology will be selected (mid of 2011); at that moment the commitment in terms of funds and resources will become firm.

Likely some institutes may leave the project if the selected sensor technology is not the one that they technically support. For this reason, when assigning responsibilities and resources to institutes, it has always being considered that enough resources should be available independently of the sensor technology that will be selected eventually.

The IBL collaboration is composed of several large institutes and many medium and small size institutes creating a considerable geographical diversity. These two factors, size and geographical distribution of the groups, have been an important factor in organizing the project, so as to optimize the potential of each group.

The IBL collaboration includes both institutes that built the existing ATLAS Pixel detector and new institutes. This group combines the expertise gained during the construction and operation of the current Pixel detector with a notable injection of new groups that make it possible to design and built the IBL in the short time scale needed. The IBL has also challenging issues linked to the beam pipe extraction, installation of the IBL with the new beam pipe, new cooling system and

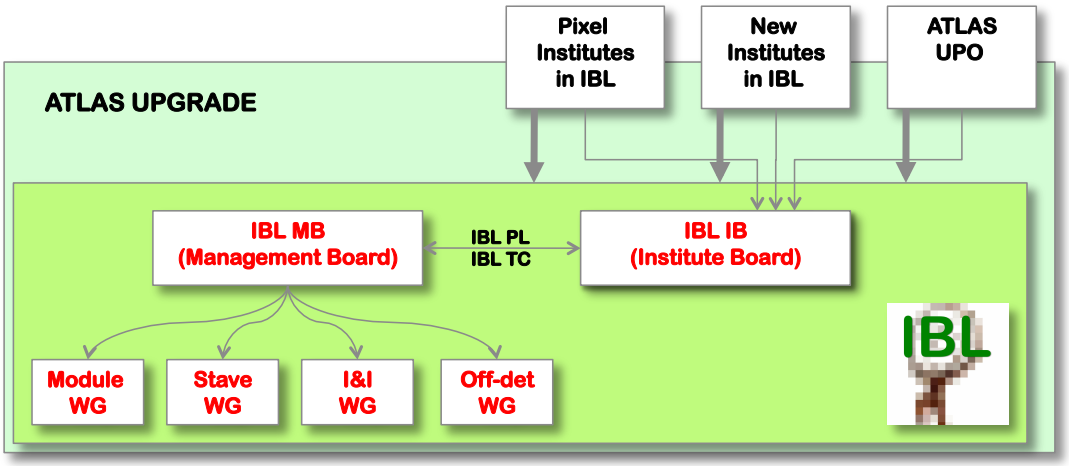


Figure 143. Organization chart for the IBL project.

plant, operation in a radiation activated environment, that would not be possible without a strong support of the ATLAS Technical Coordination.

From the former considerations the IBL collaboration is composed of Pixel institutes, new institutes and the Upgrade Project Office (UPO). The UPO is part of the ATLAS Technical Coordination in charge of the upgrade of the ATLAS detector.

11.1.2 Institute board

The Institutions contributing with both funds and personnel to the IBL project are part of the Institute Board (IB). The IB is an extension of the Pixel IB, and it usually meets right after the regular Pixel IB meetings.

The IB takes decisions on major technical issues and on sharing of resources and responsibilities. However, key technology choices affecting the overall performance of ATLAS are brought forward to the collaboration as a whole for decision in the ATLAS Collaboration Board.

11.1.3 Management board

The IBL Management Board (MB) controls the execution of the project. The MB is jointly chaired by the IBL Project Leader and Technical Coordinator (see Section 11.1.4). They appoint other MB members that shall be endorsed by the IB. The present MB composition is: Working Group coordinators (see Section 11.1.5), and the Pixel coordinators of Off-line, TDAQ and DCS software. Further members are the (Extended Pixel) Institute Board Chairperson, the Pixel detector and Inner Detector Project Leaders. The ATLAS Upgrade Coordinator, Technical Coordinator and Resource Coordinator are ex officio members.

MB meetings, that are hold every two weeks, have closed participation to MB members and speakers are invited to report on specific issues, on request of the IBL MB. The MB uses *Indico* and *SharePoint* to distribute material for discussion (see Section 11.1.7). Minutes are circulated to the IBL collaboration.

11.1.4 Project leader and technical coordinator

The IBL Project Leader (IBL PL) is elected in accordance to the ATLAS rules [96] and is in charge for two years, with the possibility to be renewed by $2/3^{rd}$ majority. The Institutes signing the IBL MoU, which are the ones bringing the resources to the project, vote for the selection of the PL.

It is up to the IB, in consultation with the PL, to decide wether to continue to have a Technical Coordinator (IBL TC), and if so, on the selection process.

11.1.5 Working groups

The IBL construction activities have been divided into four working Groups (WG). Each WG has two coordinators, who steer the activities and hold periodic meetings. Sharing of responsibilities between the two coordinators in each working group have been defined on mandate documents. The activities in the four working groups are:

Module WG

- Sensor design, prototyping, production and quality control.

- FE-I4 design, prototyping, procurement and quality control.
- Bump-bonding, thinning, bare module production and quality control.

Stave WG

- Local support (stave) including cooling pipe design, procurement and quality control.
- Cooling and stave thermal management design.
- Flex Hybrid and internal service design, procurement and quality control.
- Stave loading with module and electrical, thermal and mechanical quality control.

Integration & Installation WG

- Design and procurement of global support for beam-pipe, staves and services.
- Procurement of new beam-pipe.
- Integration of the staves with beam pipe and services in SR1 and quality control with cooling system and electronics.
- Design and installation of cooling plant and cooling services.
- Extraction of beam pipe. Installation of IBL package with beam pipe.
- Installation of services (cables, cooling, gas piping).
- ALARA compliance.

Off-detector WG

- Design and procurement of the R/O chain, including ROD/BOC and opto-links.
- Design and procurement of the power chain, including LV and HV power supplies and PP2 regulators.
- Design and procurement of DCS and interlock system.
- Design of procurement of cables and opto-fibers.
- System tests.
- Installation of the off-detector system.

11.1.6 IBL general meeting

These meetings are held three to four times a year and are the forum where discussions on any aspects of the IBL project take place. The different sessions are organized by the IBL PL and TC with the help of the WG coordinators. The progress and results of the four WGs are periodically presented at the General Meetings.

11.1.7 Collaborative tools

To transmit the information within the IBL project members, a *Share Point Collaborative Workspace* [98] has been created. Material relative to the project is uploaded and maintained under the responsibility of the WG coordinators and of the IBL PL and TC. This repository is used during the phase of preparation of documents. The final, approved documents are referenced and uploaded into the EDMS structure [99]. Working group and IBL general meeting agendas and slides are available in *Indico* [100].

A few, open-subscription (to ATLAS members) mailing lists have been created: a general mailing list[8] and lists for each of the WGs[9]. The software simulation activities have a dedicated mailing list[10] too. Additional mailing lists are created at discretion of WG coordinators, PL and TC.

11.2 Responsibilities

11.2.1 Resources and institute responsibilities

The overall IBL cost was evaluated based on a Work-package Breakdown Structure (WBS) prepared in 2009. At that time most of the project was still a conceptual design and costs were evaluated on the basis of knowledge from the construction of the existing Pixel detector. The total estimated cost is 9.7 MCHF of CORE value. It should be noted that the selection of the sensor technology could affect the final cost and this will be reflected in the final MoU.

Part of those costs were foreseen, for the so called B-layer replacement, already in 2002 when the MoU for Maintenance and Operation of the ATLAS detector [101] was made. Costs were planned to be covered by institutions who built the Pixel detector. The need of additional items and technology changes are covered by new institutions that joined the IBL project. For common infrastructure items, the costs are shared amongst the ATLAS Funding Agencies or institutes in proportion to the number of their scientific staff holding PhD or equivalent qualifications who are entitled to be named as authors of scientific publications of the Collaboration. These costs shall be charged to the M&O Category A.

The complete IBL project has been divided into 11 items, called ”MoU Items". A short description of each of those items and their cost are given in Table 43. The distribution of resources to cover those items from participating institutes is shown in Table 44. The IBL i-MoU [97] gives more details on costs and assigned resources.

11.2.2 Participating institutes

The participating institutes signing the interim-MoU are listed below.

Annecy LAPP: LAPP, Université de Savoie, CNRS/IN2P3, Annecy-le-Vieux, France.

J. Ballansat, P.-Y. David, P. Delebeque, N. Massol, T. Rambure, T. Todorov, T. Yildizkaya.

Barcelona: Institut de Física d'Altes Energies, IFAE, Edifici Cn, Universitat Autònoma de Barcelona, ES - 08193 Bellaterra (Barcelona), Spain.

[8] atlas-ibl-gen@cern.ch

[9] atlas-ibl-wg1@cern.ch, atlas-ibl-wg2@cern.ch, atlas-ibl-wg3@cern.ch, atlas-ibl-wg4@cern.ch

[10] atlas-ibl-software@cern.ch

System	MoU Item	Description	Cost (kCH)
Module	1	Sensor - prototype (including bumping to FE-I4), production, procurement & QC	752
	2	FE-I4 prototype (v1), production (v2), test	1 372
	3	Bump-bonding, thinning, bare module - prototype, production & QC	726
Stave	4	Local support (stave): CF structure, TM, pipe - prototype, production & QC	467
	5	Module assembly, stave loading, flex-hybrid, internal electrical services - design, production & QC	436
Off-detector	6	R/O chain: opto-board, opto-fiber, TX/RX, BOC, ROD, TDAQ (S-link, TIM, SBC, ROS, crate)	1 025
	7	Power chain: HV/LV PS, PP2 regulators, type2, 3 & 4 cables, interlock, DCS	505
Integration &	8	Integration in SR1 & System test	492
Cooling plant	9	Cooling plant & cooling services to PP1	461
Beam-pipe &	10	Beampipe & mechancal interfaces (to staves, to type 1 services, IST)	1 990
Installation	11	Installation in the pit: beampipe extraction, IBL+beampipe insertion, services installation	1 515
		Total	*9 741*

Table 43. The 11 MoU items and their evaluated CORE costs.

M. Cavalli-Sforza, S. Grinstein, I. Korolkov, C. Padilla, I. Troyano.

Bergen: University of Bergen, Department for Physics and Technology, Allegaten 55, NO - 5007 Bergen, Norway.

W. Liebig, H. Sandaker, B. Stugu.

Berkeley LBNL: Lawrence Berkeley National Laboratory and University of California, Physics Division, MS50B-6227, 1 Cyclotron Road, Berkeley, CA 94720, United States of America.

S. Dube, K. Einsweiler, M. Garcia-Sciveres, D. Gnani, N. Hartman, B. Heinemann, B. Holmes, F. Jensen, J. Joseph, Y. Lu, A. Mekkaoui, R. Witharm.

Berlin HU: Humboldt University, Institute of Physics, Berlin, Newtonstr. 15, D-12489 Berlin, Germany.

S. Grancagnolo.

Bologna: INFN Sezione di Bologna and Università di Bologna, Dipartimento di Fisica, viale C. Berti Pichat, 6/2, IT - 40127 Bologna, Italy.

G. Bruni, M. Bruschi, I. D'Antone, D. Falchieri, A. Gabrielli, A. Polini, R. Travaglini, A. Zoccoli.

Bonn: University of Bonn, Physikalisches Institut, Nussallee 12, D - 53115 Bonn, Germany.

D. Arutinov, M. Backhaus, M. Barbero, W. Dietsche, A. Eyring, L. Gonella, M. Gronewald, T. Hemperek, F. H§gging, J. Jansen, M. Karagounis, H. Kr§ger, A. Kruth, W. Ockenfels, S. Schultes, J.W. Tsung, N. Wermes.

Brandeis: Brandeis University, Department of Physics, MS057, 415 South Street, Waltham, MA 02454, United States of America.

J. Bensinger, A. Dushkin, K. Hashemi, H. Wellenstein.

CERN: CERN, CH - 1211 Geneva 23, Switzerland.

M. Battistin, O. Beltramello, M. Capeans, A. Catai, A. Catinaccio, F. Dittus, D. Dobos, C. Gallrapp, B. di Girolamo, J. Godlewski, H. Jansen, T. Klioutchnikova, A. La Rosa, S. Malyukov, S. Michal, D. Mladenov, G. Mornacchi, M. Nessi*, H. Pernegger, G. Piacquadio, M. Raymond, E. Richards, G. Spigo, R. Vuillermet, S. Wenig, Z. Zajacova, L. Zwalinski.

** Also at Université de Genève, Switzerland.*

DESY: DESY, Notkestr. 85, D-22603 Hamburg and Platanenallee 6, D-15738 Zeuthen, Germany.

I.-M. Gregor, U. Husemann, V. Libov, K. Mönig, I. Rubinskiy.

Dortmund: TU Dortmund, Experimentelle Physik IV, DE - 44221 Dortmund, Germany.

C. Gössling, D. Münstermann, A. Rummler, G. Troska, T. Wittig.

Geneva: Université de Genève, Section de Physique, 24 rue Ernest Ansermet, CH - 1211 Geneve 4, Switzerland.

G. Barbier, F. Cadoux, A. G. Clark, S. Débieux, D. Ferrere, C. Husi, D. La Marra, M. Weber, X. Wu.

Genova: INFN Sezione di Genova and Università di Genova, Dipartimento di Fisica, via Dodecaneso 33, IT - 16146 Genova, Italy.

D. Barberis, R. Beccherle, G. Darbo, G. Gagliardi, G. Gariano, C. Gemme, P. Morettini, B. Osculati, F. Parodi, S. Passaggio, L. Rossi, A. Rovani, E. Ruscino.

Glasgow: University of Glasgow, Department of Physics and Astronomy, Glasgow G12 8QQ, United Kingdom.

R. Bates, C. Buttar.

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11.3 Planning and Milestones

The IBL project schedule covers from prototyping to the end of the project, defined as when the IBL is handed over, ready for operation, to the ATLAS Pixel system. The main blocks of the schedule are given by the prototyping, qualification and production of the core components of the IBL as well as their final integration, as listed below:

- FE-I4 readout chip and sensors.
- Module prototyping and assembly.
- Bare stave prototyping and production and, loading of modules to the staves.
- Design and production of stave support, IST, beam pipe and the integration of staves to the final IBL package on the surface.

- Prototyping and production of off-detector elements (services, readout, power supply, DCS and cooling).
- Installation of off-detector parts and installation of the IBL detector.
- Final stage of commissioning the IBL in ATLAS and hand over for operation.

For the installation of the IBL, a long shutdown is needed with a full opening of ATLAS on one side. Full opening is needed because of the beam pipe operations (removal of beam pipe and installation of IBL package with a new beam pipe). In the current planning the long shutdown when the IBL will be installed is expected to start at the end 2015 / beginning of 2016.

Figure 144 shows the main blocks of the schedule. Currently the development of the readout chip is the main component driving the schedule. The first chip version is foreseen during 2010, the second engineering version during 2011 and the production during 2012. The decision on sensor technology is expected at the end of the module qualification program by mid 2011. The module production will be the main activity during second half 2012 and early 2013. Stave production and loading with modules is foreseen for 2012-13. The surface integration of the IBL will be the main activity in 2014, followed by system tests of the final package. The current schedule foresees two contingency periods: 3 months during stave loading in 2013 and 3 months at the end of IBL integration in the surface. This leads to a ready for installation date in May 2015, including those two contingency periods. Currently the main schedule risk is the FE-I4 development and this until detailed test results of the first version are available; they are expected during the second half of 2010. Table 45 gives an overview of milestones based on this schedule.

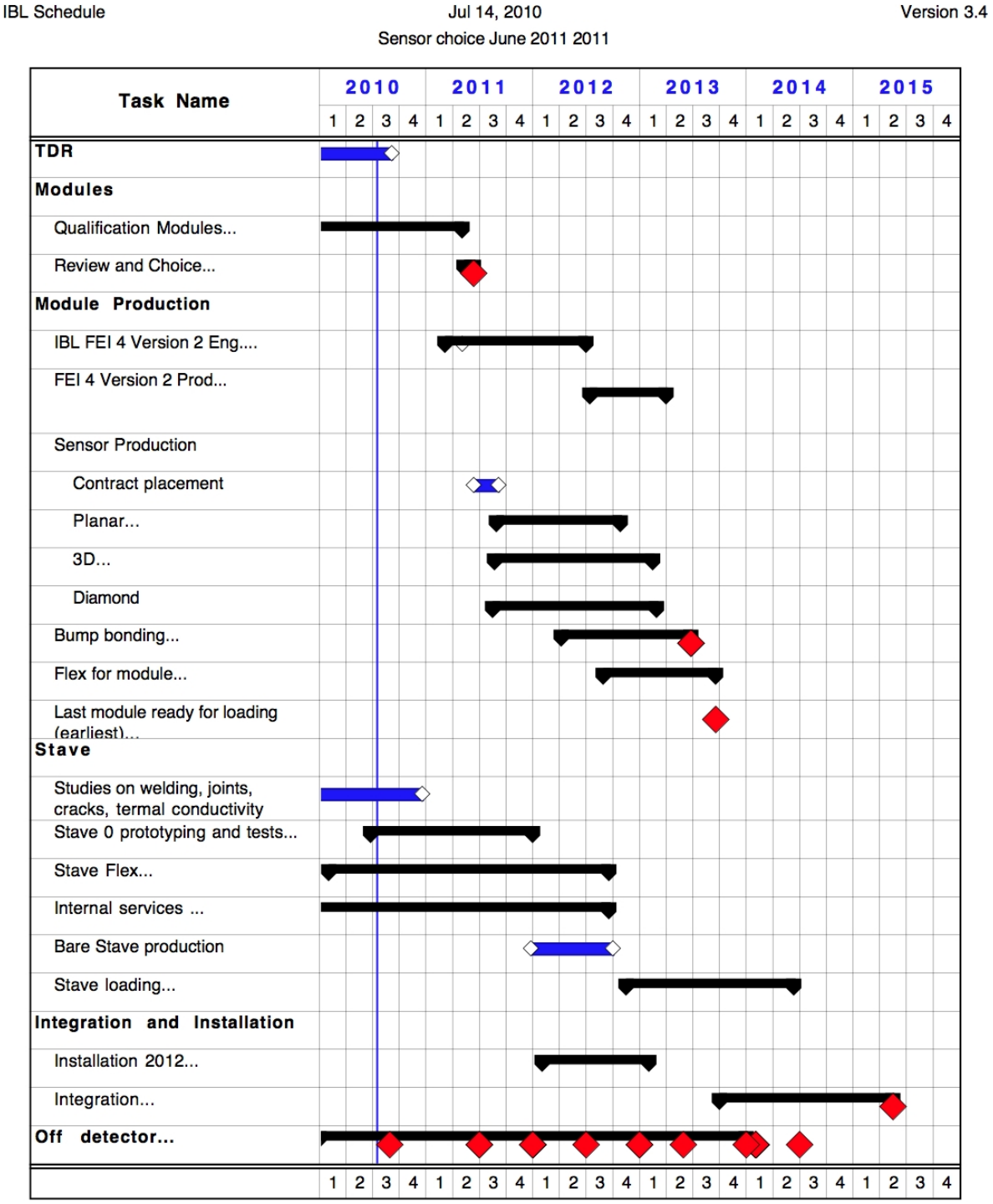

Figure 144. Overview of the IBL project schedule (version of July 2010).

Institutions in the IBL Construction		IBL MoU Deliverables										
		1	2	3	4	5	6	7	8	9	10	11
Institution	Country	Sensor	FE-I4	Bump-bonding	Stave	Mod.Load	R/O Chain	PS Chain	Integration	Cooling plant	BP & Interfaces	Installation
Annecy LAPP	France				1							
Barcelona	Spain	1		1				3	2			
Bergen	Norway	1										
Berkeley LBNL	United States of America		1				1				1	
Berlin HU	Germany											
Bologna	Italy						1					
Bonn	Germany	1	1	1		1			2			
Brandeis	United States of America										1	
CERN	Switzerland	1		1	1	1			1	2		
DESY	Germany						1	1				
Dortmund	Germany	1										
Geneva	Switzerland		1			1			1		1	
Genova	Italy		1			1	3	3				
Glasgow	United Kingdom	1										
Göttingen	Germany		2				1		2			
Grenoble LPSC	France										1	1
Heidelberg ZITI	Germany											
Iowa	United States of America							1	2			
KEK	Japan	1		1								
Liverpool	United Kingdom	1										
Ljubljana	Slovenia	1										
LPNHE Paris	France	1			2							
Manchester	United Kingdom	1										
Marseille CPPM	France		1		1	1						
Milano	Italy			1	1			1				
Munich MPI	Germany	2										
New Mexico	United States of America	1										
Nikhef	Netherlands		1		2					2		
Ohio State University	United States of America	1					1					
Oklahoma	United States of America						1		2			
Oklahoma SU	United States of America						1					
Orsay LAL	France	1										
Oslo	Norway	1				2			2			
Prague AS	Czech Republic	1										
Santa Cruz UC	United States of America	1				1			2			
Siegen	Germany						1					
SLAC	United States of America	1			2	1	2		2	2		
Stony Brook	United States of America	1					2		2			
Taipei AS	Taiwan						1					
Toronto	Canada	1										
Udine	Italy	1										
Wuppertal	Germany				1		1	1	2			
ATLAS TC	World Wide									1	1	1

Legend:

1	Funds/Deliverables and Personnel
2	Personnel only
3	In kind M&O-A

Table 44. Contributions of IBL Institutions, in work and costs.

Milestone	Description	Due Date
M1	FE-I4 version 1 submission	Jun 2010 (done)
M2	Sensor choice	Jun 2011
M3	FE-I4 version 2 submission	Sep 2011
M4	First production modules	Nov 2012
M5	Last production modules	Sep 2013
M6	Stave loading completed (contingency incl.)	Jun 2014
M7	IBL ready for installation (contingency incl.)	May 2015

Table 45. Major IBL Milestones.

A. Appendix: From Pixel *B*-Layer Plan to IBL

The *B*-Layer replacement plan

The layout of the Pixel system has undergone several changes from the ATLAS Technical Proposal (TP) [102, 103] in 1994 to the present design. In the TP the two exterior layers were put at radii larger than 10 cm to survive three years at low luminosity ($\mathscr{L} = 10^{33}$ cm^{-2}s^{-1}) plus seven years at nominal luminosity ($\mathscr{L} = 10^{34}$ cm^{-2}s^{-1}), corresponding to an integrated luminosity of 730 fb^{-1}. At that time, the available sensor technology and electronics would not have allowed to go below 10 cm radius for operating ten years at LHC and hence, the *B*-layer was foreseen only for the initial three years of low luminosity, at a radius of 4 cm (one centimetre less than the built detector). Also, the beam pipe in the TP is smaller (outer diameter of 5 cm instead of 5.8 cm).

The *B*-layer developed further in the years to come. In 1997, when the ID TDR [11, 104] was published, the radius discussed was between 4.15 cm and 4.70 cm, being a function of the beam pipe diameter which was still undetermined. The outer Pixel layers were still at a radius above 10 cm, but the gap between the two was reduced.

The Pixel TDR [105] came one year later in 1998. The Pixel TDR considered a Pixel layout where the two outer barrels were in the same thermal enclosure as the Semiconductor Tracker (SCT), using the same global support structure. The *B*-layer design was based a clam-shell concept to allow replacement of this layer every three years of LHC operation at nominal luminosity. The clam-shell concept and the tool, excerpted from the Pixel TDR, to extract and insert the *B*-layer is shown in Fig. 145.

The progress in the sensor technology (oxygenated sensor) and, at the same time, the delay in the transition to radiation hard versions of the front-end chip and of the module control chip (MCC), led to the definition of a "reduced layout" in the year 2000. This layout had two pixel layers (*B*-layer and layer-1) insertable. The idea being the need of having only one barrel layer

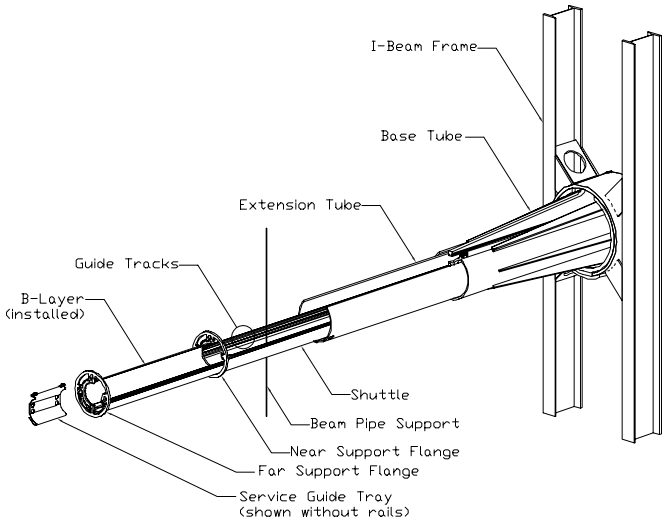

Figure 145. The tooling foreseen for extracting/inserting the Pixel *B*-layer as conceived at the time of the Pixel TDR.

(layer-2) ready in time for installation together with the rest of the ID.

Further accumulated delay brought, one year later (2001), to a fully insertable Pixel detector. Initially the *B*-Layer kept the original clam-shell design that allowed the insertion/extraction separately from the rest of the barrel and of the disks, but the reduced space available for the internal services did not allow to separate those of the *B*-layer from the rest of the detector. Finally, the only way to replace the *B*-layer became the extraction of the whole Pixel package.

Table 46 shows the changes of the barrel Pixel detector geometry from the ATLAS TP to today. It is worth mentioning that from the ATLAS TP until today, the module size and layout remained almost unchanged with 16 FE chips. The initial pixel size of 50 $\mu m \times 300$ μm became the present one of 50 $\mu m \times 400$ μm.

The *B*-layer Task Force and the IBL Concept

In January 2008, the ATLAS Executive Board (EB) established a task force (*B*-Layer Task Force - BLTF) with the mandate to present to the Collaboration an updated strategy for the *B*-layer and the Pixel system evolution in ATLAS. The BLTF met regularly from February to June 2008 and presented the final report [3] to the ATLAS collaboration in July 2008.
The BLTF analyzed several general issues related the evolution of the Pixel system: radiation studies on the Pixel detector and evaluation of the radiation damage of sensor and on-detector electronics, activation of material, ALARA procedures, ATLAS opening and closing scenarios including beam-pipe extraction and options for a new beam pipe.
Given the difficult accessibility of the present system, several failure modes of the present system were considered, in particular hard failures of the internal cooling, on-detector optical components, mechanical adhesion, wire-bonding and internal electrical connections. The BLTF also looked at plans for LHC machine upgrade and luminosity scenarios.

The replacement options that were investigated by the task force are:

1. A 2-layer replacement detector based on the existing detector design and using the existing detector technology where possible.

2. A variant of (1), with one or both of the layers based on prototype sensor and FE electronics technology being developed for the LHC upgrade, depending on its availability.

3. A small radius *B*-layer insertion using existing sensor and electronics technology.

	TP Layout		ID TDR		Pixel TDR		Reduced		Insertable	
	1994		**1997**		**1998**		**2000**		**Today**	
	R (cm)	Staves	R (cm)	Staves	R (cm)	Staves	R (cm)	Staves	R (cm)	Staves
BL	4.0	16	4.75	20	4.3	18	5.05	22	5.05	22
L1	11.5	36	10.55	44	10.1	42	7.90	34	8.85	38
L2	16.5	52	13.75	58	13.2	56	12.70	56	12.25	52

Table 46. Pixel barrel layout versions from ATLAS Technical Proposal to the as-built detector.

4. A small radius *B*-layer insertion using prototype technology being developed for the sLHC.

The best and most feasible solution ended up being number 4, with the others not favoured for various reasons: procurement time (1 and 2) and reduced performance with respect to the existing detector (1), and also radiation limitations and mechanical constraints (3). The most critical aspects of the selected option 4 were considered to be the extraction of the existing beam pipe in situ without damaging the current *B*-layer and the feasibility of inserting a new *B*-layer together with a smaller radius beam-pipe.

B. Appendix: ATLAS IBL Acronyms

ADC	Analogue-to-Digital Converter
ALARA	As Low As Reasonably Achievable
ASIC	Application-Specific Integrated Circuit
ATCA	Advanced Telecommunications Computing Architecture
ATLAS	A Toroidal LHC ApparatuS
AWG	American Wire Gauge
BBIM	Building Block Interlock and Monitoring
BER	Bit Error Rate
BeO	Beryllium Oxyde
BC	Bunch Crossing
BCR	Bunch Counter Reset
BLTF	B-Layer Task Force
BOC	Back Of Crate
BPM	Bi-Phase Mark encoded
BPR	Back Pressure Regulator
CERN	European Organization for Nuclear Research
CF	Carbon Fibre
CMM	Coordinate Measuring Machine
CTE	Coefficient of Thermal Expansion
CTP	Central Trigger Processor
CVD	Chemical Vapor Deposition
DAC	Digital-to-Analogue Converter
DAQ	Data Acquision system
DB	DataBase
DESY	Deutsches Elektronen-Synchrotron
DC	Direct Current
DCS	Detector Control System
DSS	Detector Safety System
DMILL	Durci Mixte sur Isolant Logico-Lineaire (a radiation-hard ASIC technology)
DORIC	Digital Opto-Receiver Integrated Circuit
DSP	Digital Signal Processors
DSS	Detector Safety System
ECR	Event Counter Reset
EDMS	Engineering Data Management System
ELMB	Embedded Local Monitor Board
ENC	Equivalent Noise Charge
EoS	End of Stave
FE	Front-End
FEA	Finite Element Analysis
FIT	Front-end Integration Tool
FPGA	Field-Programmable Gate Array
FSM	Finite State Machine
HEP	High Energy Physics
HL-LHC	High Luminosity LHC
HSIO	High Speed I/O
HTC	Heat Transfer Coefficient
HV	High Voltage
IB	Institute Board
ID	Inner Detector
IDEP	Inner Detector End-Plate
IBL	Insertable B layer
iMoU	Interim Memorandum of Understanding
IPC	Inter Process Communication
IST	IBL Support Tube
ITT	Integration and Testing Tool
JVF	Jet-Vertex Fraction
LHC	Large Hadron Collider
LVDS	Low-Voltage Differential Signalling
LV	Low Voltage

LVL1	Level 1
MB	Management Board
MCC	Module Control Chip
MDP	Maximum Design Pressure
MoU	Memorandum of Understanding
MSR	Mark-to-Space Ratio
NRZ	Non Return to Zero
NTC	Negative Temperature Coefficient
OPC	OLE for Process Control
OTDR	Optical Time Domain Reflectometer
PCB	Printed Circuit Board
PiN (diode)	Positive intrinsic Negative (diode)
PL	Project Leader
PP	Patch Panel
PST	Pixel Support Tube
PVSS	Prozessvisualisierungs und Steuerungs System
RCE	Reconfigurable Cluster Element
ROBin	ReadOut Buffer Interface
ROD	ReadOut Driver
ROS	ReadOut System
RP	Radio Protection
RST	Reset
RX	Receiver
SBC	Single Board Computer
SEU	Single Event Upset
SCT	SemiConductor Tracker
SEU	Single Event Upset
SF	Safety Factor
SIT	System Integration Tool
SMT	Stave Mounting Tool
SPS	Super Proton Synchrotron
SR1	Atlas Inner Detector Integration facility SR1 building 2175
TAS	Target Absorber Secondaries
TC	Technical Coordinator
TCT	Transient Current Technique
TDAQ	Trigger and Data AcQuision
TDC	Time-to-Digital Converter
TDR	Technical Design Report
TIG	Orbital Tungsten Inert Gas
TIM	TTC Interface Module
ToT	Time Over Threshold
TPP	Test Patch Panel
TRT	Transition Radiation Tracker
TTC	Timing, Trigger, and Control
TX	Transceiver
UBM	Under Bump Metallization
USA	Underground Service Area
UPO	Upgrade Project Office
VCSEL	Vertical Cavity Surface-Emitting Laser
VDC	VCSEL Driver Chip
VI	Vacuum Inner detector
VME	Versa Module Eurocard
WBS	Work-package Breakdown Structure
WG	Working Group

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