ATLAS-IBL Pixel Upgrade

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on the behalf of

ATLAS IBL Collaboration

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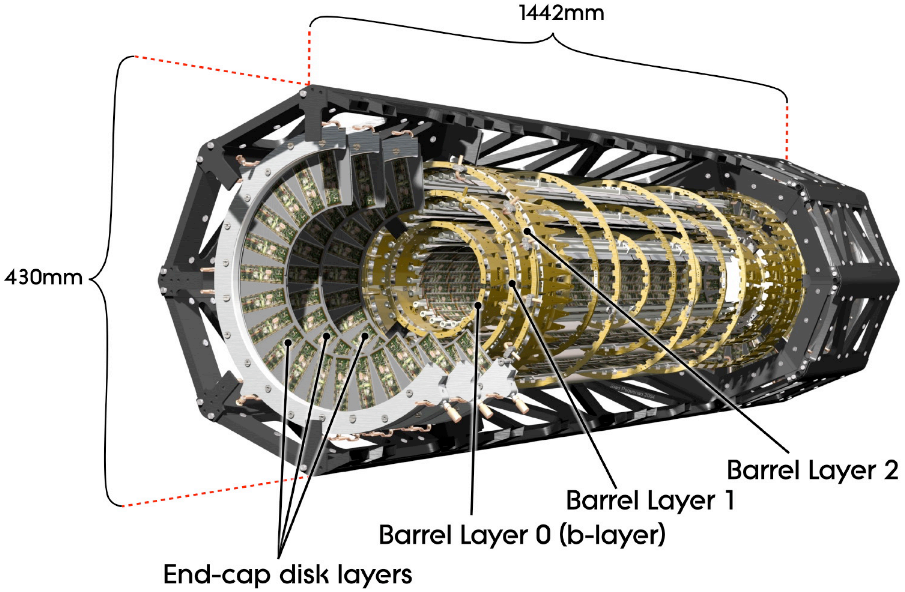
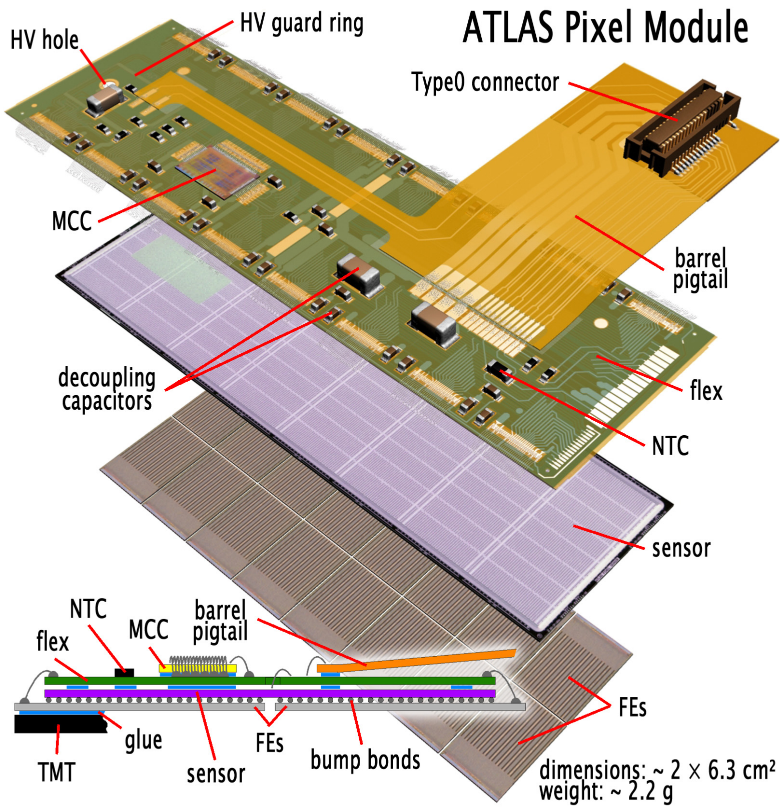
Overview

- The current ATLAS Pixel detector
- The 4th Pixel Layer: Insertable B-Layer (IBL)
- IBL Layout
- Requirements for IBL sensors and electronics
- The FE-I4 front-end electronics
- Highlights form ATLAS Pixel Sensor Upgrade programs
  - Planar-Si, 3D-Si and Diamond
- IBL Module design
  - Planar-Si design
  - 3D-Si design
  - CVD Diamond design
- Bump bonding
- 2010/11 IBL Module qualification program
- IBL status and outlook

The current ATLAS Pixel detector



- ATLAS Pixel Detector
  - 3 barrels + 3 forward/backward disks
  - 112 stave and 4 sectors
  - 1744 modules
  - 80 million channels



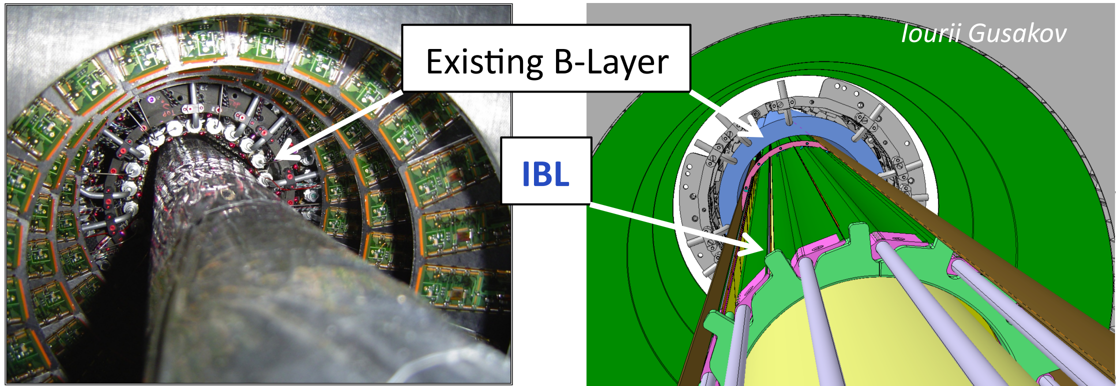
- **ATLAS Pixel Module**
  - 16 front-end chips (FE-I3) module with a Module Controller Chip (MCC)
  - 46080 R/O channels 50 µm x 400 µm (50 µm x 600 µm for edge pixel columns between neighbour FE-I3 chips)
  - Planar N-in-N DOFZ silicon sensors, 250um tick
  - Designed for 1 x 10^{15} 1MeV fluence and 50 Mrad
  - Optolink R/O: 40÷80 Mb/link

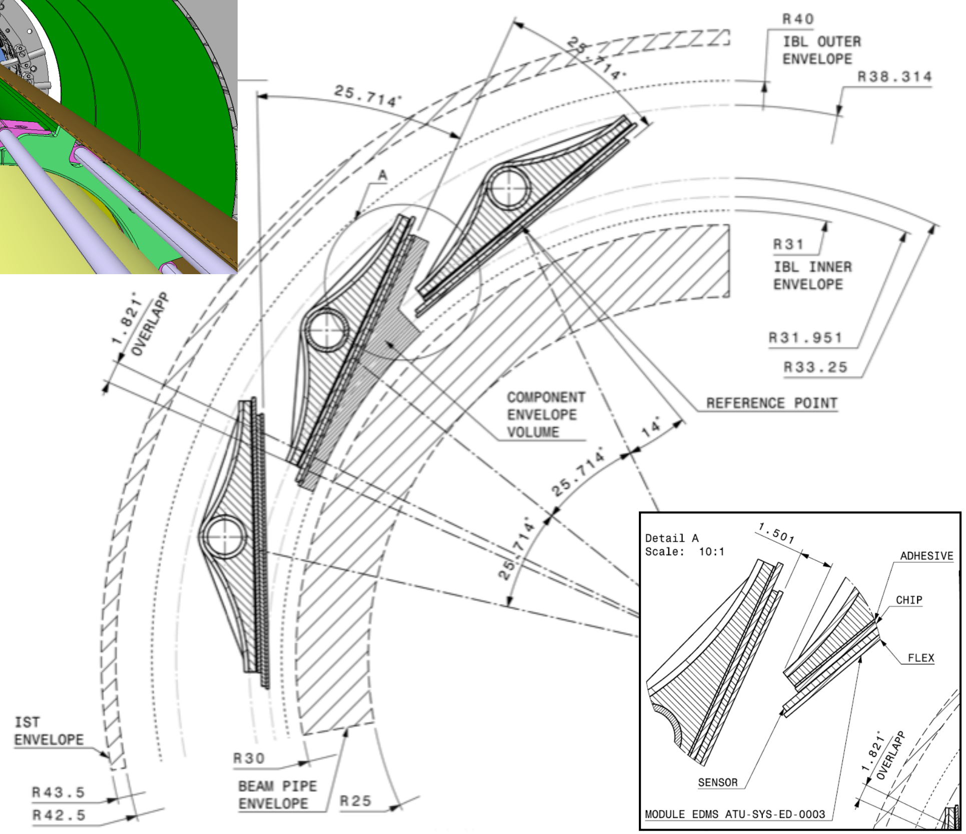
The 4th Pixel Layer: Insertable B-Layer

- Add a 4th low-mass Pixel Layer inside the present B-Layer: The Insertable B-Layer
  - Improve performance of existing system
  - Maintain performance when present B-Layer degrades
  - Existing Pixel detector stays installed and a 4th layer is inserted inside the existing pixel detector together with new beam pipe → Requires new, smaller radius beam pipe to make space
  - It needs to be replaced in a long shutdown (length required is more like 9 months). Build detector ready for installation end 2014
- It serves also as technology step from now to sLHC
  - IBL project will be the first to use much of the new technologies currently under development for sLHC
  - Radiation hardness ~ $5x10^{15}$ n_{eq}/cm^2
  - Front-end (FE-I4): go to IBM 130 nm process and improve readout architecture
  - Sensors: investigate new planar-Si sensors, 3D-Si sensors, and CVD diamond sensors
  - Readout system & optolink: 160MB/s for data
  - CO_2 Cooling system & mechanics: develop light-weight support

IBL Layout

- The envelopes of the existing Pixel Detector and of the beam-pipe leave today a radial free space of 8.5 mm
- The reduction of 4 mm in the beam-pipe radius brings it to 12.5 mm
- → Make possible the design of the IBL detector to fit in !!!



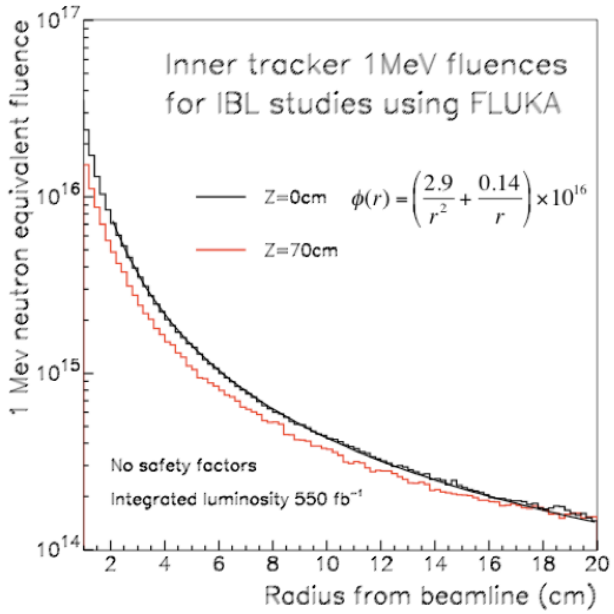


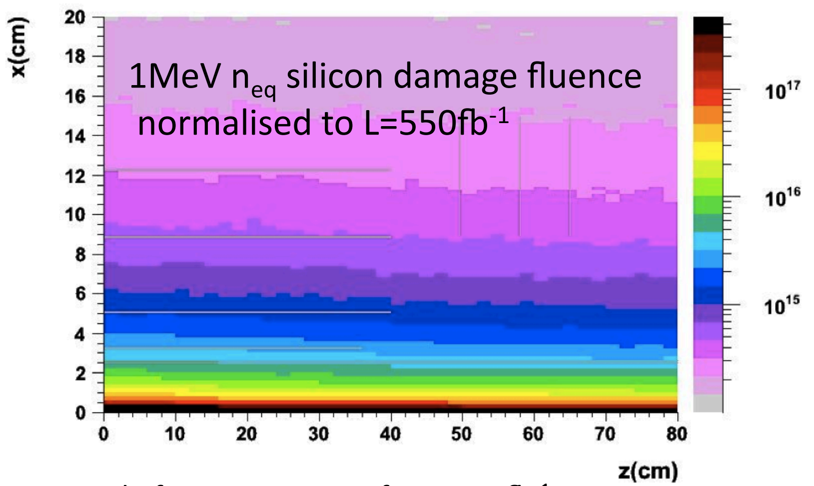
- Defined the baseline geometry
- 14 staves
- 32 FE-I4's per stave with sensors facing the beam pipe
- Main number:
  - R_{in} = 31 mm
  - R_{out} = 38.2 mm
  - $\langle R_{sens} \rangle$ = 33 mm

Requirements for IBL sensors & electronics

Requirements for IBL

- IBL design peak luminosity = 3 x 10^{34} $cm^{-2}s^{-1}$ → New FE-I4 / higher hit rate
- Integrated luminosity seen by IBL=550 fb^{-1} → Survive to sLHC phase II
- Design sensor/electronics:
  - NIEL dose = 3.3 x 10^{15} ± ("safety factor") ≥ 5 x 10^{15} n_{eq}/cm^2 (equivalent to 1000 fb^{-1})
  - Ionizing dose ≥ 250 Mrad
  - Low dead area in Z: slim or active edge
  - Max sensor power < 200 mW/cm^2 normalized to -15C sensor temperature
  - Maximum bias voltage (system issues): 1000 V





- Fit made for 2 < r < 20 cm for L=550fb^{-1}
- Gives for IBL @ 3.2 cm (550 fb^{-1}):

Φ1MeV=3.3x10^{15} n_{eq}/cm^2 (1.6 MGy)

The FE-I4 front-end

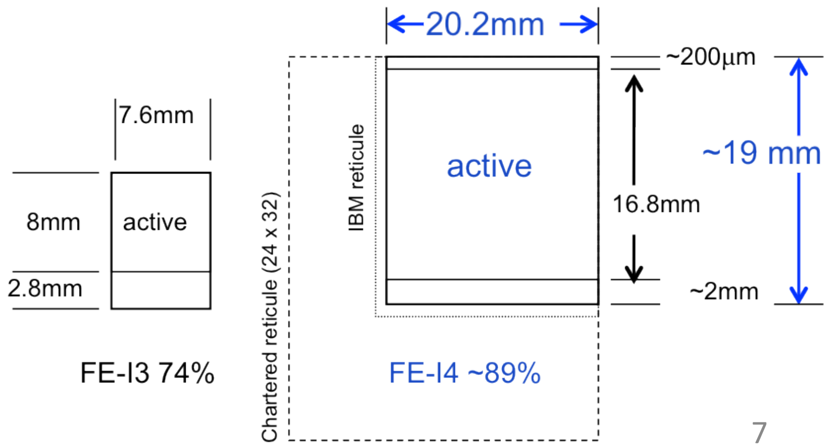
- Reason for a new FE design:
  - Increased rad hard
  - New architecture to reduce inefficiencies (*L*=3xLHC)
- Biggest chip in HEP to date
- Greater fraction of footprint devoted to pixel array
- Lower power*: don't move the hits around unless triggered*
- Able to take higher hit rate: *store the hits locally in each pixel and distribute the trigger*
- No need for extra module control chip: *significant digital logic block on array periphery*
- Present status: *Submission end of June 2010*

Design collaboration (15 IC designers):
Bonn, CPPM, INFN-Genova, LBNL, NIKHEF

Specification & test setup development:
Bonn, CERN, Goettingen, LBNL

- FE-I3 → FE-I4

	FE-I3	FE-I4
Pixel size [μm^2]	50x400	50x250
Pixel array	18x160	80x336
Chip size [mm^2]	7.6x10.8	***20.2x19.0***
Active fraction	74%	89%
Analog current [μA/pix]	26	***10***
Digital current [μA/pix]	17	***10***
Analog voltage [V]	1.6	***1.5***
Digital voltage [V]	2.0	***1.2***
Pseudo-LVDS out [Mb/s]	40	***160***

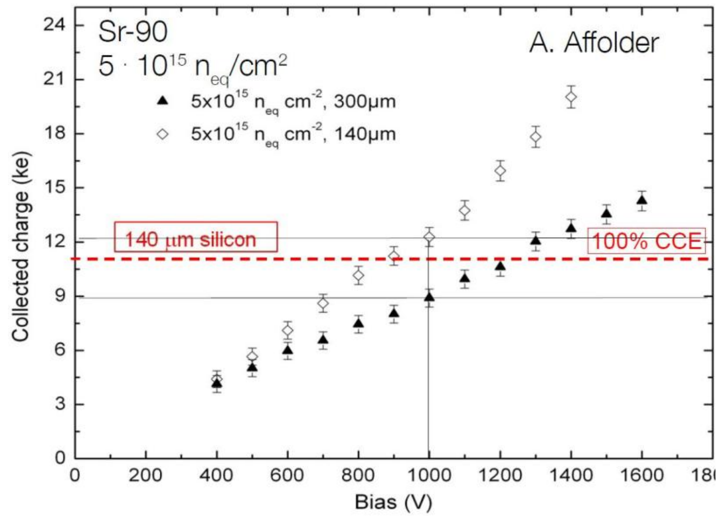


Highlights from *ATLAS Planar R&D*

- ATLAS approved R&D project for sLHC
- Participating Institutes: 17
- Main areas of R&D:
  - Slim edge sensors to reduce inactive area
  - Radiation damage in planar sensors
  - Bulk materials (N-in-N, N-in-P, DPFZ and MCz)
  - Simulation of sensor design and detector layout
  - Low threshold operation of FE readout
  - Low cost, low scale pixel production

D. Muenstermann
J. Weingarten
Manchester and PPS Workshops
References at page 24

- Charge Multiplication (CM)
  - Observed CM in highly irradiated strips & diodes (RD50)
  - Charge collection efficiency (CCE) frequently exceeds 100% (especially thin sensors)
  - Over a wide region, CCE is nearly linear function of bias voltage
  - Thin Sensors:
    - Superior charge collection at high fluence
    - Less material



See talk by G. Casse on Thu.

Highlights from *ATLAS Planar R&D*

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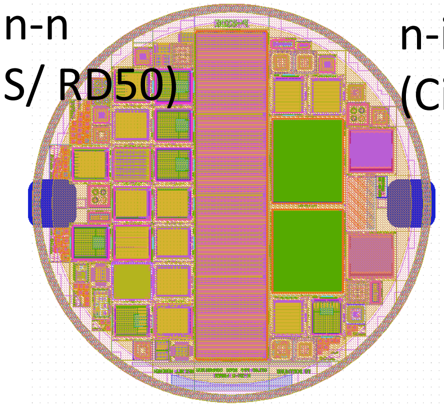
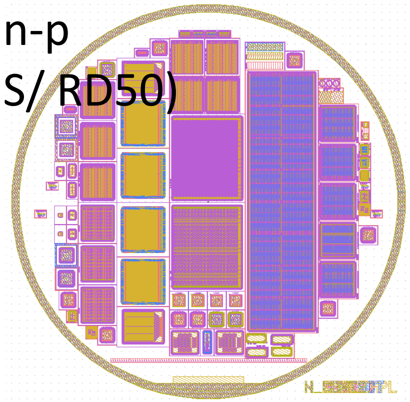
References at page 24

- Sensor production
  - PPS/RD50 production at CiS
  - Dedicated IBL production at CiS
  - KEK with HPK
  - Micron

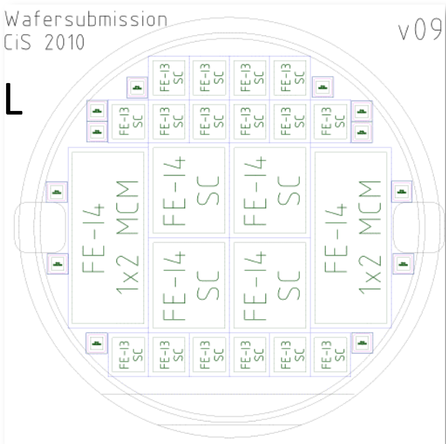
n-in-n (CiS/ RD50)

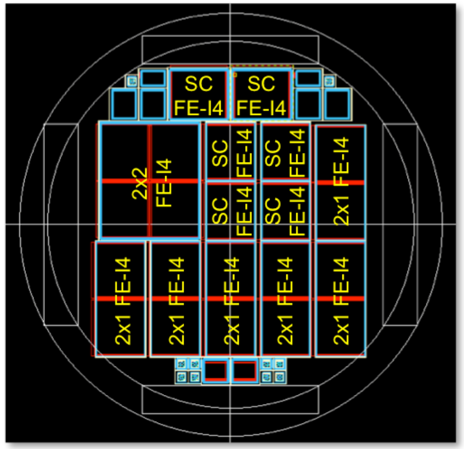


n-in-p (CiS/ RD50)



IBL





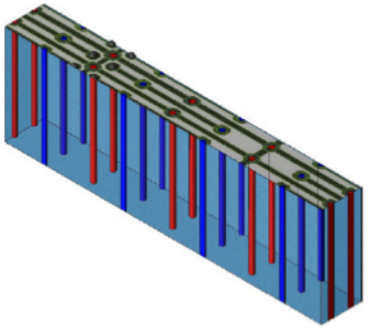
- Low-threshold operation at 1100 e- (front-end: FE-I3)
- Irradiation and test beam
  - **Irradiation**: CERN (24 GeV protons), Karlsruhe (25 MeV protons), Ljubljana (reactor neutrons), Prague (reactor neutrons)
    - Samples was characterize and partially tested in test beam
  - **Beam Tests**: CERN and DESY (Eudet Telescope)

Highlights from *ATLAS 3D R&D*

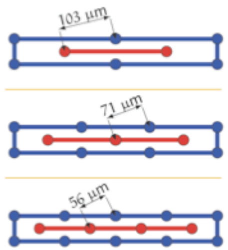
- ATLAS approved R&D project for sLHC

  "Development, testing and industrialization of full-3D active-edge and modified-3D silicon radiation pixel sensors with extreme radiation hardness for the ATLAS experiment."

- 18 participating institutes and 4 industrial partners
- Proposed by S. Parker et al.: NIM A 395 (1997) 328.



- Electrodes (both types) are processed inside the wafer bulk instead of being implanted on the wafer surface.
- Active edges: the edge of the sensor is an electrode.
- Cell configuration: 2E, 3E or 4E.



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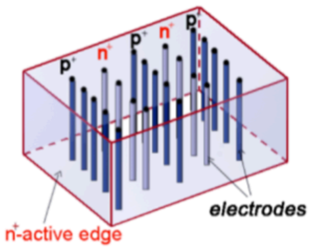
Manchester Workshop
and VCI-2010
References at page 24

- Two technologies are being studied

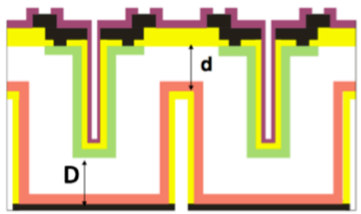
Full 3D Active Edge

3D Consortium



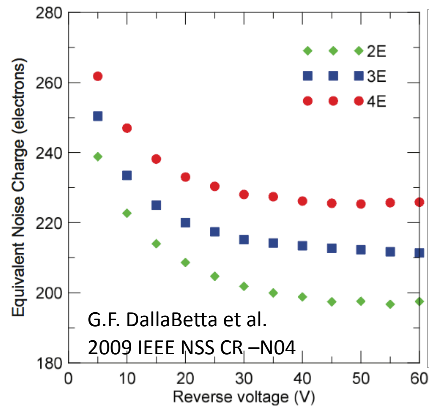
- 3DC: fabricated at Stanford and tested with ATLAS pixel readout. Design at its 5th generation.
- SINTEF: FE-I3 bump bonded sensors. FE-I4 run produced at Fall 09.

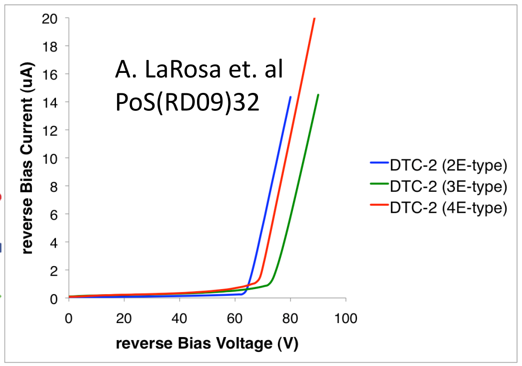
Double Side Double Type Column



- FBK/IRST:completed a FE-I3 run. Full 3D in the next run.
- CNM: being completed and bump bonded to FE-I3 (March 2010).

Signal, noise and IV curve of sensors bonded to FE-I3 chips have been studied





Highlights from *ATLAS 3D R&D*

- Strong on-going systematic rad. hard studies
  - Early studies: radiation tolerance up to 3-5 x 10^{15} n_{eq}/cm^2

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Manchester Workshop
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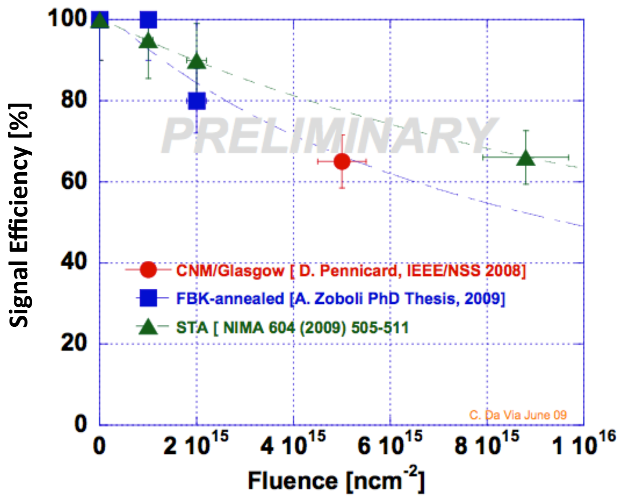
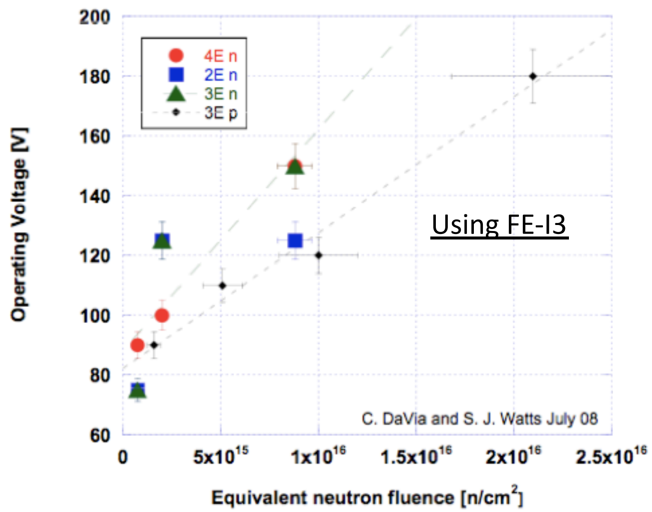
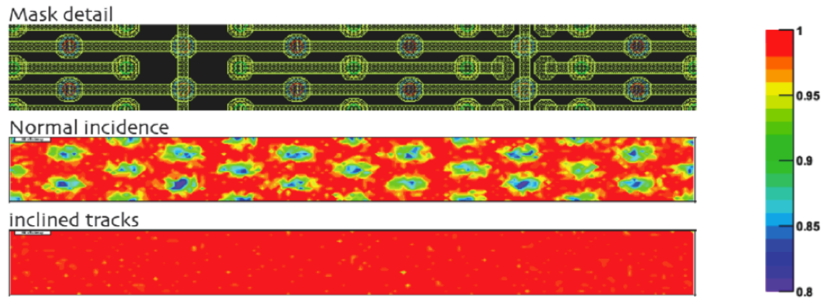
References at page 24





- Current irradiation: CERN (24 GeV protons), Karlsruhe (25 MeV protons), Ljubljana (reactor neutrons)
- June10: Test beams with irradiated assemblies

- From 2009 beam Tests
  - 1x Atlas pixel planar (as reference), 1x 3D (full column) and 2x (partial double column) have been tested in 1.6 Tesla Magnet
  - For inclined tracks 3D sensors have similar efficiency and spatial resolution as planar
    No Lorentz angle effect in 3D sensor
  - Active edge shows efficiency up
    to 5-10um form active edge



Highlights from *ATLAS DPix R&D*

- ATLAS approved R&D project for sLHC
- Participating institutes: 7 (strong collaboration with RD42)
- Original R&D proposal goals:
  - Industrialize bump bonding to diamond sensors
  - Qualification radiation tolerance
  - Optimization of front-end electronics
  - Lightweight mechanical support – exploit minimal cooling requirement
  - Aimed at tracker upgrade, bidding for IBL

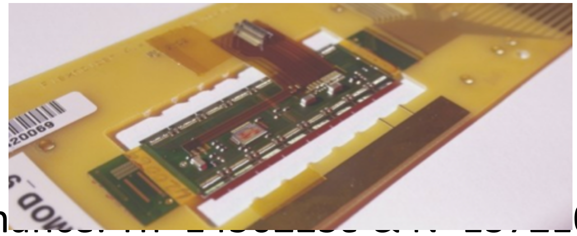
M. Mikuz and W. Trischuk
Manchester and RD42 Workshops
References at page 24

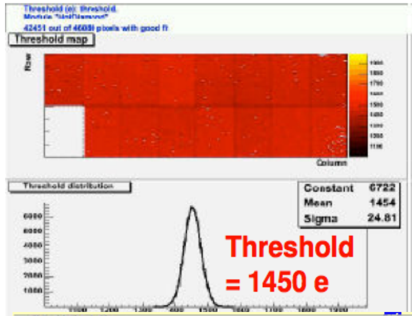
- Two producers
  - DDL and II-VI
- Diamond advantage
  - Small capacitance → low noise (140 e vs 180 e of Planar); possible lower threshold operation
  - Sensor can operate a room temperature or cold; no sensor cooling required
  - No leakage current

Property	Diamond	Silicon	
Band gap [eV]	5.5	1.12	Low leakage
Breakdown field [V/cm]	10^7	$3x10^5$	
Intrinsic resistivity @ R.T. [Ω cm]	> 10^{11}	$2.3x10^5$	
Intrinsic carrier density [cm^{-3}]	< 10^3	$1.5x10^{10}$	
Electron mobility [cm^2/Vs]	1900	1350	
Hole mobility [cm^2/Vs]	2300	480	
Saturation velocity [cm/s]	0.9(e)-1.4(h)x 10^7	0.82x 10^7	
Density [g/cm^3]	3.52	2.33	
Atomic number - Z	6	14	
Dielectric constant - ε	5.7	11.9	Low capacitance
Displacement energy [eV/atom]	43	13-20	Radiation hard
Thermal conductivity [W/m.K]	2000	150	Heat spreader
Energy to create e-h pair [eV]	13	3.61	
Radiation length [cm]	12.2	9.36	
Spec. Ionization Loss [MeV/cm]	4.69	3.21	
Aver. Signal Created / 100 μm [e_0]	3602	8892	Low signal
Aver. Signal Created / 0.1 X_0 [e_0]	4401	8323	

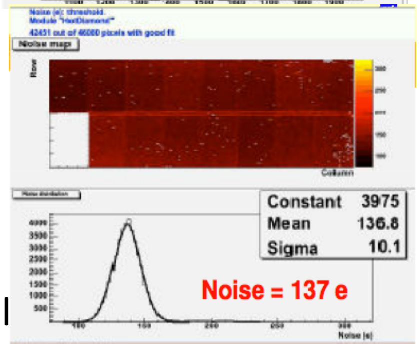
Highlights from *ATLAS DPix R&D*

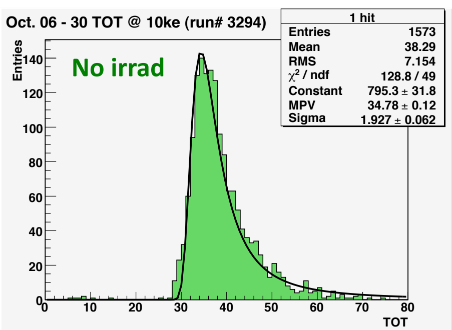
- Have assembled 3 ***pCVD*** full modules (16 FE-I3 sized)
  - 1x built at OUS, IZM and Bonn
  - 2x built in industry: all steps from polished sensor to bump-bonding performed at IZM Berlin

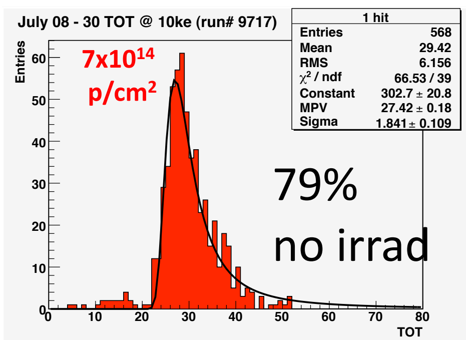


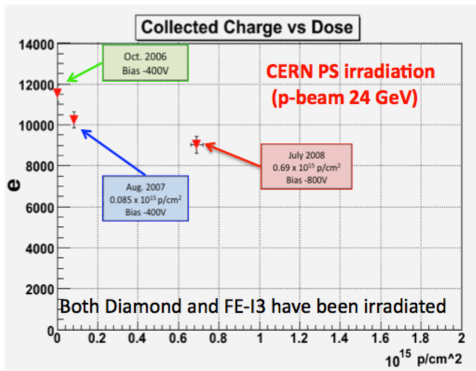


- Have also assembled few ***scCVD*** single chip modules
  - 1x FE-I3 sized tested in Lab & test beam before and after irradiation ($7x10^{14}$ p/cm^2)
  - 6x ¼ FE-I3 sized (processed at IZM w/ their standard pixel metallization)
  - Irradiation test: Karlsruhe (25 MeV protons), CERN (24 GeV protons) and PSI



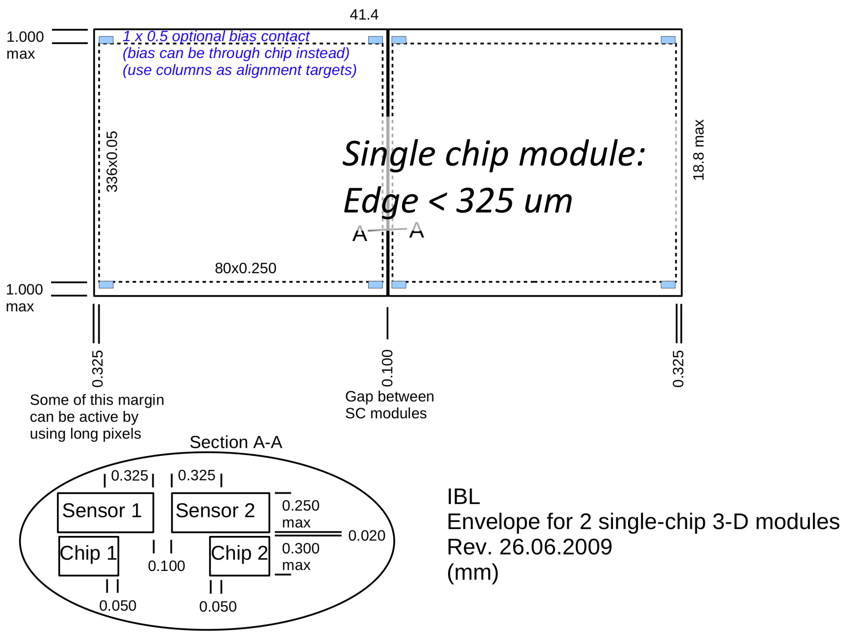


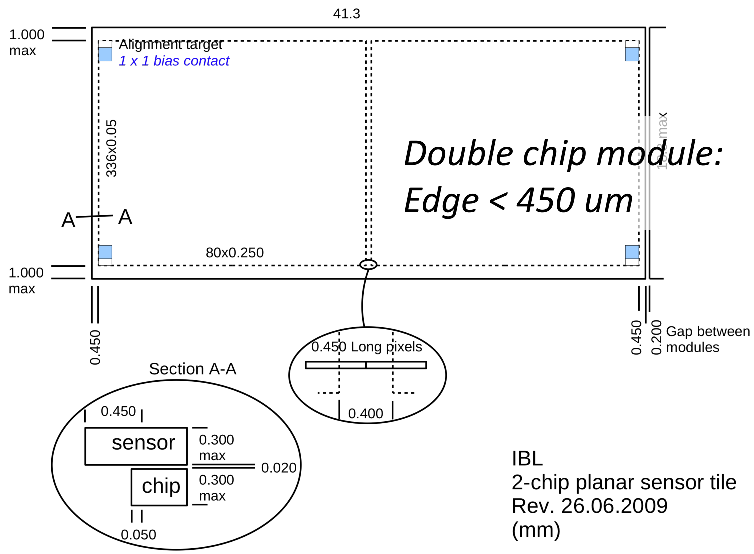




IBL Module Design

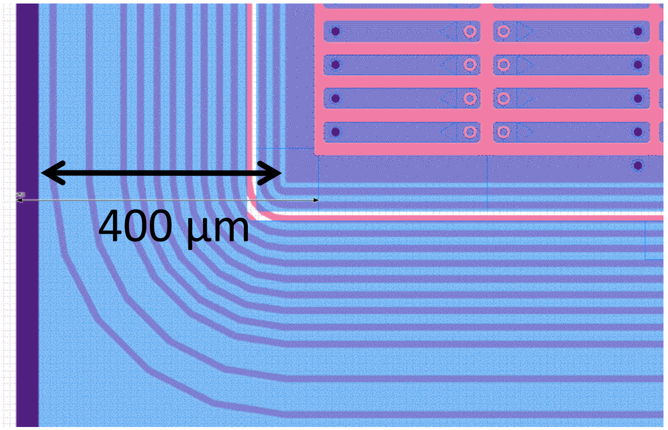
- Sensor technology independent
- Decision on sensors after prototyping with FE-I4
  - Need module prototypes with FE-I4 (full 2010)
  - Will produce qualification modules with Planar, 3D and Diamond sensors this year as soon as we get FE-I4's
- Common sensor baseline for engineering and system purposes
  - 3D / Diamond sensors → Single chip modules
  - Planar sensors → Two chip module
- Sensors/module prototype for ~10% of the detector in 2010



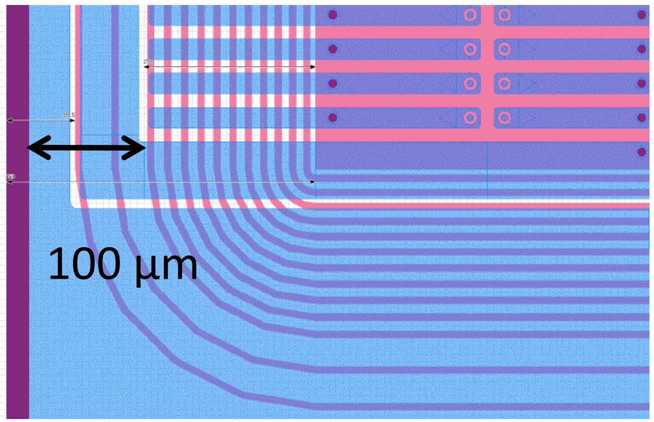


Sensors: Planar-Si

- Two **N-in-N** designs with different guard ring structures:
  - ***Design A***: 450 µm wide guard ring structure regarded as conservative design

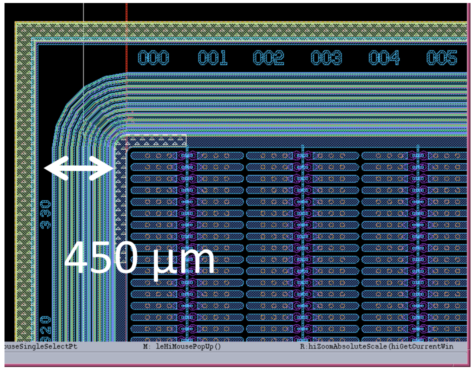


  - ***Design B***: more aggressive slim edge design with only 100 µm wide inactive area by shifting the guard ring structure under underneath the active pixel area



Sensors: Planar-Si

- **Thin N-in-P** design
  - Utilize the advantages of thinned sensors at given maximum bias voltage
  - Standard 450 µm wide inactive area
  - Special passivation layer for HV operation



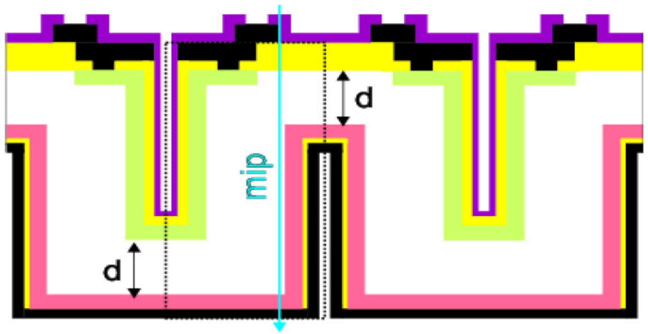
→ *All 3 designs will be available for prototyping in 2010:*

- ***N-in-N*** designs are build by CiS and are already partly at IZM for bump bonding
- ***N-in-P*** design was successfully tested with CiS run and will be produced at HLL Munich on 6” wafer (will be thin)
- Both single and 2-chip sensor will be available for module prototyping
- 60 single-chip & 30 double chip module

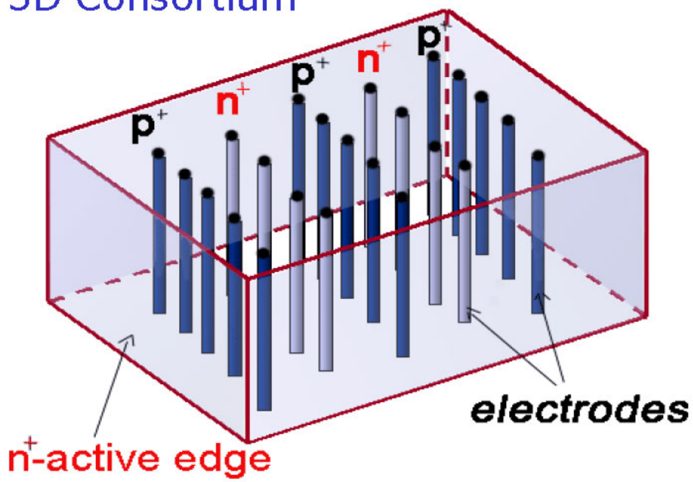
Sensors: 3D-Si

- Two designs with equivalent electrical performance:
  - Full 3D active edge design – *preferred option*
  - Double column design – *200 µm slim edge*
  - N-in-P design with 230 µm sensor thickness
  - 10-14 µm hole diameter
  - Both design are currently under fabrication at different foundries
    - Stanford / SLAC
    - Sintef
    - FBK-irst
    - CNM

Double Column Design

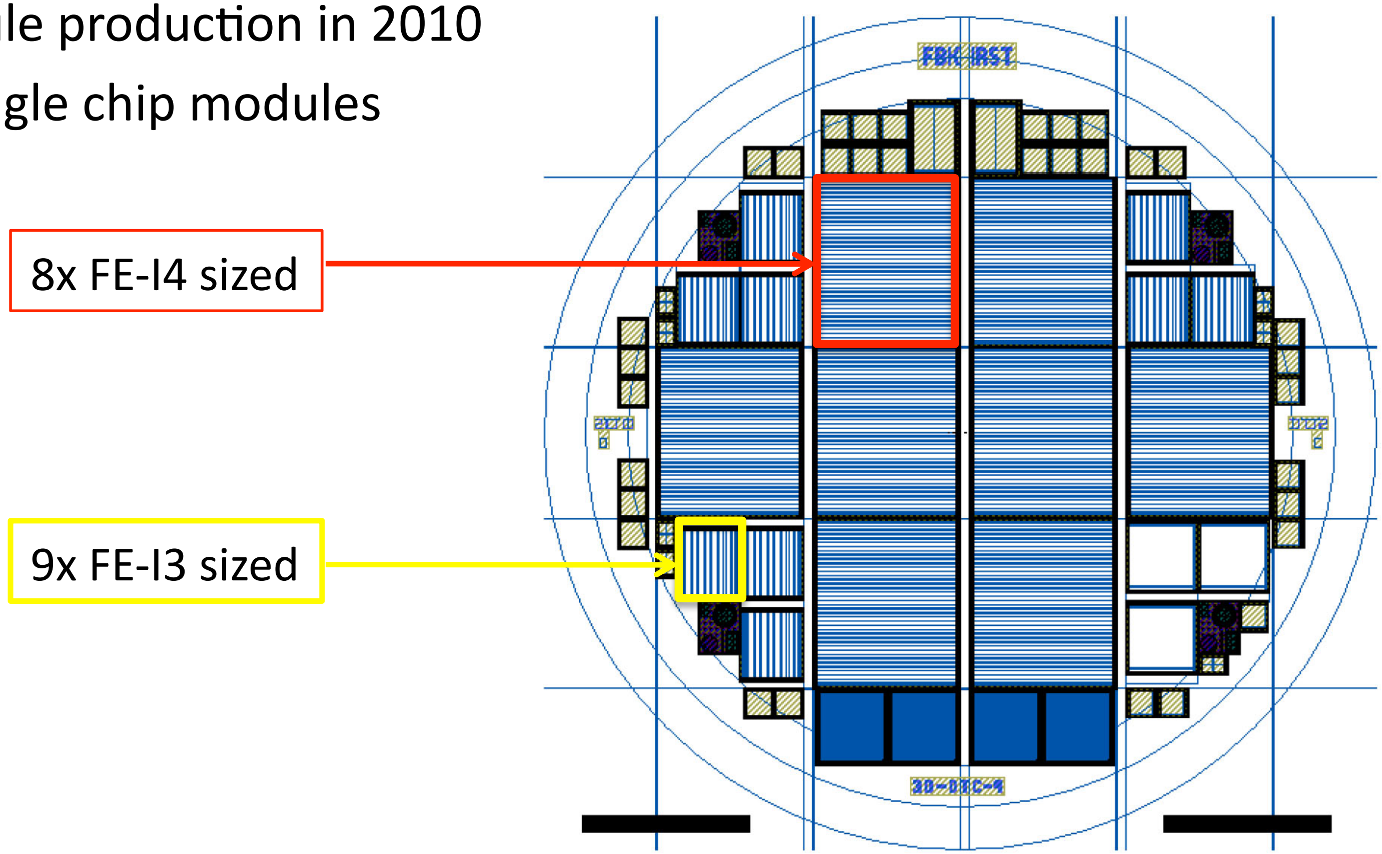


Full 3D Active edge
3D Consortium



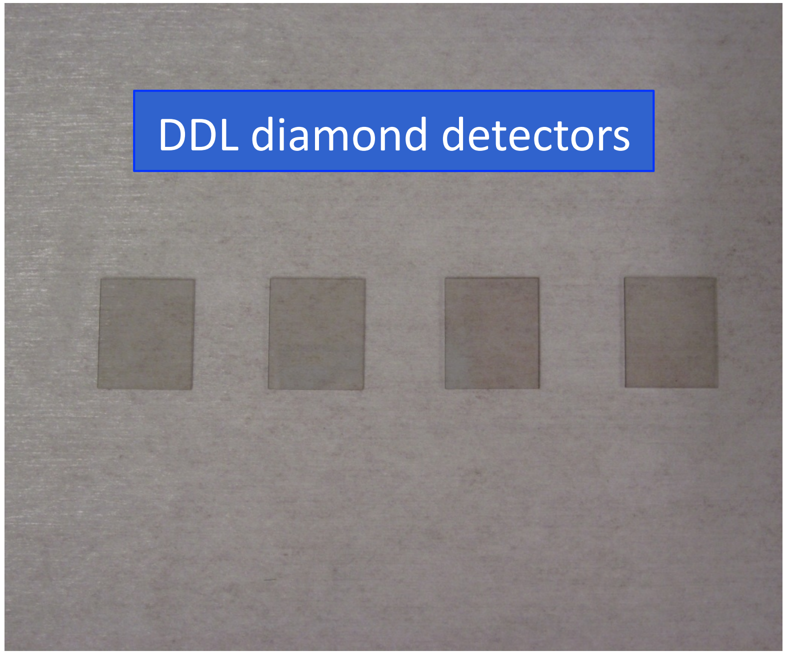
Sensors: 3D-Si

- Common floor plan wafer design:
  - Featuring 8x FE-I4 and 9x FE-I3 single chips
  - Will use a common bumping mask
  - Sensor fabrication was started and sensors will be available for prototype module production in 2010
  - 60 single chip modules



Sensors: Diamond

- Diamond sensors from the long term RD42 vendor DDL:
  - Already 6x FE-I4 sized sensors available
  - Measured CCD between 240 and 260 µm
  - Possible 2+2 more sensors to order
  - Can use already delivered FE-I3 module sized sensors either for FE-I4 single chip sensors over 2 chip sensors
  - Sensor metallization will be done at IZM by putting the UBM on.

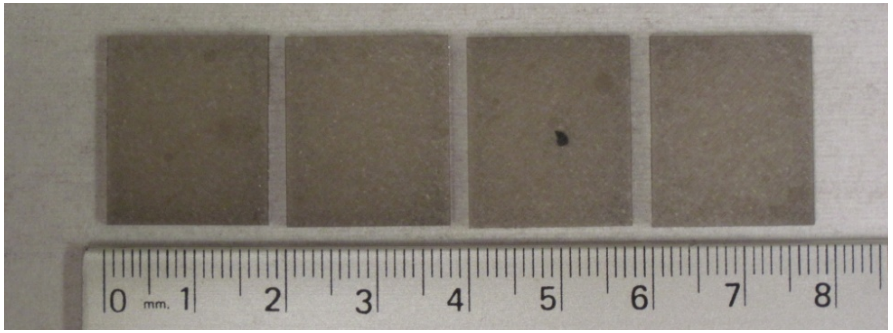


Sensors: Diamond

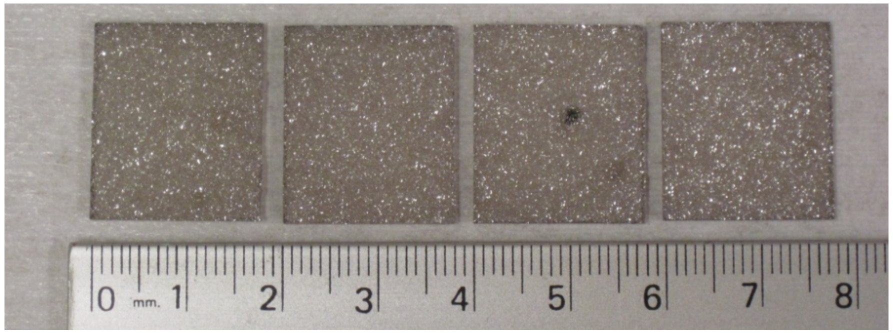
ATLAS EXPERIMENT

- Recently a new diamond supplier came into the focus II-VI
  - Already 4x FE-I4 sized sensors delivered for tests
  - Surprisingly good results although growth process not optimized for radiation detectors: CCD=220-230 µm at 0.7 V/µm
  - Still more work needed for vendor qualification but looks very promising
  - Pixel metallization process will be done at IZM as for DDL detectors

II-VI diamond detectors



Substrate side

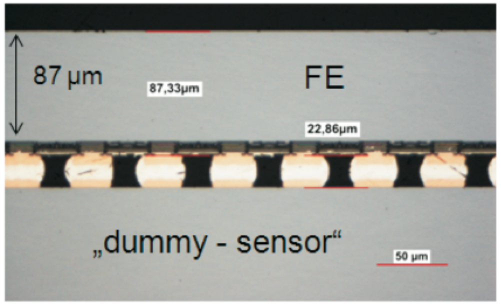


Growth side

→ Sensor available from DDL and II-VI: 20x Single Chip

Bump Bonding

- General requirements for the bump bonding process for IBL module are:
  - a fine bump pitch of 50 µm
  - a high bump density of 80 bumps per mm^2 (or 26 880 bumps per readout IC)
  - a high yield with a defect rate < 10^{-4}
- Large volume bump bonding experience from ATLAS Pixel Detector (ATLAS Pixel BB production – *Jinst 3 P07007 (2008)*)
- Program to qualify for FE-I4 and different sensor technologies
  - Goal to go below 190 µm of Pixel detector: target to 90 µm



Cross-section of a flip chipped test assembly of FE-I4 size thinned down to 90 µm using solder bump technology at IZM Berlin.

Jinst 3 P07007 (2008)

	Indium		PbSn		Total	
	Modules	Fraction	Modules	Fraction	Modules	Fraction
Assembled	1468		1157		2625	
Rejected	172	11.7%	35	3.0%	207	7.9%
Accepted (total)	1296	88.3%	1122	97.0%	2418	92.1%
Accepted as delivered	1101	75.0%	1035	89.5%	2136	81.4%
Accepted after reworking	195	13.3%	87	7.5%	282	10.7%

The BB technology has to compatible with the different proposed sensor options:

+ Current Pixel planar n-in-n detector was used & showed to be compatible with solder and Indium BB tech.
+ 3D-Si sensors was BB to FE-I3 at IZM and Selex
+ Diamond was BB to FE-I3 at IZM Berlin

Technology in use within HEP community

Bump technology	Vendors	Status
Solder (SnAg or PbSn)	IZM Berlin (Germany) RTI (USA) VTT (Finland)	Used for ATLAS, CMS & ALICE Pixel; Experience with big and thin chips
Indium	Selex (Italy)	Used for ATLAS Pixel
Indium with reflow	PSI (Switzerland)	Used for CMS Pixel
Solid Liquid Interdiffusion (SLID)	IZM Munich (Germany)	First dummies produced
DBI Oxide Bonding	Ziptronix (USA)	First tests with 3D-Integration
Glue Injection Mirco-Bonding	ZyCube (Japan)	First tests with 3D-Integration

2010/11 Module qualification program

- Main focus on test preparation for FE-I4 based on USBPix System
- **Two Batches** of IBL qualification module with two goals:
  - Batch 1: Demonstrate that FE-I4 works with sensors (thick chip, minimal risk on bump bonding, likely all single chip module) – start bonding mid August
  - Batch 2: Demonstrate IBL module specs (thin chip, production experience, 2 chip modules for planar) – start bonding early September
- Batch 1 test results available in Dec 2010/Mar 2011
  - Need to make best possible use of test beam time and irradiations
  - Information available for sensor and chip performance (irradiation)
- Batch 2 test results available in May/ Jun 2011
  - Need to look for irradiation and test beam outside CERN
  - This is the time when we have the full module info (i.e. including production experience with final module specs)

IBL Status and Outlook

- IBL project is the upgrade for the ATLAS Pixel Detector in LHC phase-I upgrade
- A 4^{th} layer is to be included into the Pixel system
- Radiation tolerance of electronics and sensors is under investigation
- Many R&D items have been started in all the components needed
- Aim is to be ready for installation in 2014

References (ATLAS Pixel R&D projects)

- **PLANAR-Si Pixel**
  - https://twiki.cern.ch/twiki/bin/view/Atlas/PlanarPixelUpgrade
  - http://agenda.hep.manchester.ac.uk/contributionDisplay.py?contribId=15&sessionId=4&confId=1181
  - http://indico.cern.ch/conferenceDisplay.py?confId=88492

- **3D-Si Pixel**
  - https://twiki.cern.ch/twiki/bin/view/Atlas/PixelUpgrade3D
  - http://agenda.hep.manchester.ac.uk/contributionDisplay.py?contribId=40&sessionId=12&confId=1181
  - http://indico.cern.ch/getFile.py/access?contribId=126&sessionId=9&resId=0&materialId=slides&confId=51276

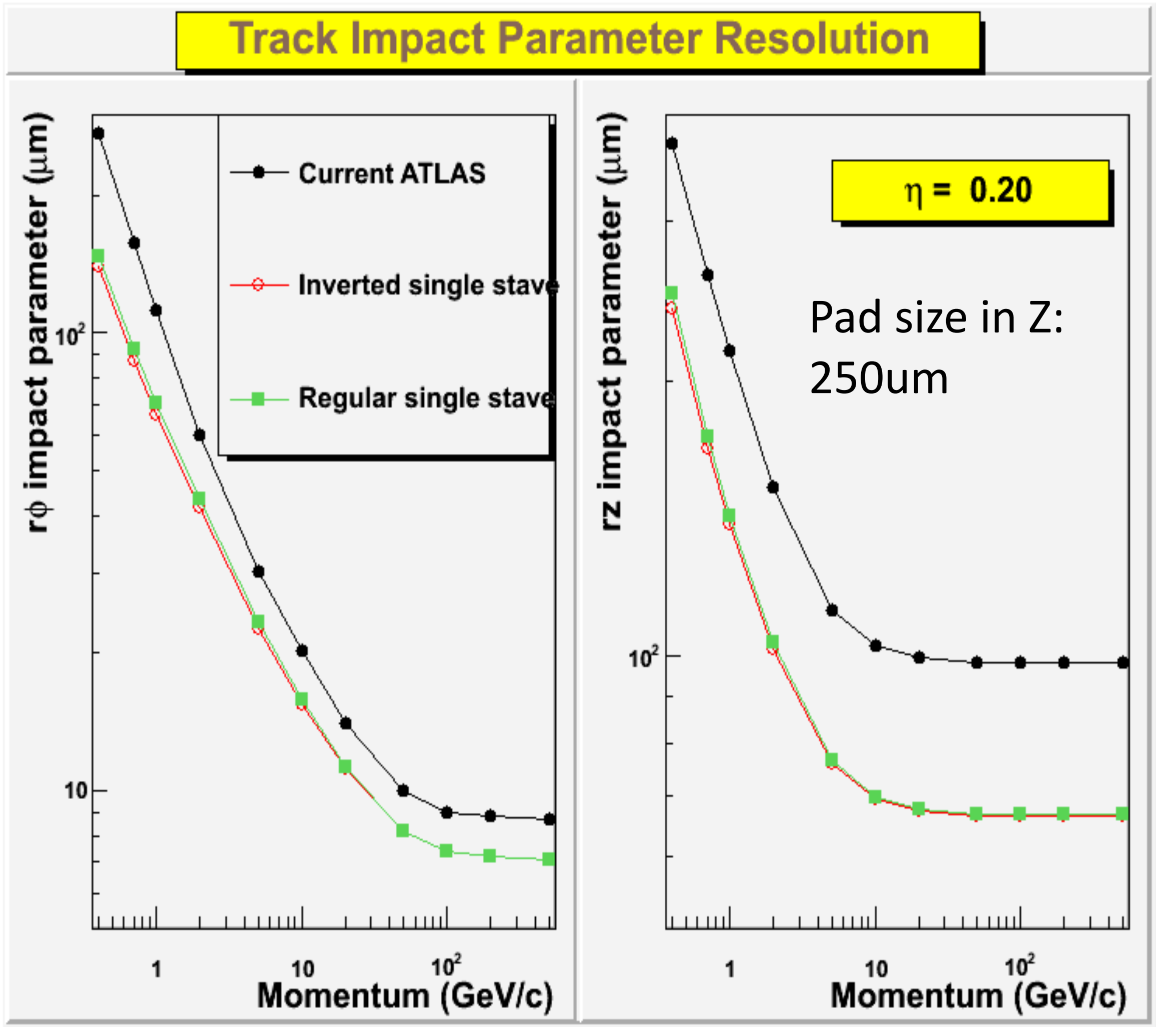
- **CVD Diamond Pixel**
  - http://indico.cern.ch/categoryDisplay.py?categId=1322
  - http://agenda.hep.manchester.ac.uk/contributionDisplay.py?contribId=26&sessionId=8&confId=1181
  - http://indico.cern.ch/conferenceDisplay.py?confId=93151

BACKUP SLIDES

Track Impact Parameter Resolution

- Improvement of IP resolution:
  - Z 100um → ~ 60um
  - RΦ: 10um → ~7um
- b-tagging: Light jet rejection factor improves by factor ~2
- To maintain Pixel Detector performance with inserted layer, material budget is critical

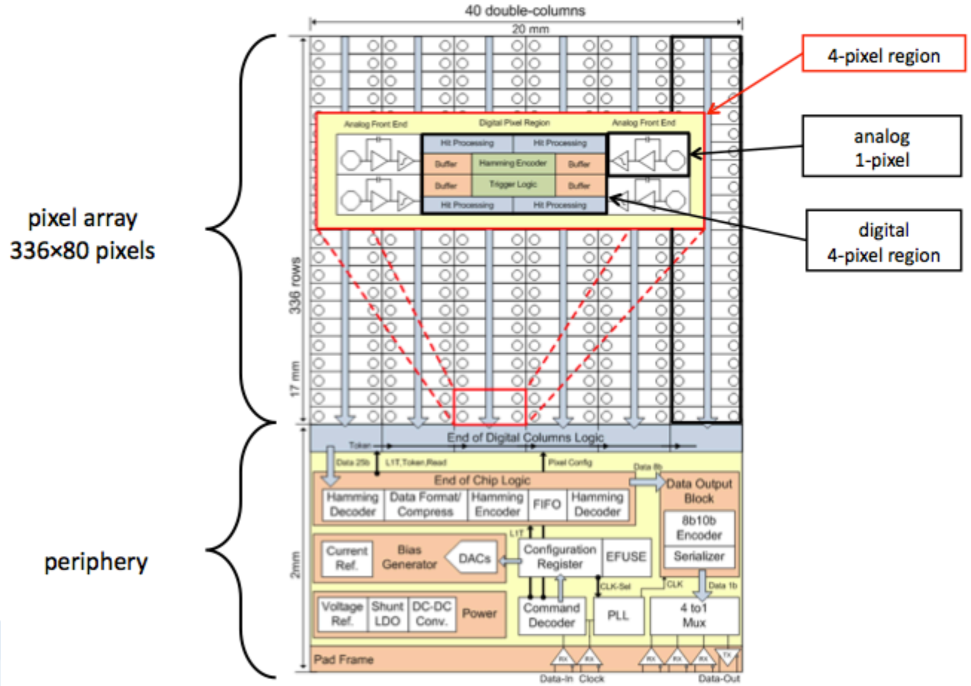
Component	% X_0
beam-pipe	0.6
New-BL @ R=3.5 cm	1.5
Old BL @ R=5 cm	2.7
L1 @ R=8 cm	2.7
L2 + Serv. @ R=12 cm	3.5
Total	11.0

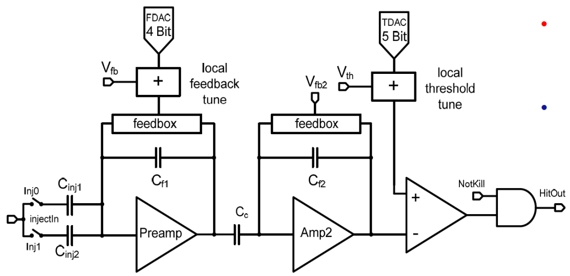


The readout IC: FE-I4

Specifications	Value	Unit	Conditions/comments
Pixel size	50 x 250	μm²	
Bump pad opening	12	μm	diameter
Input	-Q		DC coupled
Maximum charge	100,000	e	
DC leakage current tolerance	100	nA	
Pixel array size	80 x 320	Col x Row	
Last bump to physical edge	≤ 100	μm	
Normal pixel input capacitance range	100÷500	fF	
Edge pixel input capacitance	150÷700	fF	Sides for long pixels and top for ganged
Radiation tolerance	250	Mrad	Specs met at this dose
In-time discriminator threshold with 20 ns gate and 400 fF load	≤5000	e	Region can still assign small hits below in-time threshold to correct time bin

Specifications	Value	Unit	Conditions/comments
Hit-trigger association resolution	25	ns	
Same pixel two-hit discrimination	400	ns	At 5000 e in-time threshold and when both hits are 20 ke
Single channel ENC sigma	<300	e	400 fF load, nominal current
Tuned threshold dispersion	<100	e	sigma
Charge resolution	4	bits	
ADC method	ToT		
Average hit rate with 1% data loss	400	MHz/cm²	3.2 μs trigger latency, 100 kHz trigger rate
Max number consecutive triggers	16		
Trigger latency (max)	6.5	μs	
Maximum sustained trigger	200	kHz	
Serial command/clock input	40	Mb/s - MHz	1 + 1 input per chip
Serial data output	160	Mb/s	1 output per chip
Output data encoding	8b/10b		
I/O signals	~LVDS		Current balanced differential



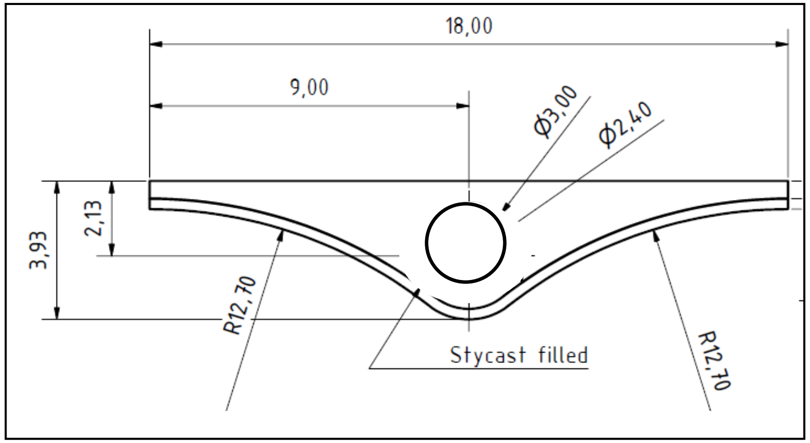


2-stage architecture optimized for low power, low noise, fast rise time.

- regular cascode preamp. NMOS input.
- folded cascode 2nd stage PMOS input.
- Additional gain, C_c/C_{f2} ~6.
- 2nd stage decoupled from leakage related DC voltage shift.
- C_{f1} ~17 fF (~4 MIPs dynamic range).

Stave: design baseline

- The choice of the CO_2 coolant led to drop several design options and allowed set the stave baseline.
- It is Koppers KFOAM based, with 2mmID x 120um Ti pipe. The structural stiffness is provided by a cyanate ester laminate $[0/60/-60]_{S2}$ YS-80/EX1515.
- The main parameters are collected in the table where it is still considered the CF pipe stave. This option is actually at low priority and it is meant to go through the qualification process only.



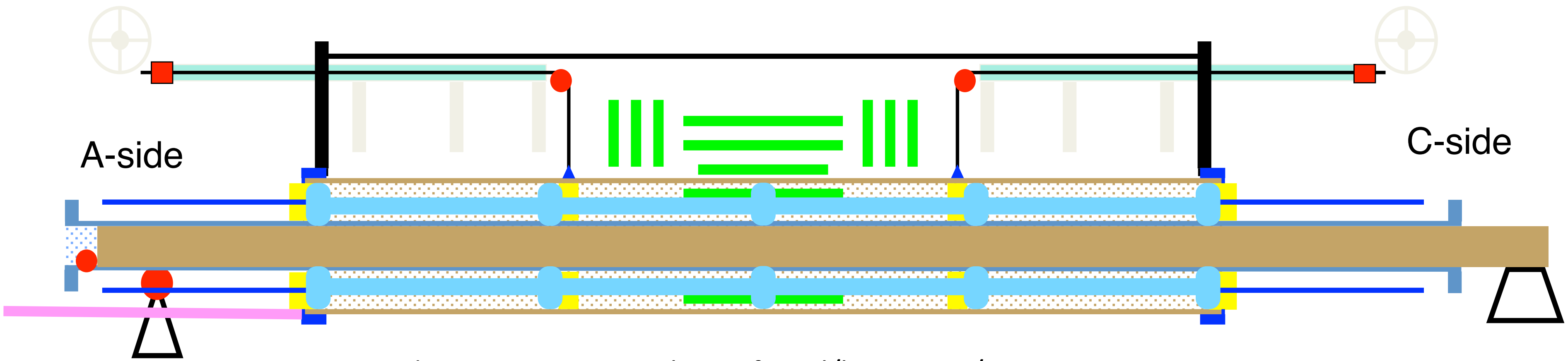
- The conductive thermal figure of merit has been measured directly on a stave sample.
- The deformation induced by the cool down is from a FEA analysis.

STAVE TYPE	Omega Thickness [μm]	Foam Density [g/cm³]	Pipe Material	Pipe Diameters [mm]	Radiation Length X/X_0 [%]		Thermal Figure of Merit G [°C.cm²/W]	Thermal Def. [mm]
					Bare Stave	Full Stave Assembly		
Ti pipe Stave	300	0.25	Ti grade II	ID=2 OD=2.2	0.57	1.166	11	41
CF Pipe Stave	150	0.25	CF	ID=2.4 OD=3	0.36	0.956	25	50

Ref: D. Giugni – AUW, DESY 21th Aptil 2010

Installation

- Procedure studied on mock-up at CERN Bat. 180
  - The beam pipe flange on A-side is to close to the B-Layer envelope – Need to be cut on the aluminum section
  - A structural pipe is inserted inside the beam pipe and supported at the both side
  - The support collar at patch panel PP0 A-side is disassembled and extracted with wires at PP1
  - Beam pipe is extracted from the C-side and it pulls the wire at PP1
  - New cable supports are inserted inside Pixel Support Tube (PST) at PP0
  - A support carbon tube is pushed inside the PST alone the structural pipe



Started to setup a 1:1 mock-up of Pixel/beampipe/PP1 in Bat 180