Associative Memory design for the Fast TracK processor (FTK) at Atlas

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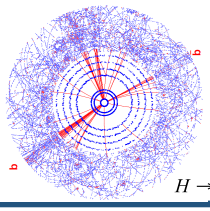
The ATLAS Luminosity



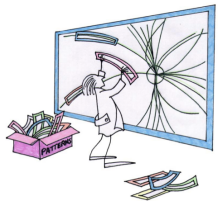
The existing ATLAS trigger does the needed track reconstruction in the level-2 farm, which will work well up to LHC design luminosity of 1×10^{34} (figure).

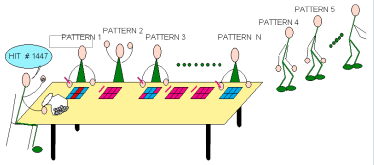
•At SLHC Phase I luminosity should be improved of a factor 3, increasing the need for fast and powerful tracking system.

$H \rightarrow b\bar{b}$ at LHC

Pattern Recognition using Associative Memory (AM)

A large bank of pre-computed low resolution tracks (roads) is used for very fast tracking.

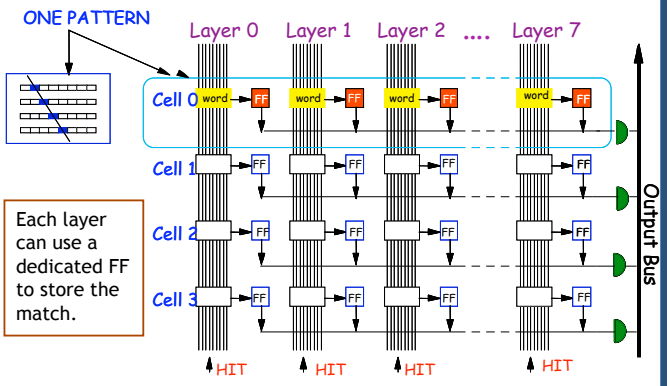




✓ AM [1] finds tracks during detector readout

✓ Full resolution tracks (near offline quality) are extrapolated using fast track techniques inside the roads [2], where linearized fit can be performed.

AMChip Core



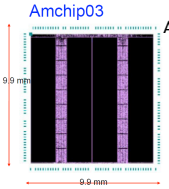
Each layer can use a dedicated FF to store the match.

Parallel comparison between the incoming hit coordinates with the stored patterns.

Ability to correlate data received at different times.

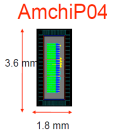
Fast response and high flexibility in data reception

90 nm Miniasic & Full custom



Amchip03 built with 180 nm technology [1]

(Std-cell design)

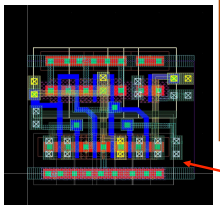


Currently working at CDF

New 90 nm Miniasic prototype (Full-custom core)

How to improve by a factor 2 pattern density while keeping consumption under control

1.Full custom

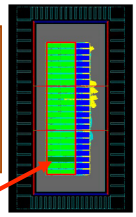


Each full custom layer become a new standard cell:

- ➢ std cell costraints & rules
- ➢Model for behavioral simulation
- ➢Model for timing simulation

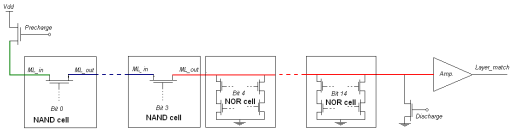
Layout of a NAND CAM cell

32x8 layers in each block



Full custom cells cover the green region

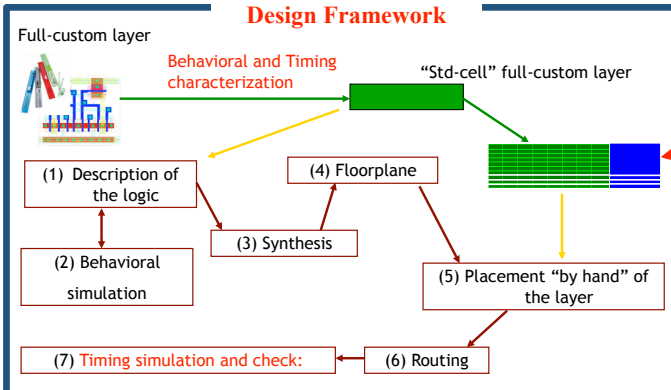
2. Power saving technique: selective precharge [3]



Mixing NOR and NAND cell: the Match-line is precharged ONLY if the first 4 bits have a match.

Power reduction of factor 3

Design Framework



History and perspective

What is now in CDF :

- ➢180 nm technology
- ➢40 MHz clock frequency
- ➢1x1 cm area
- ➢5 Kpattern/chip with 6 Layers
- ➢Core voltage 1.8V

What's new in AmchiP04	Effect
90 nm technology	reduction of pattern area (1/4)
Full custom	reduction of pattern area (1/2)
Up to 1.5x1.5 cm area	more area avaible but higher consumption
100 MHz clock frequency	faster but higher consumption
Core voltage 1V	reduction of power consumption
Selective precharge	reduction of power consumption (1/3)

We could reach density of about 60 Kpattern/chip with 8 layers mantaining roughly the same power consumption (less than 2 W/chip)!!

[1] A VLSI Processor for Fast Track Finding Based on Content Addressable Memories. A Annovi et al. IEEE Transactions on Volume 53, Issue 4,Page(s):2428 - 2433

[2] The GigaFitter: Performance at CDF and Perspectives for Future Applications. S Amerio *et al* 2010 *J. Phys.: Conf. Ser.* 219 022001

[3] Content-Addressable Memory (CAM) Circuits and Architectures: A Tutorial and Survey. K Pagiamtzis and A Sheikholeslami. IEEE journal of SSC, Vol.41, N.3, 2006.

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