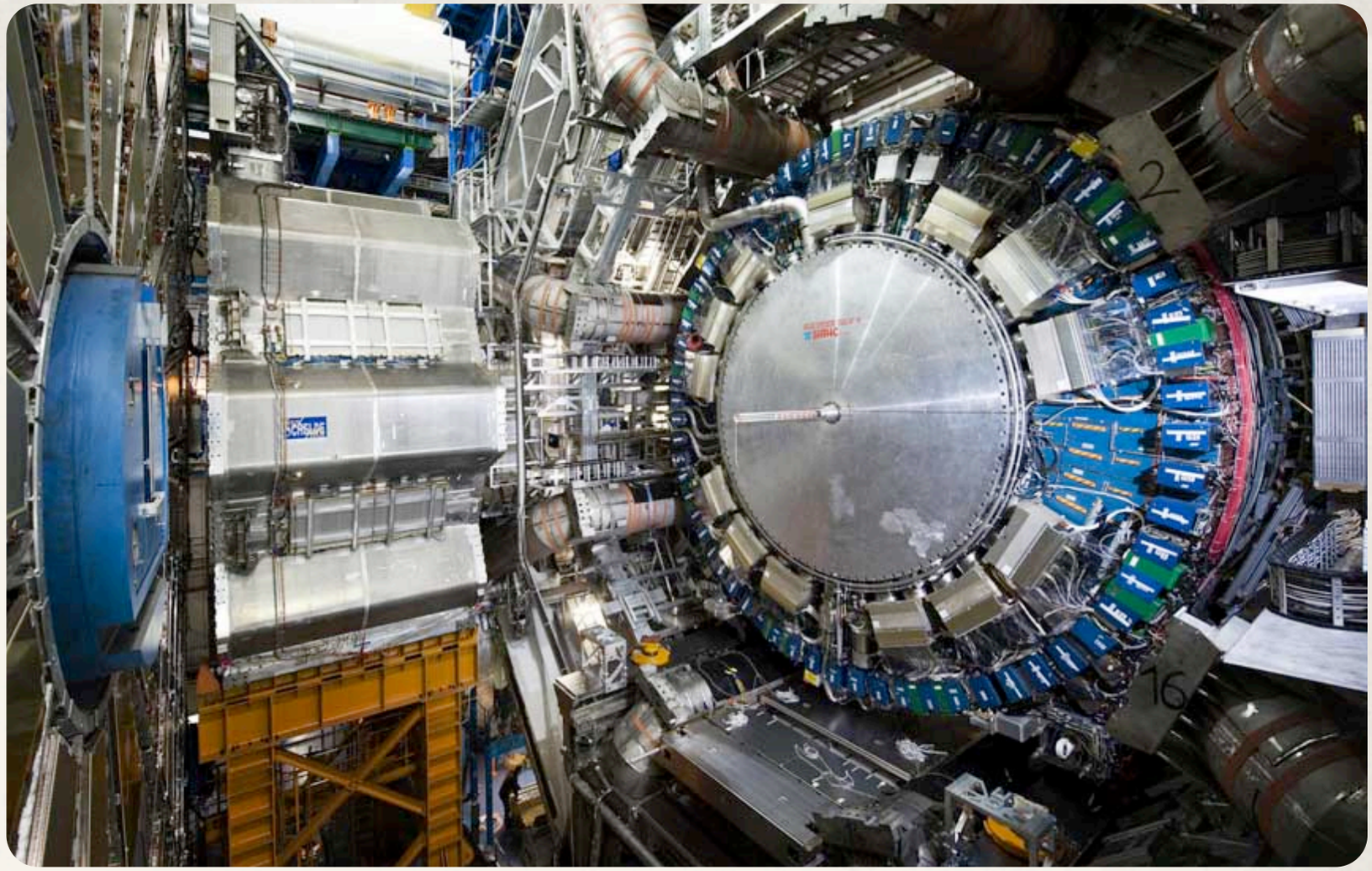


ATL-LARG-SLIDE-2010-079
23 May 2010

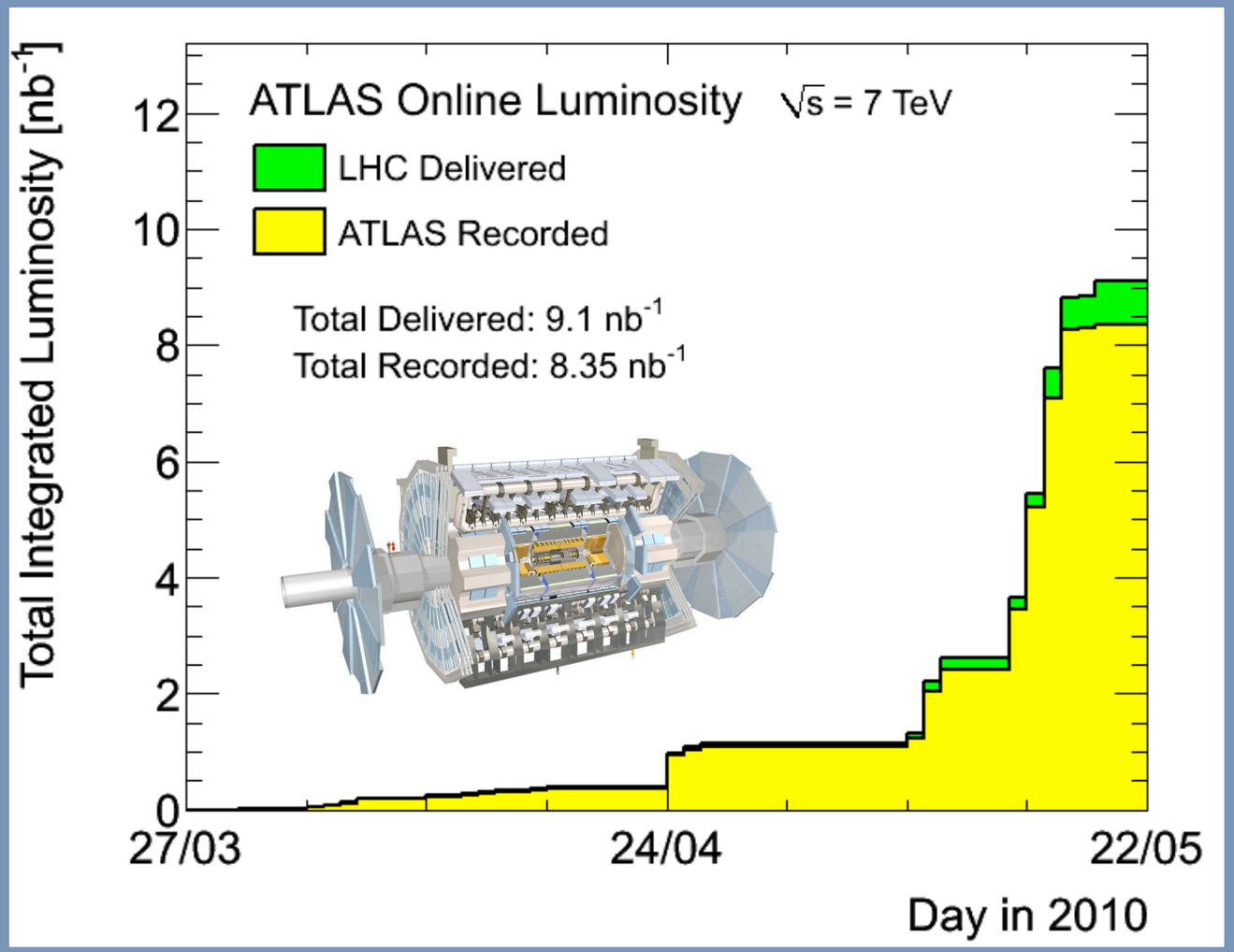
Electronic Readout of the ATLAS Liquid Argon Calorimeter: Calibration and Performance

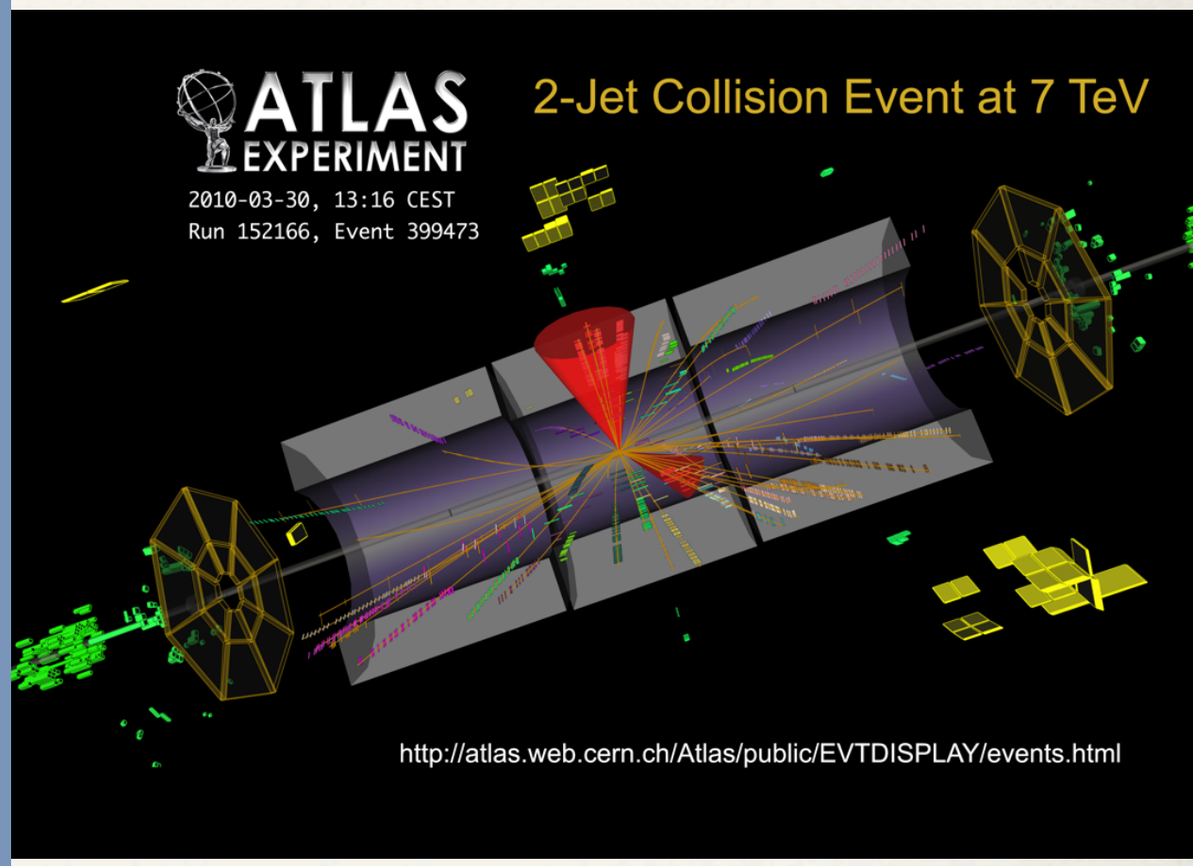
Stephanie Majewski, Brookhaven National Laboratory,
on behalf of the ATLAS Liquid Argon Calorimeter Group

25 May 2010, IEEE RealTime 2010, Lisbon, Portugal

BROOKHAVEN NATIONAL LABORATORY

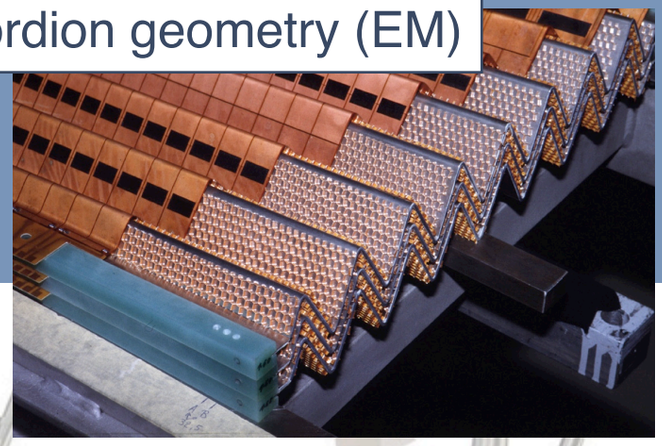
LHC and ATLAS Performance

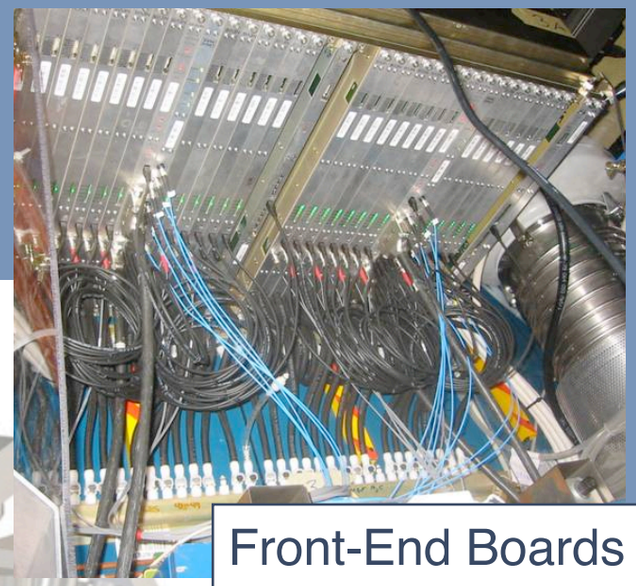




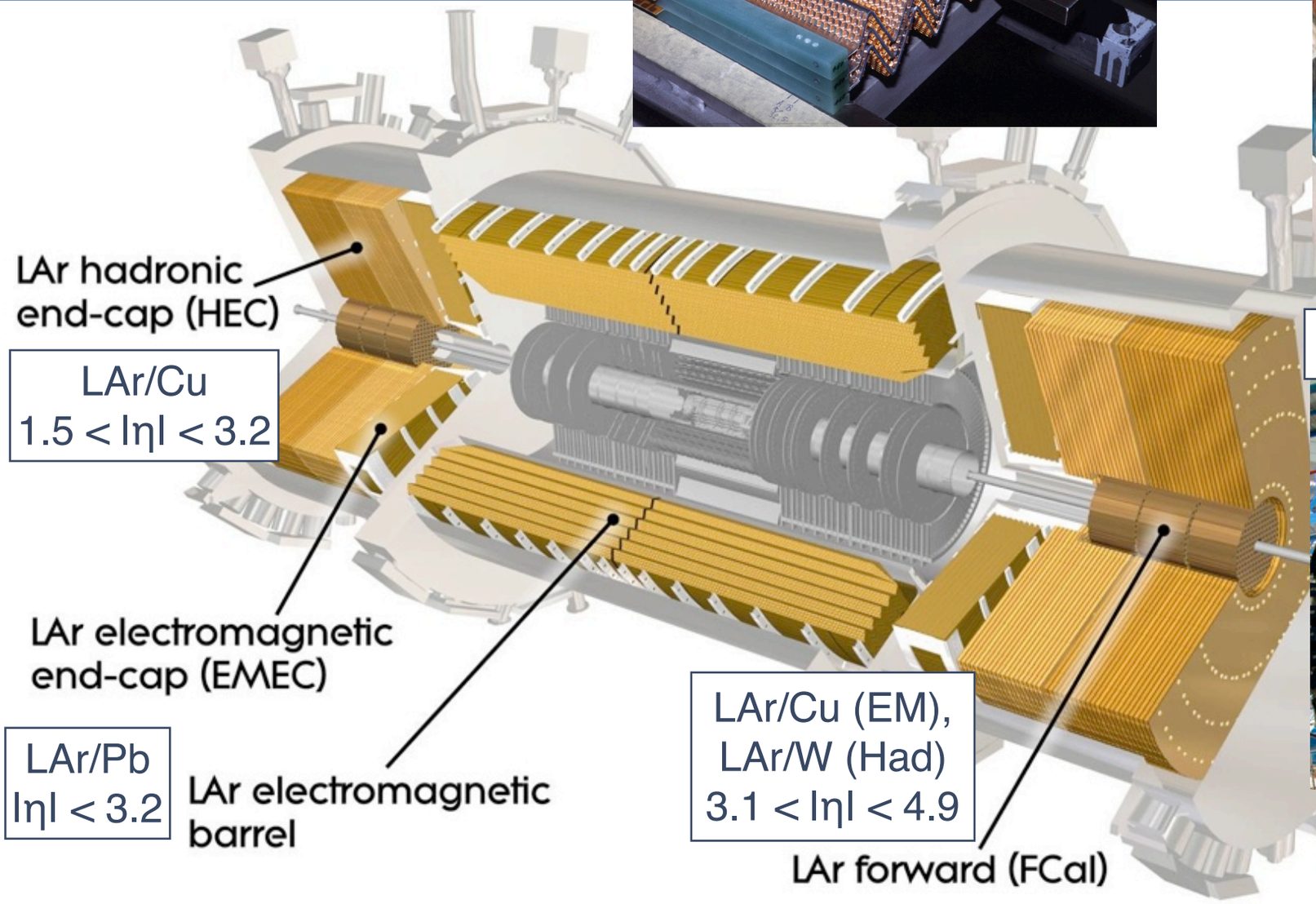
Subdetector	Number of Channels	Approximate Operational Fraction
LAr EM Calorimeter	170 k	98.5%
Hadronic endcap LAr calorimeter	5600	99.9%
Forward LAr calorimeter	3500	100%
LVL1 Calo trigger	7160	99.8%

Accordion geometry (EM)

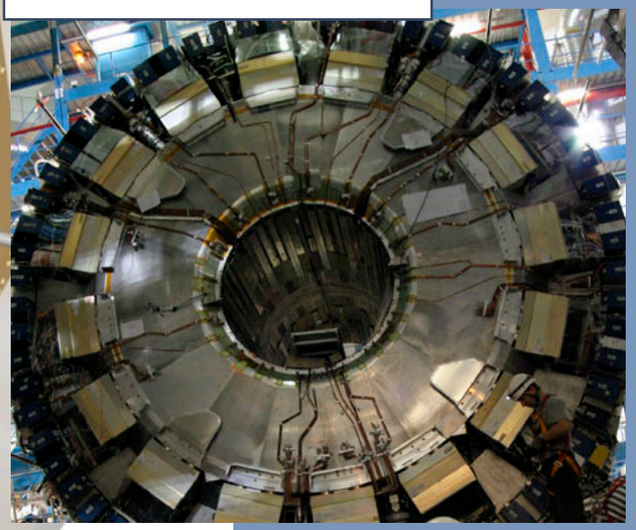




Front-End Boards



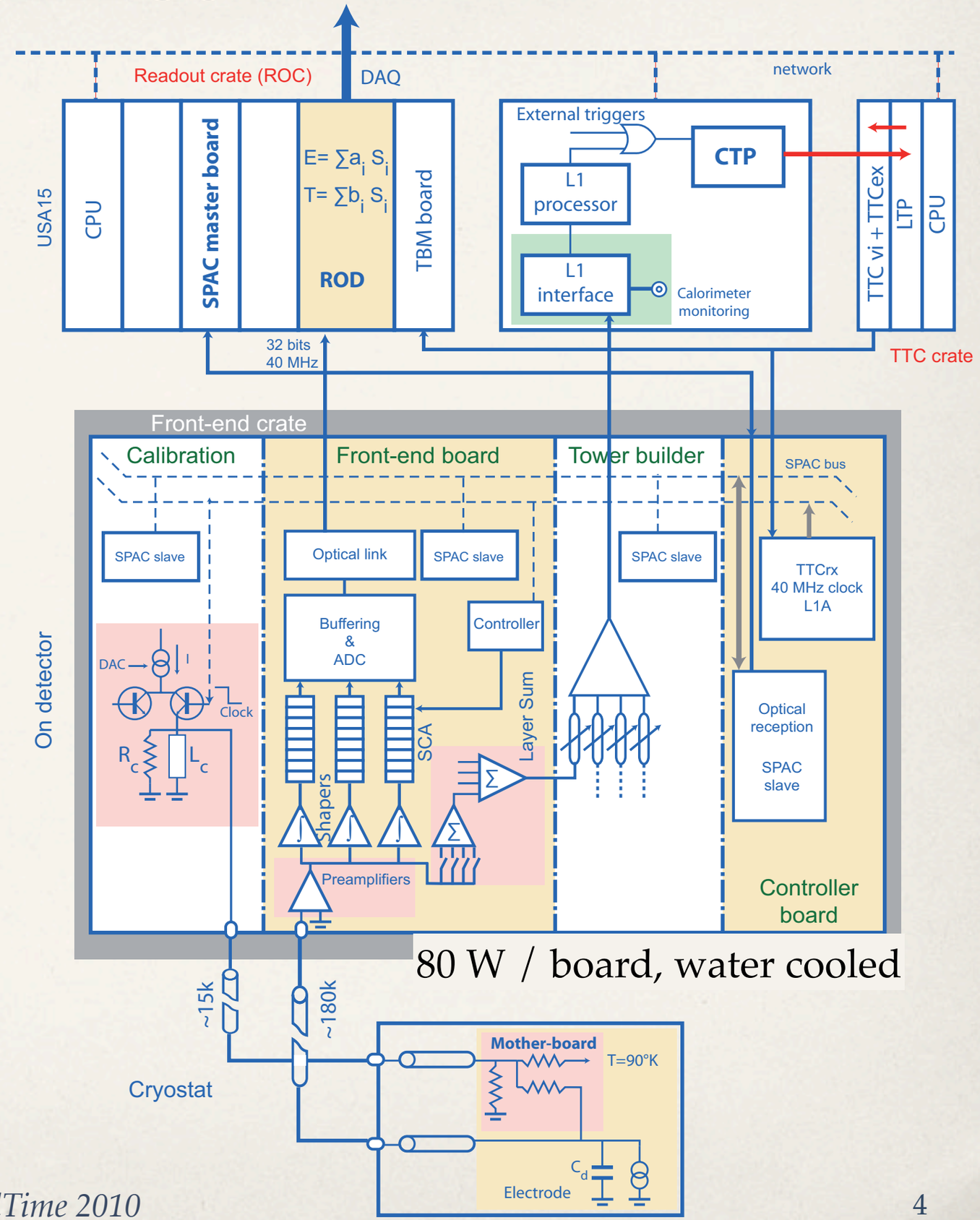
Front-End Crates



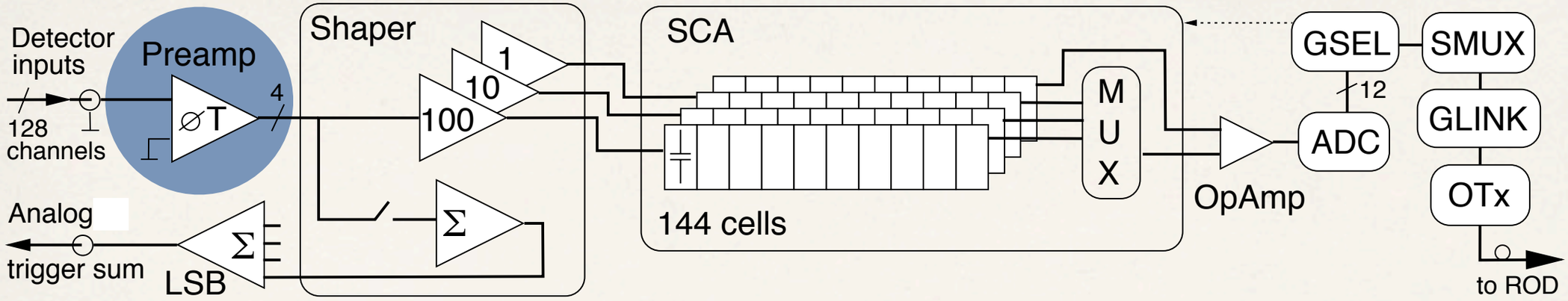
ATLAS Liquid Argon Calorimeter

Readout Electronics

- Goal: Measure the energy in **182,468 detector channels** over a wide dynamic range (tens of MeV – ~few TeV)
- Front-end electronics:
  - 1524 front-end boards read out + digitize calorimeter signals
  - ~300 other boards (calibration, analog trigger sums, controllers, monitoring)
  - 1524 fiber optic links (1.6 Gbps) to BE
- Back-end electronics:
  - 192 Read-out driver (ROD) boards provide digital filtering, formatting, and monitoring
  - ~800 optical links to ATLAS DAQ



Front-end Board Architecture

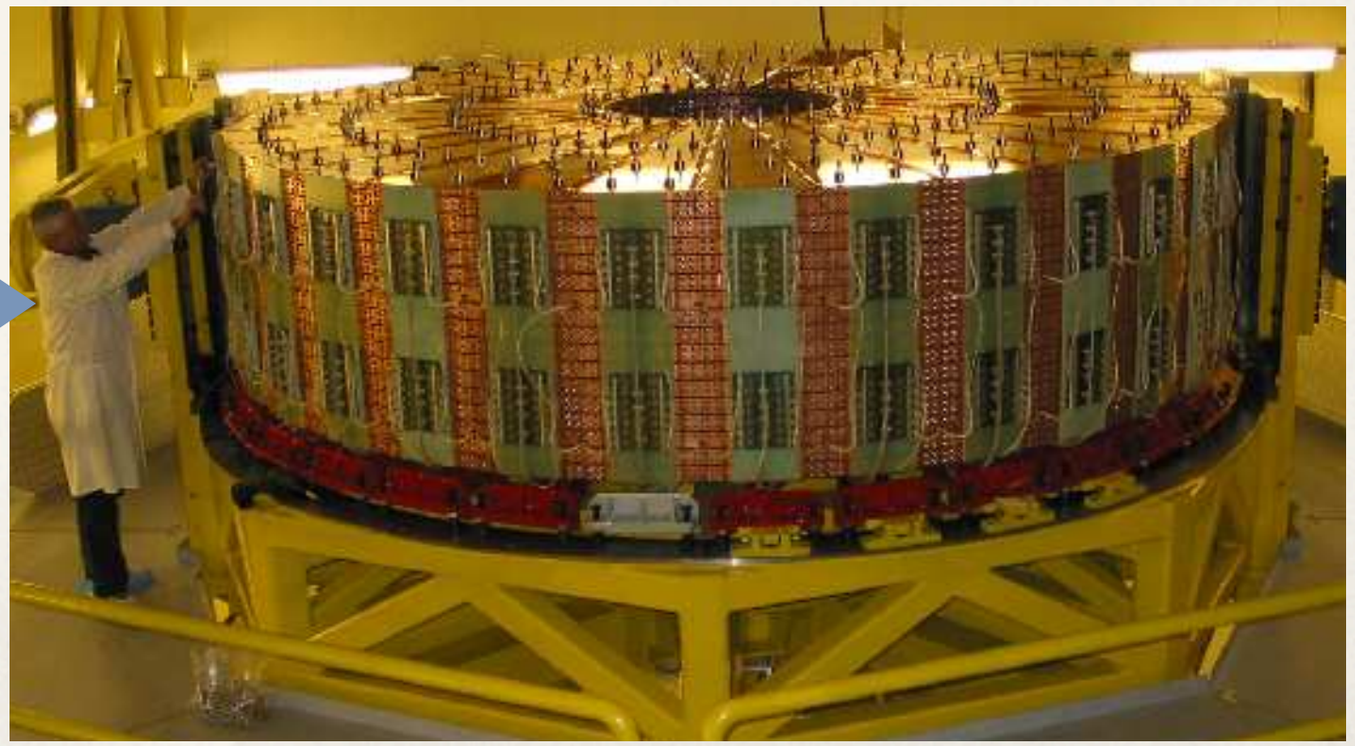


Preamp:

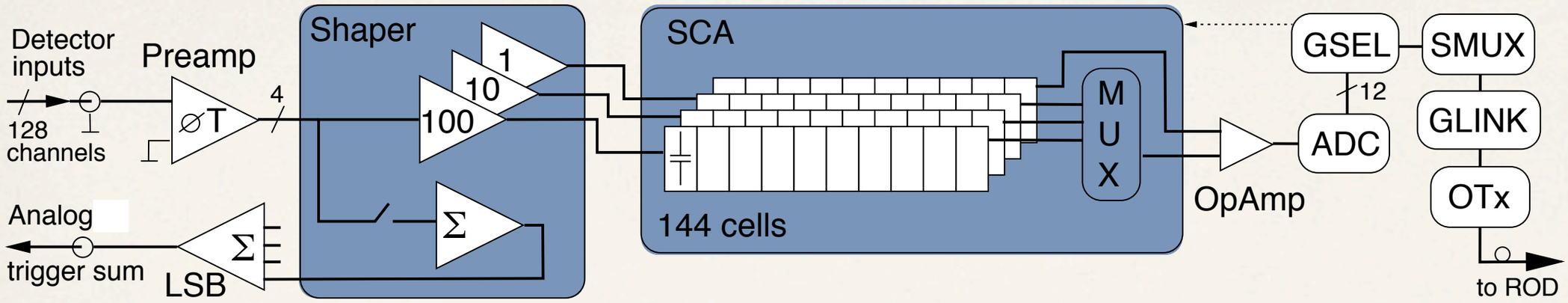
97% warm; 3% cryogenic (hadronic endcap)

3 versions match detector capacitances / dynamic ranges

Hadronic Endcap Preamp:
mounted on the detector inside the cryostat
→ on the front-end boards,
preshapers invert, amplify, and shape the signal



Front-end Board Architecture



Shaper:

3 overlapping linear gain scales
(gain values: 1 low, 9.9 medium, 93 high)

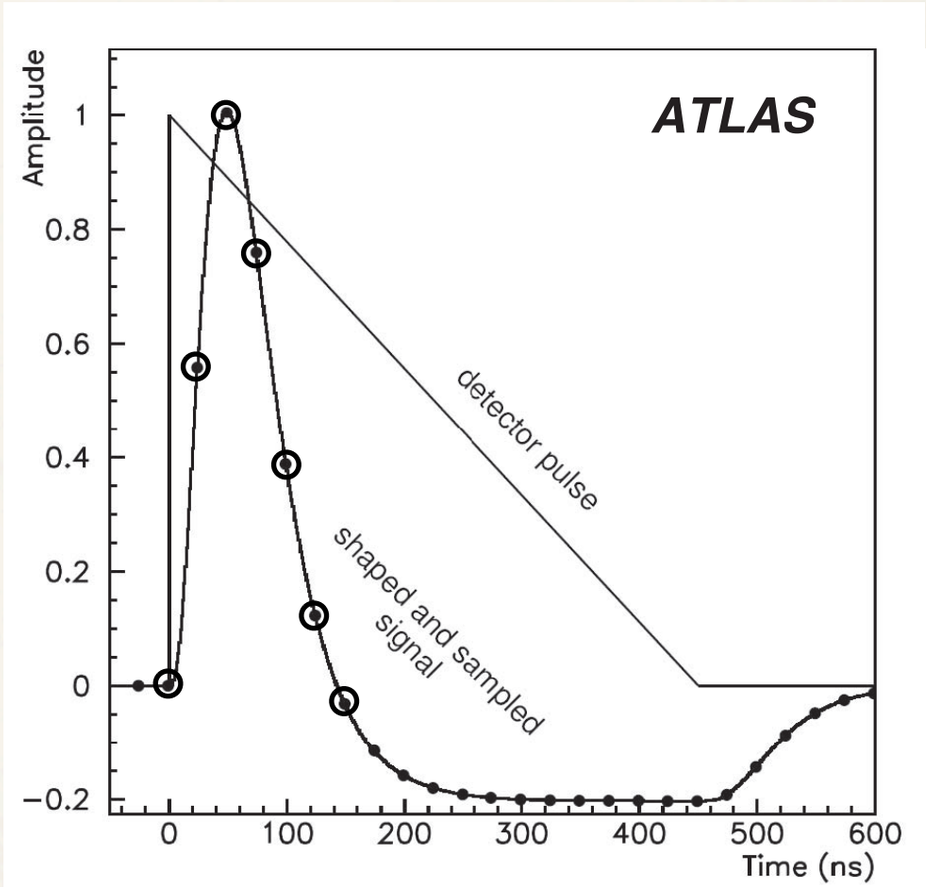
fast bipolar shaping with $\tau = RC = 13$ ns

Switched-capacitor Array (SCA):

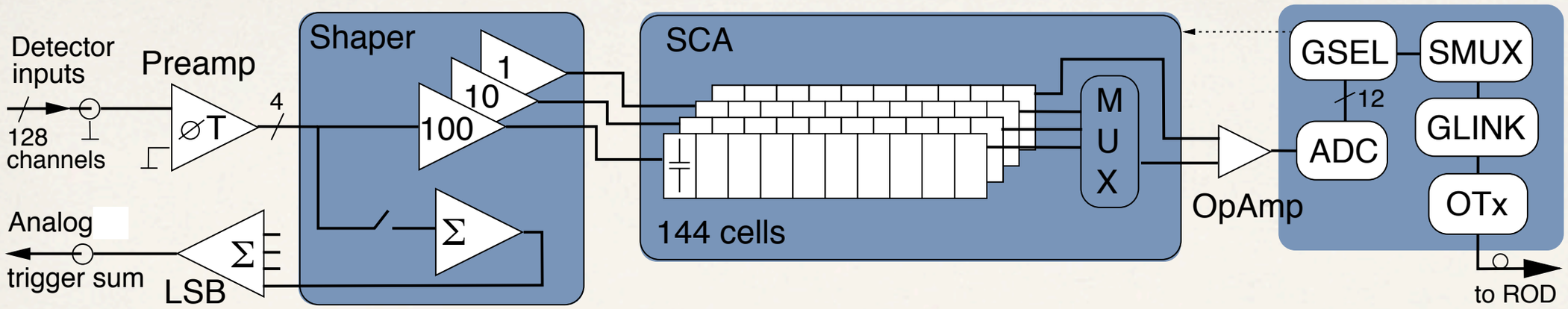
samples the shaped signals at 40 MHz (LHC bunch crossing frequency)

stores analog signals during L1 trigger latency (2.5 μs)

up to 32 samples for physics or calibration runs



Front-end Board Architecture



Shaper:

3 overlapping linear gain scales
(gain values: 1 low, 9.9 medium, 93 high)

fast bipolar shaping with $\tau = RC = 13$ ns

Switched-capacitor Array (SCA):

samples the shaped signals at 40 MHz (LHC bunch crossing frequency)

stores analog signals during L1 trigger latency (2.5 μs)

up to 32 samples for physics or calibration runs

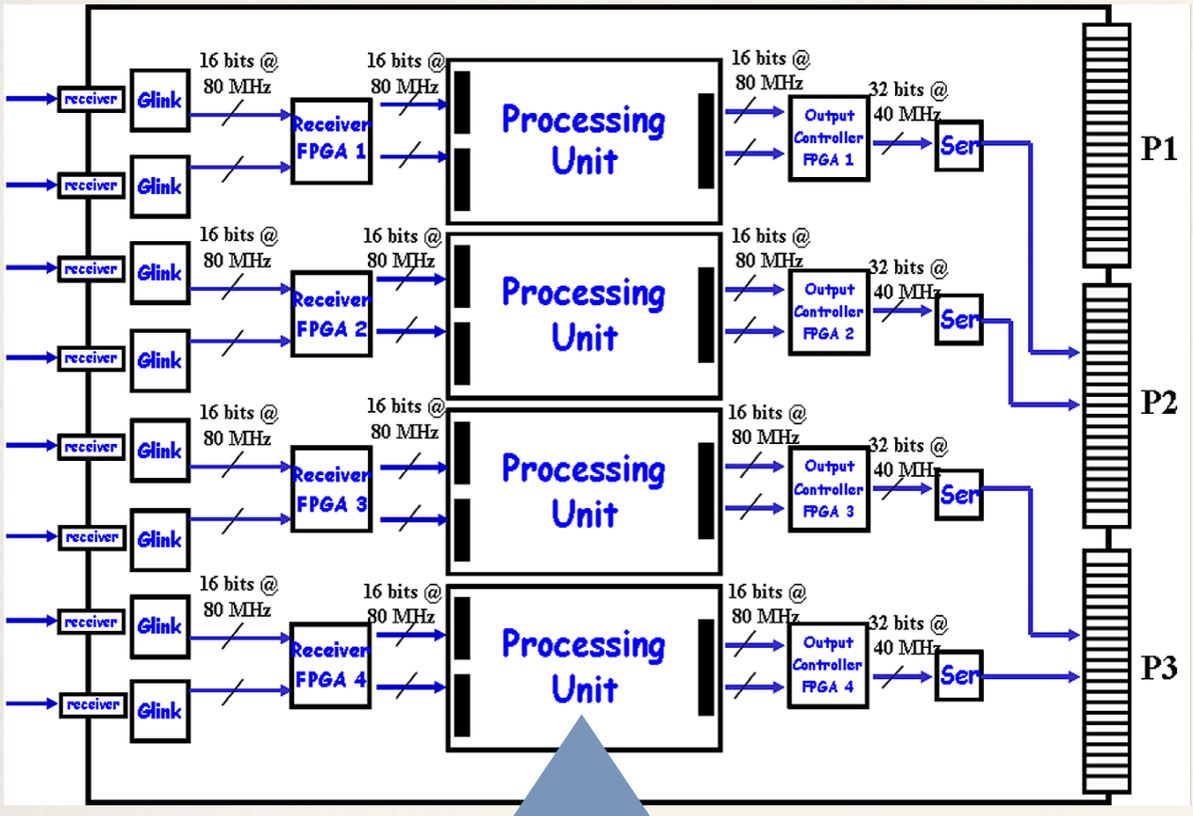
Events accepted by the L1 trigger (up to 75 kHz):

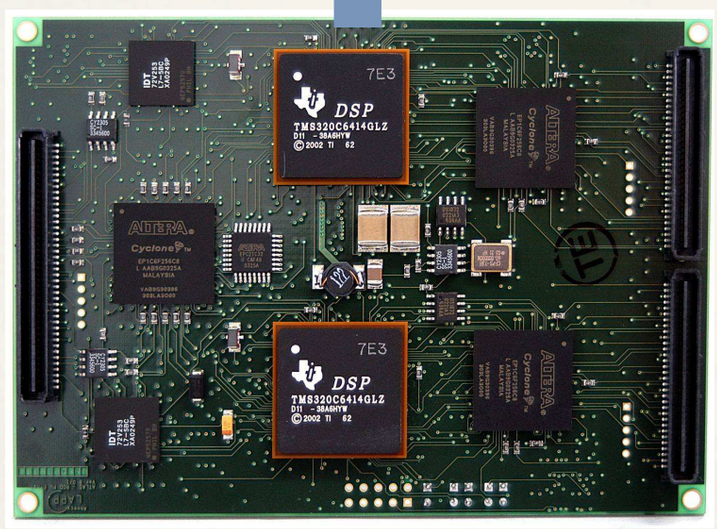
digitized by 12-bit ADCs

Gain Selector (GSEL) chips choose gain for each channel based on peak value of each sample (in medium gain, compared to 2 reference thresholds)

data formatted, multiplexed, serialized, and transmitted optically

Readout Driver (ROD)





Input FPGA:

parallelizes incoming data & verifies its integrity

memory separated into 2 banks: 1 for writing incoming data, the other for data being read by the DSP

Digital Signal Processor (DSP):

high performance: 5.7 x 10^9 instr/s

stores DSP software, input and output data buffers, histograms, and calibration constants (packed in int formats)

1 DSP processes the data from 1 front end board (128 channels)

energy, time, and quality factor calculations are performed on the DSP and have been validated

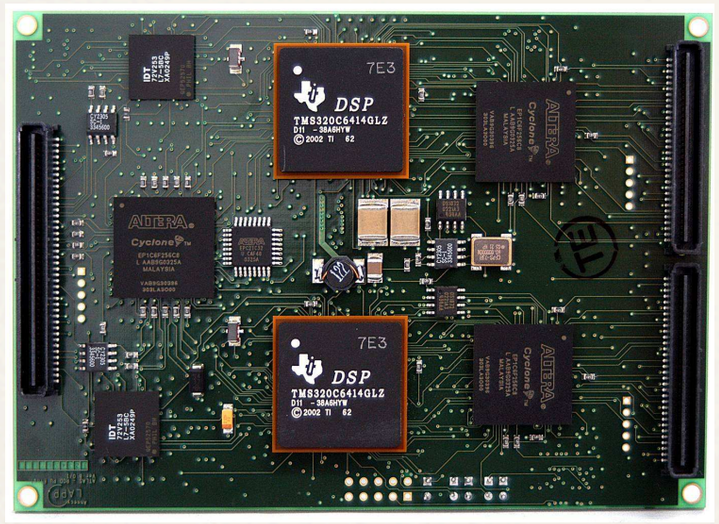
Readout Driver (ROD)

bandwidth limitations:

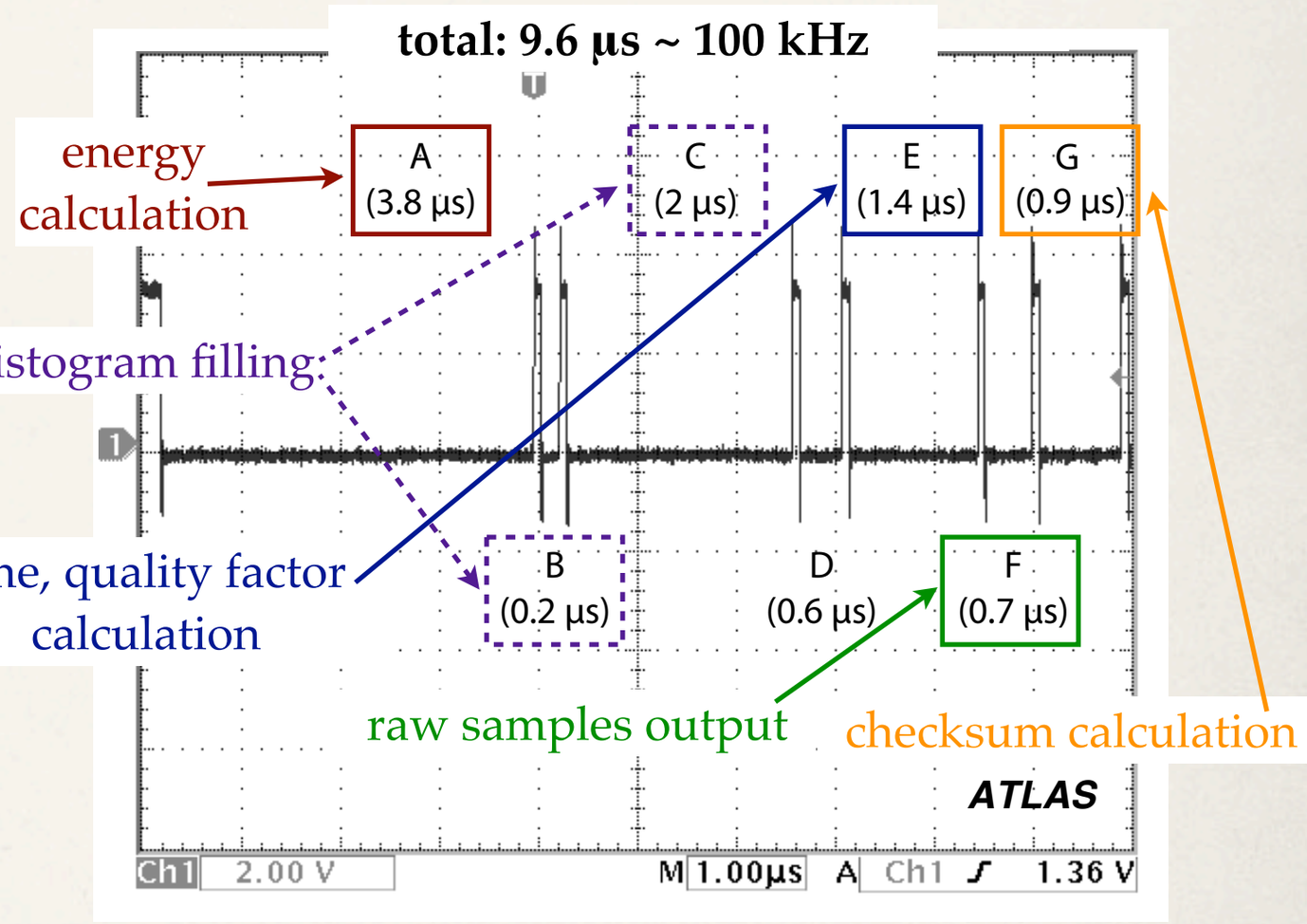
requirement: 75 kHz, achieved w/ 5 samples read out
(currently reading out 7 samples)

input: determined by front end output and input FPGA (tested up to **157 kHz**)

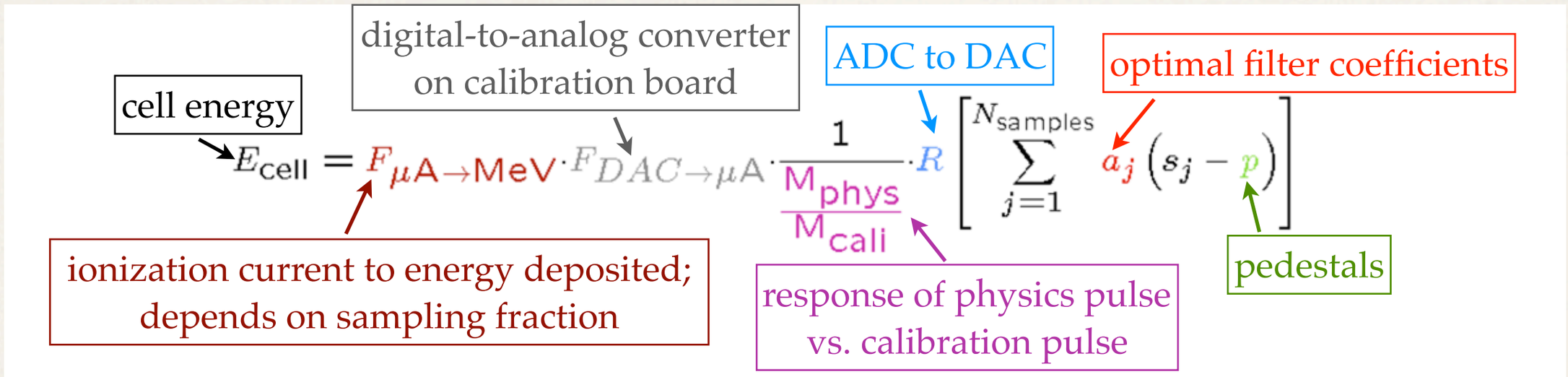
output: DSP computations and output data formatting (tested up to **85 kHz**)



DSP Processing Time for 1 Event (5-sample readout)

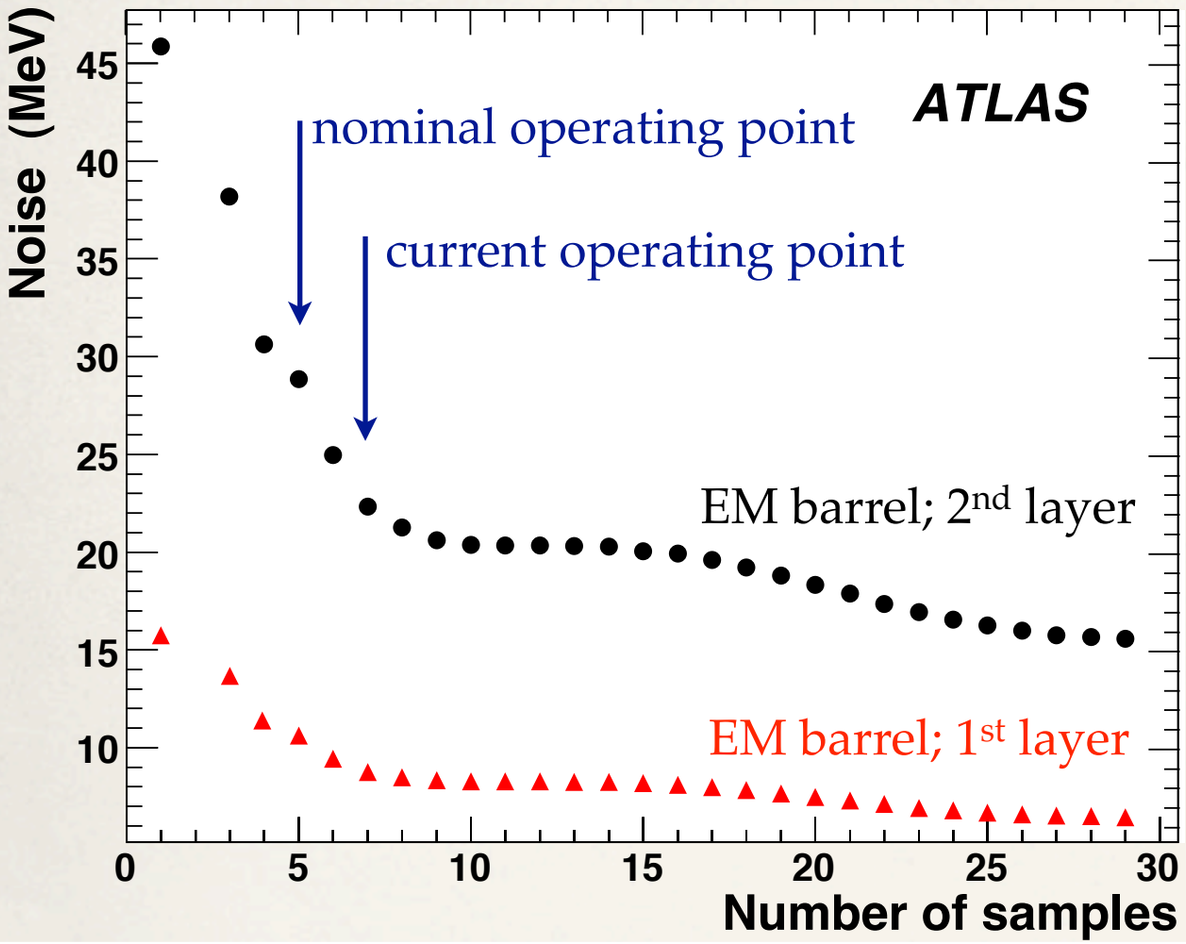


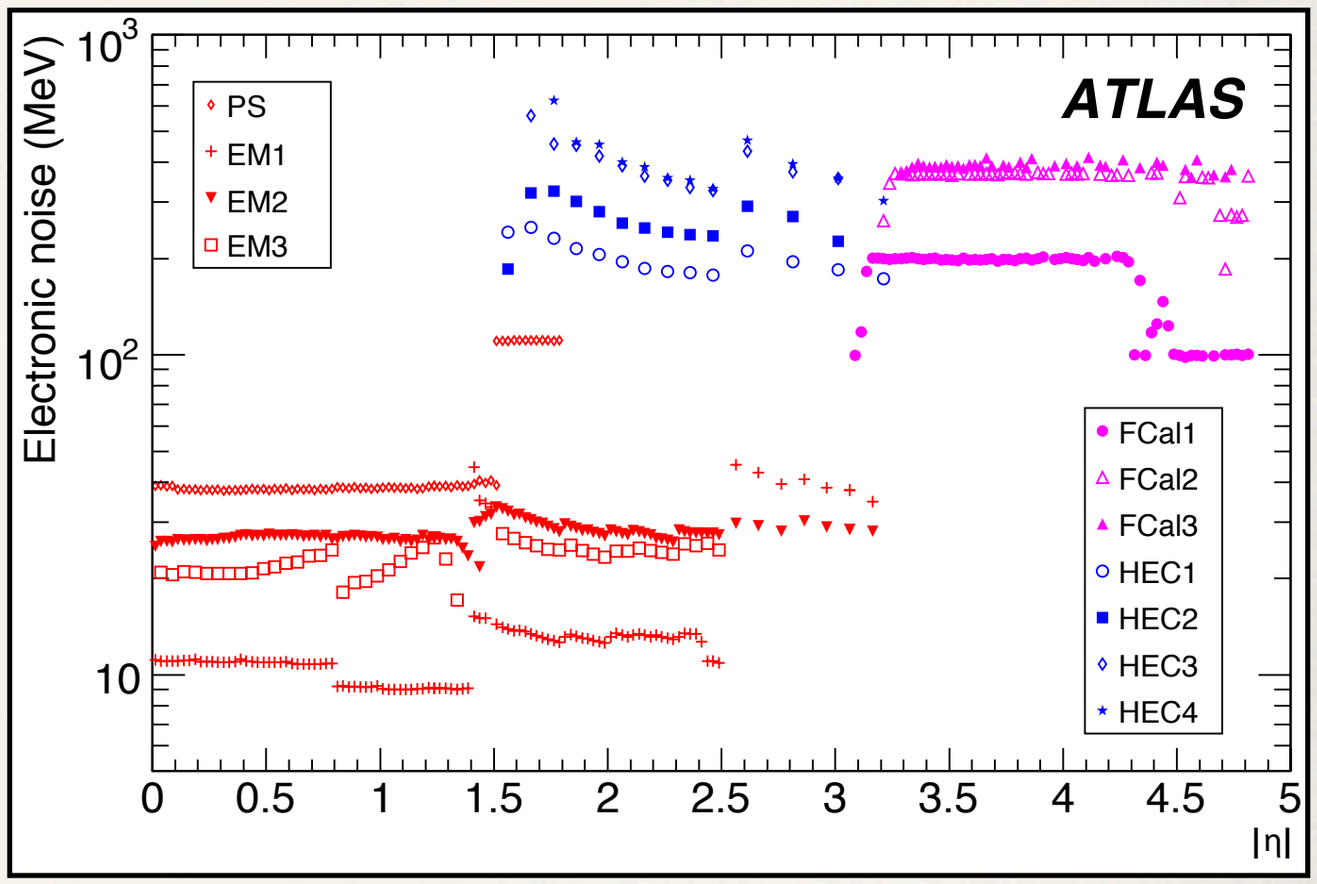
Electronic Calibration



- Calibration runs are taken regularly and automatically processed
  - Types of Calibration Runs
    - **Pedestal**: front end boards triggered and read out w/o input signal
      → determines pedestal value, noise (from RMS of pedestal)
    - **Ramp**: fixed-amplitude calibration pulses injected (exponential before shaping)
      → determines gain of readout from slope of reconstructed pulse amplitude vs. DAC setting
    - **Delay**: fixed-amplitude pulses injected; effective sampling rate of 1 ns
      → detailed study of signal shape

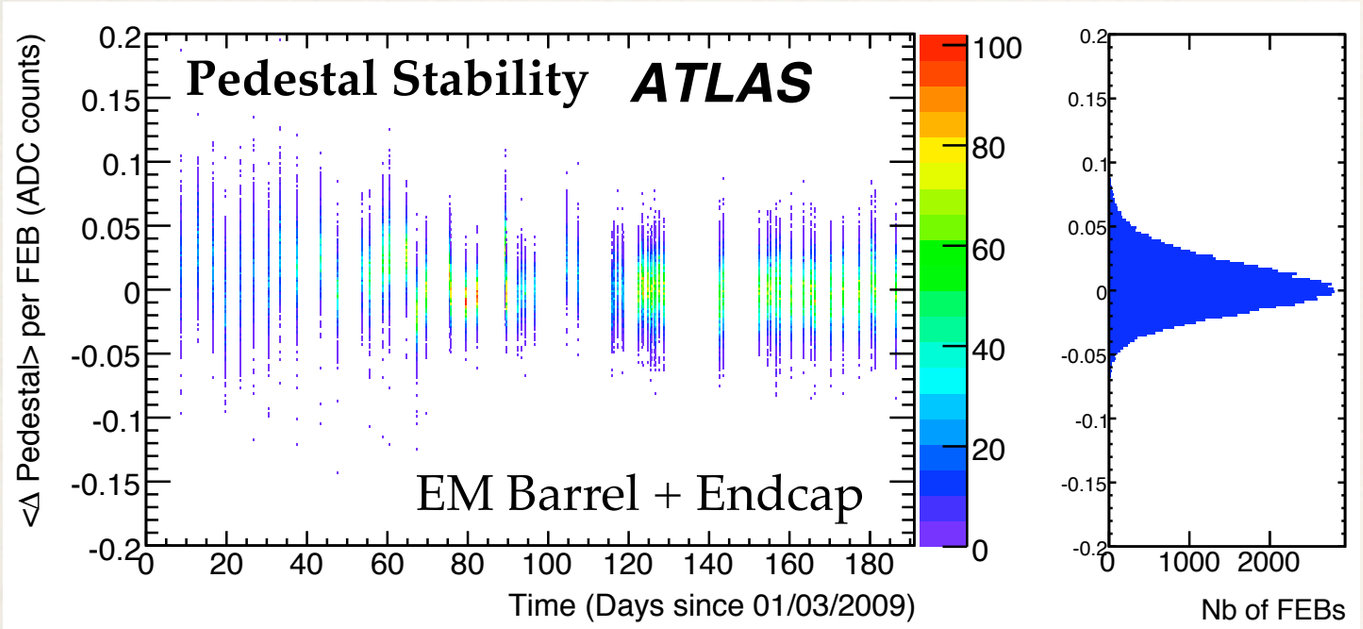
Noise Performance

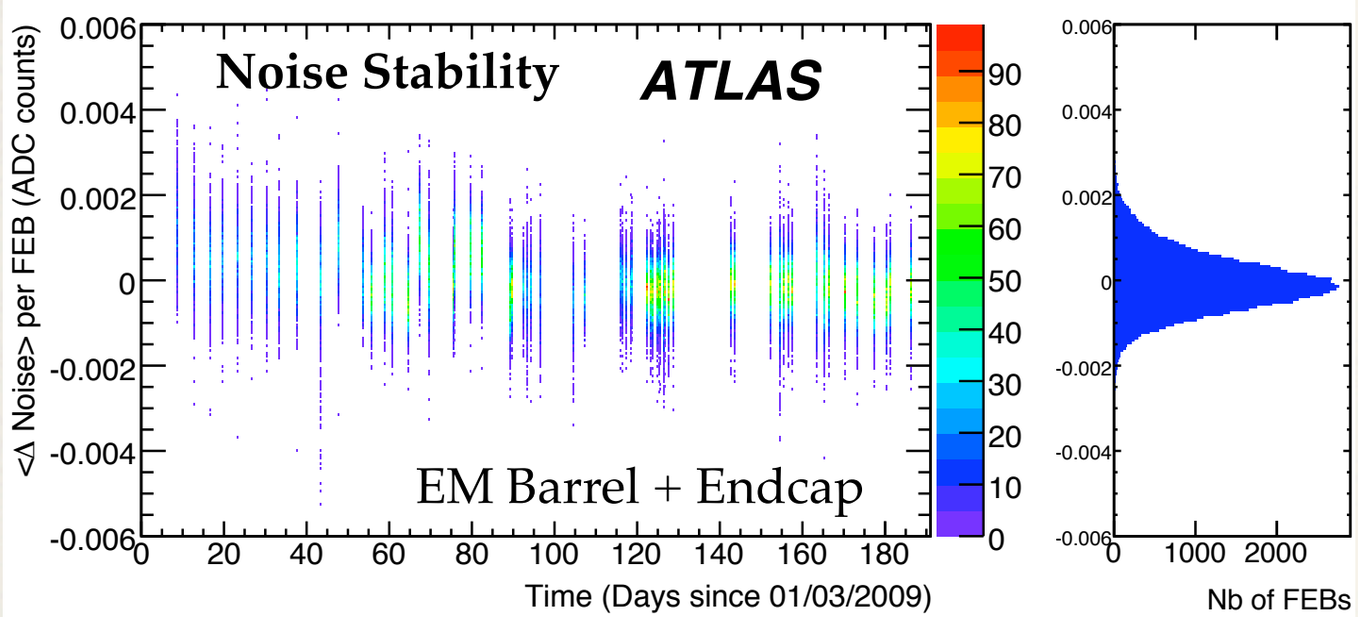




- Typical noise levels: 30 – 50 MeV (EM); 100 – 500 MeV (HEC, FCal)
- Nominal pedestal value (≈1000 ADC counts) allows meas. of the pulse's negative lobe (important for measuring drift time, effect of pile-up from earlier bunch crossings)
- Coherent noise, measured *in situ*: 2 – 6% of total noise per front end board (2 – 3% in second layer of EM → contains largest part of EM shower)

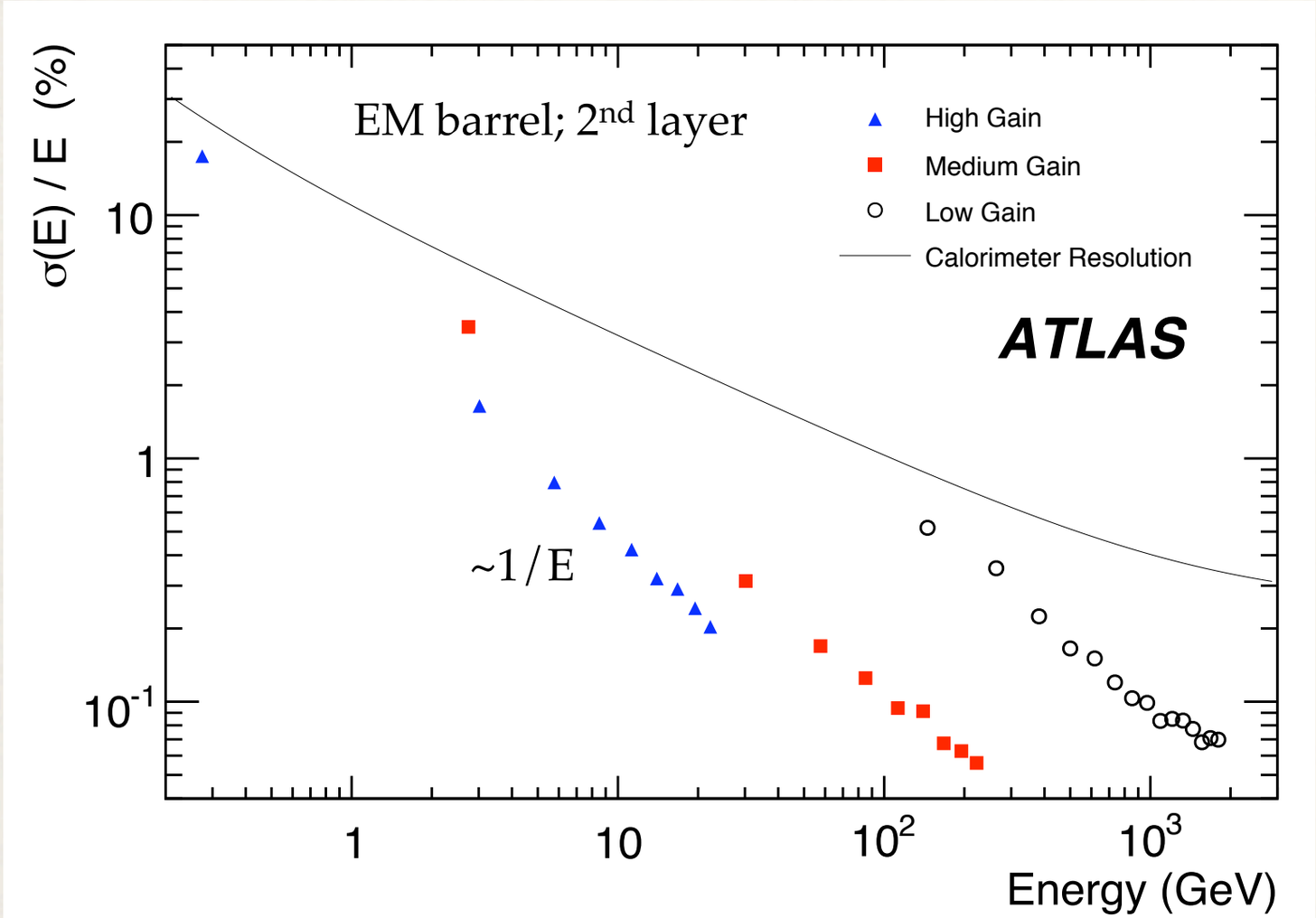
Pedestal and Noise Stability





- Stability of pedestal, noise, and auto-correlation monitored over extended periods of time (plots show a 6-month period in early 2009)
- **ΔPedestal**: ~ 0.02 ADC counts / channel (~1 MeV for medium gain in EM, ~2 MeV in HEC, ~10 MeV in FCal)
- **ΔNoise**: < 0.01 ADC counts in EM high gain, ~0.02 ADC counts in FCal (order of magnitude lower for medium, low gain)

Energy Resolution



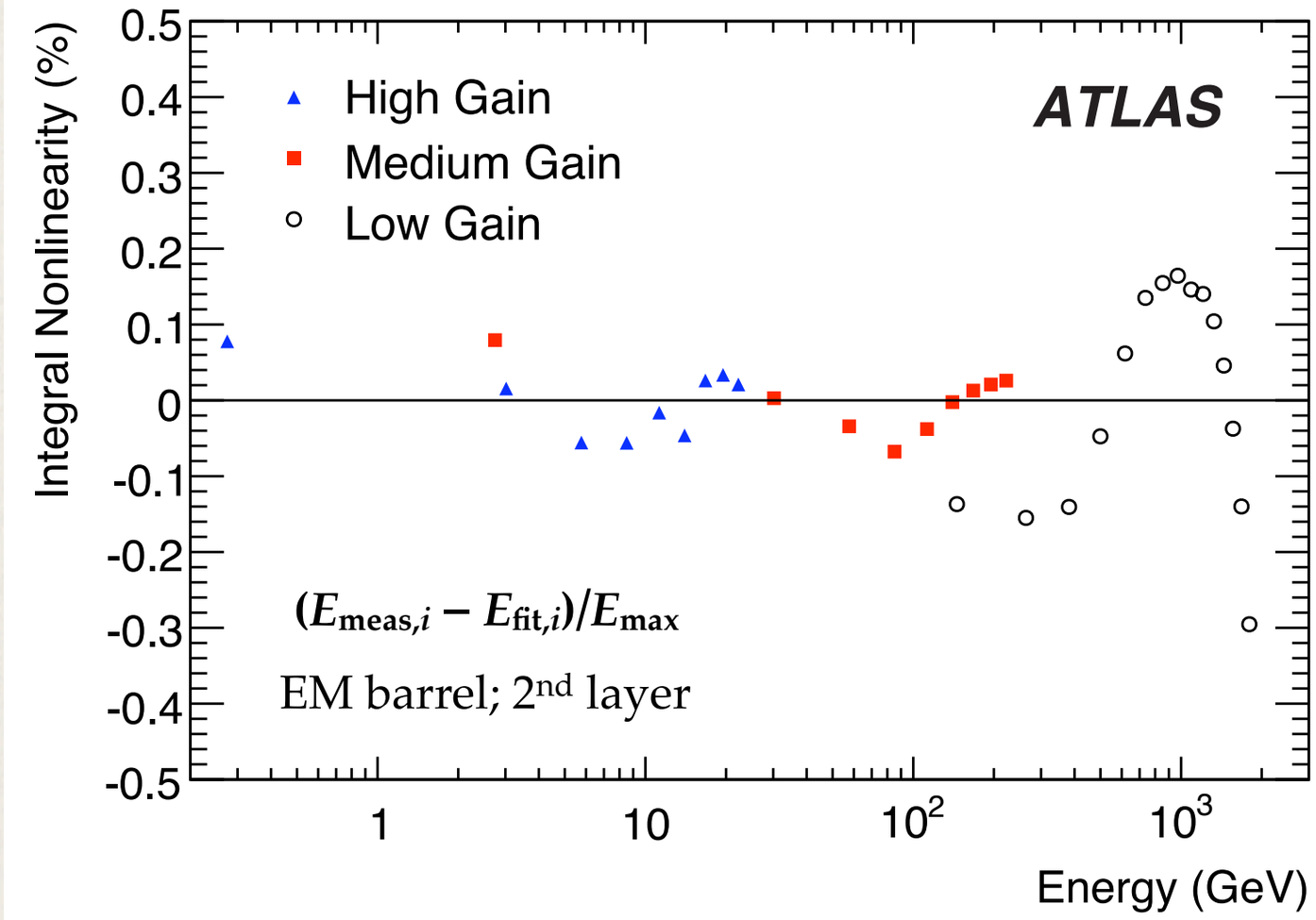
σ = RMS of a single sample (does not take into account improvement from using 5 samples)

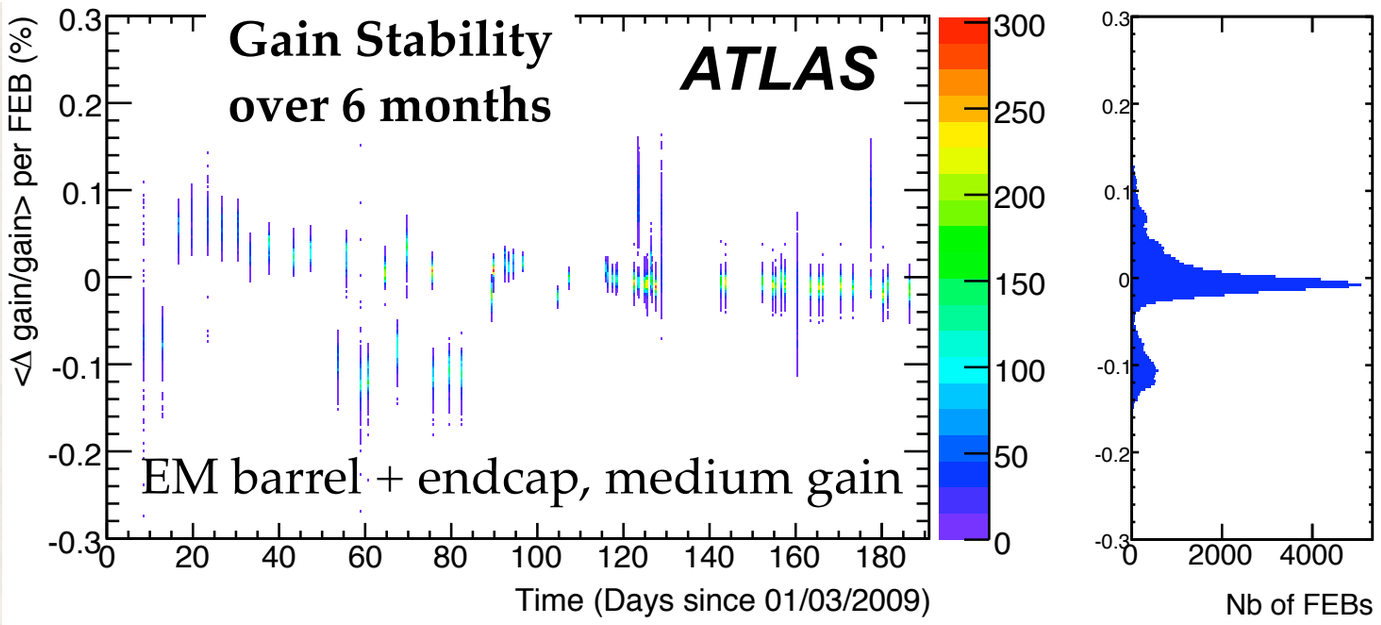
$$\frac{\sigma(E)}{E} = \frac{a}{\sqrt{E}} \oplus b \oplus \frac{c}{E}$$

a = 10% (stochastic term for EM shower)
b = 0.25% (constant term, dominates at high E)
c = 10 MeV (noise from single sample, high gain)

The energy resolution of the LAr electronic readout does not significantly contribute to the overall energy resolution

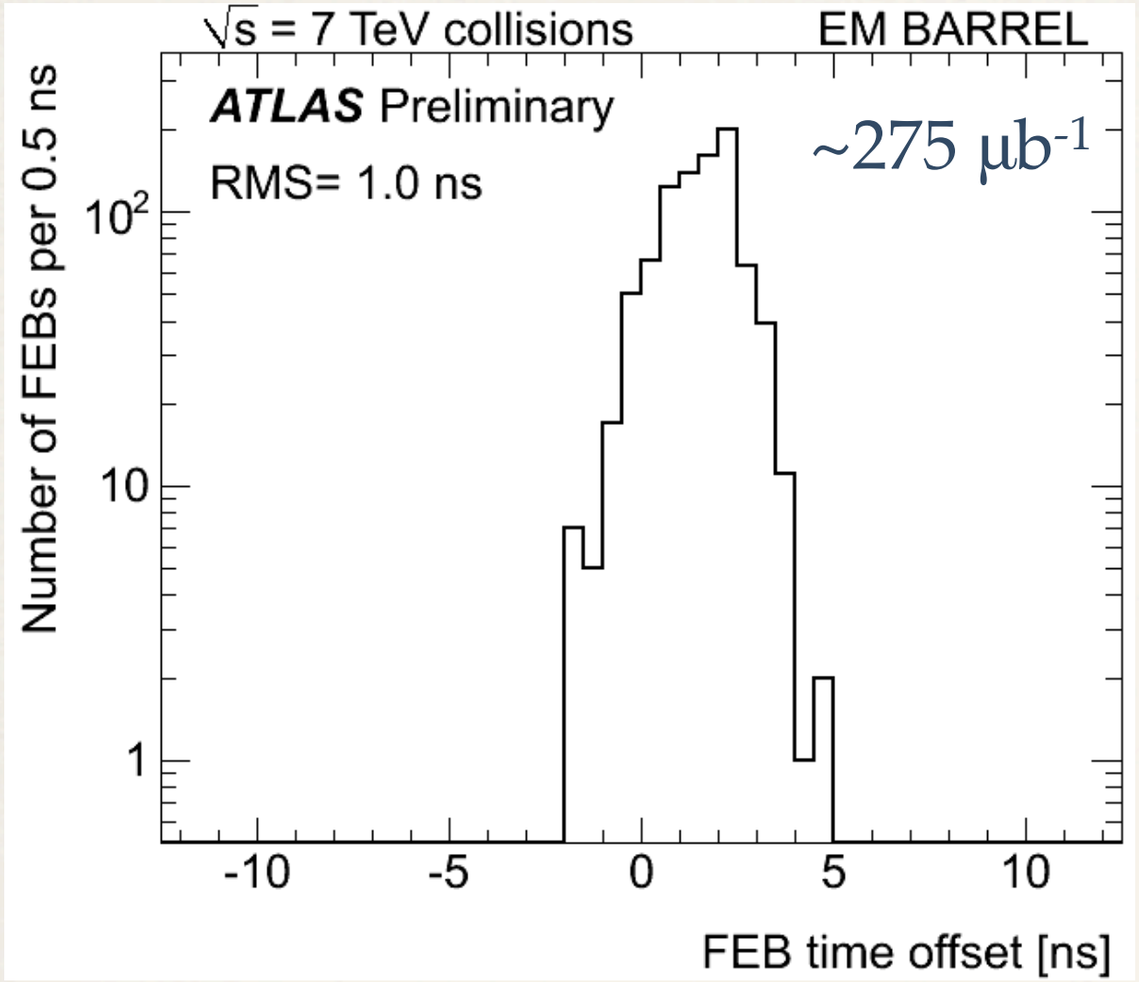
Energy Linearity and Stability





- Energy linearity and stability determined from Ramp calibration runs
- The readout electronics are **linear to ±0.2%** or better (combined effects of front end and calibration boards)
- Gain variations with time are typically within 0.3%
  - outliers still under study; no obvious correlation with temperature or magnetic field
- Crosstalk dominated by capacitive couplings within calorimeter (4 – 7% EM 1st layer)

Timing Alignment & Resolution

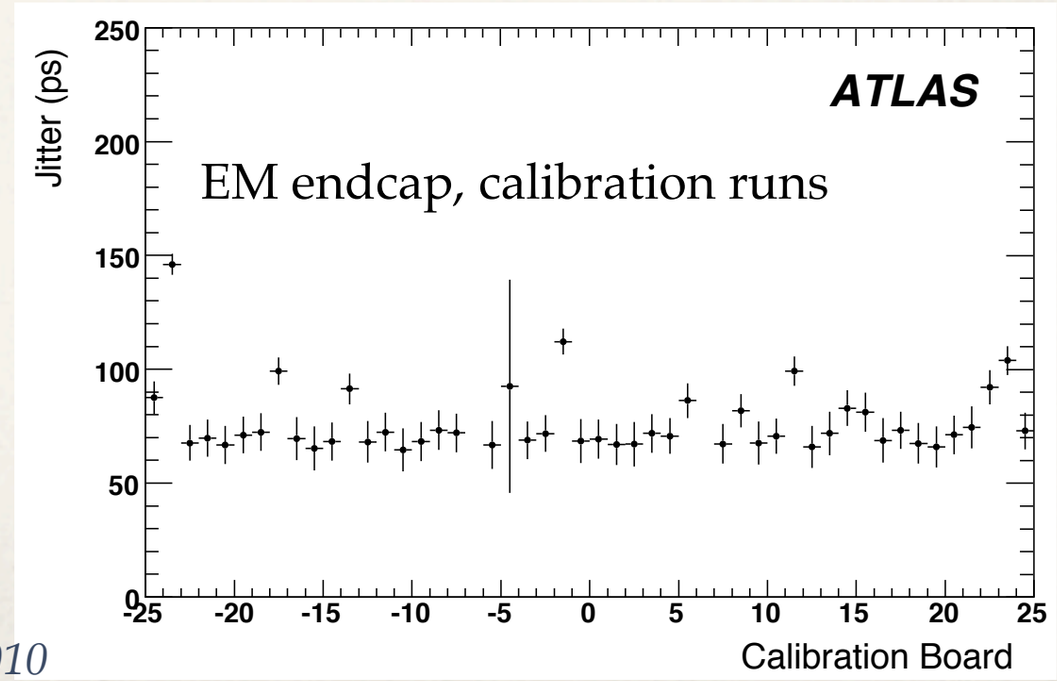


Timing Alignment:

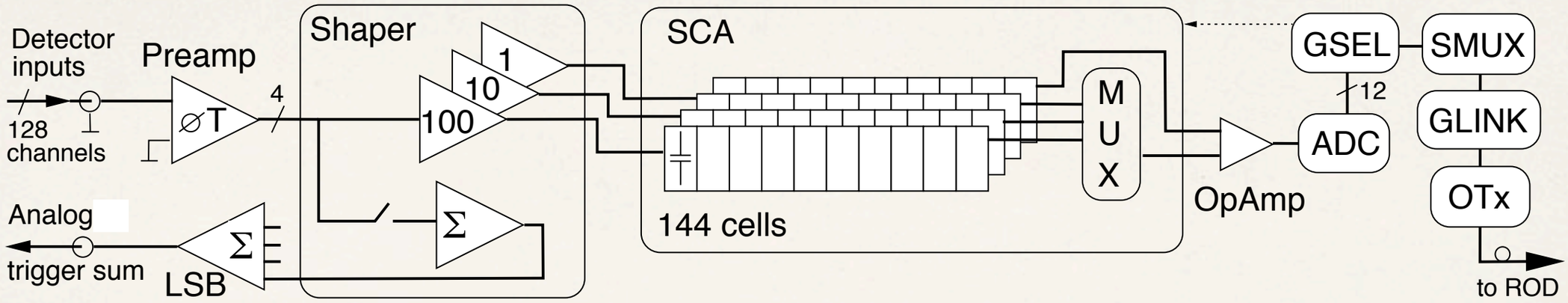
- Adjustments can be made by:
  - setting the delay per 128-channel front end board (applied based on first collision data)
  - adjusting the phase of the optimal filtering coefficients for each channel (in preparation)
- Goal: 100 ps (current resolution: ~1 ns)

Timing Resolution:

- Timing jitter per front end board < 20 ps (measured during production)
- Measured jitter dominated by calibration board TTCrx chip (~70 ps);
  expected to be lower during LHC collisions



Electronic Readout: Outlook

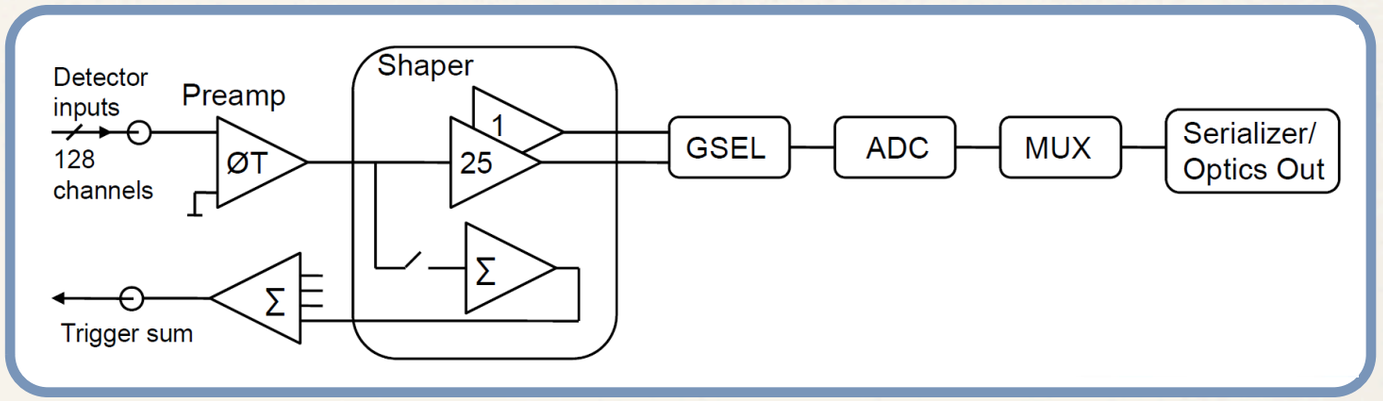


Current front end design complexities / limitations:

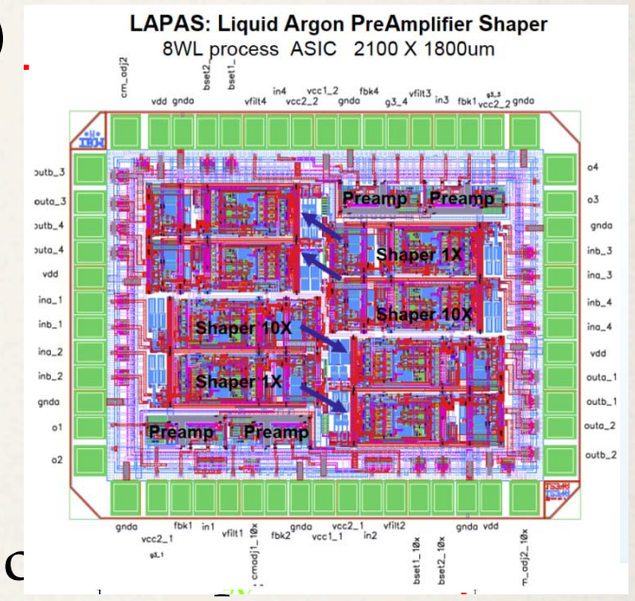
- 11 application-specific integrated circuits (ASICs), some technologies obsolete
  → **prevents component-level upgrade**
- qualified for 10 years of LHC operation
- limited #spares (~6%)
- L1 trigger rate ≤ 100 kHz, latency ≤ 2.5 μs
  → **super-LHC luminosities (up to 10^{35} $cm^{-2}s^{-1}$) challenging**
- analog summing limits L1 trigger sums to $d\eta \times d\varphi = 0.1 \times 0.1$ grid
  → **investigating more flexible, smaller granularity trigger sums**
- consecutive L1 triggers must be spaced > 125 ns apart
  → **difficult to handle bunch trains with shorter spacing**

Electronic Readout: Outlook

- **Proposed Design:** "free-running" architecture (L1 pipeline moved off-detector)



- **challenges**:
  - digitization at 40 MHz (each bunch crossing) → need faster optical links (~100 Gbps/board)
  - modern technology requires lower voltages (difficult to maintain req'd dynamic range & stringent noise performance)
  - critical rad-hard components: analog front end, ADC, optical link, and power supply
- **R&D ongoing**: e.g., IBM SiGe Quad Preamp/Shaper ASIC
  - Preamp: based on current low noise line-terminating design
  - Shaper: 16-bit dynamic range with 2 gain settings, low power c
  - testing completed on hand-wired prototype (all measurements as expected)



➡ will also explore other SiGe technologies and feasibility of CMOS-only design

Summary & Outlook

- The current LAr calorimeter electronics **meets or exceeds the required performance**
  - the readout performs over a wide dynamic range (and can be calibrated); the calibrations show excellent stability over 6-month periods
  - the DSP calculations have been optimized and validated, and the processing time meets the specification for the maximum L1 trigger rates
  - the coherent noise per channel is very low (~2–3% of the total noise)
  - pulses can be reconstructed with a precision that exceeds the intrinsic energy resolution of the calorimeters
  - front end board timing has been commissioned to ~1 ns with early 7 TeV collisions; we expect to achieve a resolution of 100 ps

Summary & Outlook

- The current LAr calorimeter electronics **meets or exceeds the required performance**
  - the readout performs over a wide dynamic range (and can be calibrated); the calibrations show excellent stability over 6-month periods
  - the DSP calculations have been optimized and validated, and the processing time meets the specification for the maximum L1 trigger rates
  - the coherent noise per channel is very low (~2–3% of the total noise)
  - pulses can be reconstructed with a precision that exceeds the intrinsic energy resolution of the calorimeters
    - front end board timing has been commissioned to ~1 ns with early 7 TeV collisions; we expect to achieve a resolution of 100 ps
- After 10 years of operation and with the sLHC expected radiation level, **an upgrade to the front end electronics will be necessary**
  - this provides an opportunity to modernize components and revise the architecture
  - **R&D is progressing** on new ASIC designs, radiation-hard optical links, a high-speed FPGA processing unit for the back end electronics, and a new power supply distribution scheme