



### **Calibration and Performance Electronic Readout of the ATLAS Liquid Argon Calorimeter:** ATL-LARG-SLIDE-2010-079 23 May 2010

**Stephanie Majewski, Brookhaven National Laboratory, on behalf of the ATLAS Liquid Argon Calorimeter Group**



*25 May 2010, IEEE RealTime 2010, Lisbon, Portugal*

# **LHC and ATLAS Performance**







# **ATLAS Liquid Argon Calorimeter**

# **Readout Electronics**

- ✤ Goal: Measure the energy in **182,468 detector channels** over a wide dynamic range (tens of  $MeV - \sim few TeV$ )
- ✤ Front-end electronics:
	- ✤ 1524 front-end boards read out + digitize calorimeter signals
	- ✤ ~300 other boards (calibration, analog trigger sums, controllers, monitoring)
	- ✤ 1524 fiber optic links (1.6 Gbps) to BE
- ✤ Back-end electronics:
	- ✤ 192 Read-out driver (ROD) boards provide digital filtering, formatting, and monitoring
	- ✤ ~800 optical links to ATLAS DAQ *S. Majewski IEEE RealTime 2010*



# **Front-end Board Architecture**



#### **Figure 2.** In this schematic block diagram of the FEB architecture, the data flow is shown for four of the 128 channels per board. The data comes from the detectors on the top left. The top left. The analog sums exist on the top left. The top le **Preamp:**

97% warm; 3% cryogenic (hadronic endcap) of processing through optical transmitters (OTxs) on the right. If these were HEC channels, the preamps

3 versions match detector capacitances / dynamic ranges

reduce the noise. **Hadronic Endcap Preamp:** mounted on the detector



# **Front-end Board Architecture**



more fixed gains, a feature that is used for certain calibration runs. The digitized data are formatted,

### **Shaper:**

3 overlapping linear gain scales are the sum Board of the next level of the next level of the next level (gain values: 1 low, 9.9 medium, 93 high)  $\parallel$   $\qquad$   $\qquad$  would be replaced by preshapers, as described in the text. As described in the text. fast bipolar shaping with  $\tau = RC = 13$  ns

#### reduce the noise. **Switched-capacitor Array (SCA):**

samples the shaped signals at 40 MHz  $\begin{array}{c|c} 0.2 & 0.2 & 0.2 \\ 0.2 & 0.2 & 0.2 \\ 0 & 0.2 & 0.2 \\ 0 & 0.2 & 0.2 \\ \end{array}$ (LHC bunch crossing frequency)

 $\begin{bmatrix} 0 & 0 & 0 \end{bmatrix}$  and  $\begin{bmatrix} 0 & 0 & 0 \end{bmatrix}$   $\begin{bmatrix} 0 & 0 & 0 \end{bmatrix}$   $\begin{bmatrix} -0.2 & \frac{1}{11} & 0 & 100 & 200 & 300 & 400 & 500 \end{bmatrix}$ stores analog signals during L1 trigger latency (2.5 μs)

up to 32 samples for physics or the medium of the medi calibration runs thresholds. The FEBs can also be configured to read out one or  $\int$ 



**Figure 3.** Shapes of the LAr calorimeter current pulse in the detector and of the signal output from the

shaper chip. The dots indicate an ideal position of samples separated by 25 ns.

**3. Pulse reconstruction and calibration**

# **Front-end Board Architecture**



more fixed gains, a feature that is used for certain calibration runs. The digitized data are formatted,

### **Shaper:**

3 overlapping linear gain scales and the law through the next level of the nex (gain values: 1 low, 9.9 medium, 93 high)  $\vert$  digitized by 12-bit ADCs would be replaced by preshapers, as described in the text. As described in the text. fast bipolar shaping with  $\tau = RC = 13$  ns

#### reduce the noise. **Switched-capacitor Array (SCA):**

samples the shaped signals at 40 MHz and data formatted multiplexed sort (LHC bunch crossing frequency) and fremewitted entirely sell-

etores analog signals during I 1 trigger, typically five samples of the Lines of the Lines per channel are read  $\frac{1}{\pi}$ otopa $\frac{1}{2}$ -bit Analog to Digital Converter ( $2.5$ ug). To optimize the  $\frac{1}{2}$ precision of the energy measurement, the Gain Selector chips (GSEL) channel, in each channel, in each channel, stores analog signals during L1 trigger latency (2.5 μs)

up to 32 samples for physics or the medium of the medi calibration runs thresholds. The FEBs can also be configured to read out one or  $\int$ 

**Figure 2.1 In this schematic block diagram of the FEB are flow in the Countries of the C1 trigger is shown for four of the C1 trigger**  $\blacksquare$ 128 channels per board. The data composite on the detectors on the top left. The analog sums exit on t

digitized by 12-bit ADCs

 $\mathbf{S}$  vitched canaditor Array ( $\mathbf{S}$ CA).  $\qquad$  of each sample (in medium gain, Gain Selector (GSEL) chips choose gain for each channel based on peak value compared to 2 reference thresholds)

> data formatted, multiplexed, serialized, and transmitted optically

# **Readout Driver (ROD)**





### **Input FPGA:**

parallelizes incoming data & verifies its integrity

memory separated into 2 banks: 1 for writing incoming data, the other for data being read by the DSP

### **Digital Signal Processor (DSP):**

high performance:  $5.7 \times 10^9$  instr/s

stores DSP software, input and output data buffers, histograms, and calibration constants (packed in int formats)

1 DSP processes the data from 1 front end board (128 channels)

C<br>ne energy, time, and quality factor calculations are performed on the DSP and have been validated

#### **Readout Driver (ROD)** energy threshold (25% of the channels in the example shown), the time and the quality factor are  $\mathbf{L}$  determined in step E. In addition to the processed data, the raw samples are also output in step  $\mathbf{L}$ F for channels above a higher energy threshold. Finally, in step G the DSP calculates a checksum that is used offline to verify the data integrity. The total processing time for all the operations is

### **bandwidth limitations:**

**requirement**: 75 kHz, achieved w/ 5 samples read out **(currently reading out 7 samples)**

input: determined by front end output and input FPGA (tested up to **157 kHz**)

output: DSP computations and output data formatting (tested up to **85 kHz**) histogram filling





9.6 *µ*s, which is low enough to meet the requirement of 13 *µ*s of processing time for 75 kHz L1

triggers.

# **Electronic Calibration**



- ✤ Calibration runs are taken regularly and automatically processed
- **Types of Calibration Runs** 
	- ✤ **Pedestal**: front end boards triggered and read out w/o input signal  $\rightarrow$  determines pedestal value, noise (from RMS of pedestal)
	- ✤ **Ramp**: fixed-amplitude calibration pulses injected (exponential before shaping)  $\rightarrow$  determines gain of readout from slope of reconstructed pulse amplitude vs. DAC setting
	- ✤ **Delay**: fixed-amplitude pulses injected; effective sampling rate of 1 ns  $\rightarrow$  detailed study of signal shape

*S. Majewski IEEE RealTime 2010*

#### Noise Performance depending on the noise measured using a single sample. The noise reduction is not the noise reduction in the n  $\overline{1}$

samples around the peak reduces the noise level, and therefore improves the precision of the energy



- **\*** Typical noise levels: 30 50 MeV (EM); 100 500 MeV (HEC, FCal) **Figure 6.** Measured noise (in MeV) for all sections of the ATLAS LAr calorimeters. The PS, and three 1);  $100 - 500$  MeV (HEC, FCal)
- Nominal pedestal value (≈1000 ADC counts) allows meas. of the pulse's negative lobe (important for measuring drift time, effect of pile-up from earlier bunch crossings)  $A$ ditional calibration runs use the calibration board to inject precise pulses with programmability  $\mathcal{A}$ amportant for measuring drift time, effect of pile the range from 1 MHz to 40 MHz, with a narrow (100 Hz) filter bandwidth, to evaluate the impact
- ✤ Coherent noise, measured *in situ*: 2 − 6% of total noise per front end board (2 − 3% in second layer of EM  $\rightarrow$  contains largest part of EM shower) ibration board, and the timing of the pulse can also be programmed. The calibration pulses are **Example 1** Coherent noise, measured in situ:  $Z - 6\%$  of total  $\frac{1}{\sqrt{2}}$  $60$  of total poice par front and hoord  $\sigma/\sigma$  of total holder per front end pour a tains largest part of EM shower) could be contained approximately as an expected contains a coherent noise of  $10<sub>10</sub>$ the total noise per channel for an external field of 1 mA/m at a frequency of 28.5 MHz. Such a field

# **Pedestal and Noise Stability**

0



<

0

- Stability of pedestal, noise, and auto-correlation monitored over extended periods of time (plots show a 6-month period in early 2009)
- ✤ **ΔPedestal**: ~ 0.02 ADC counts / channel (~1 MeV for medium gain in EM, ~2 MeV in HEC, ~10 MeV in FCal)
- ✤ **ΔNoise**: < 0.01 ADC counts in EM high gain, ~0.02 ADC counts in FCal (order of magnitude lower for medium, low gain)

### Energy Resolution curso enc



*E* = √*E* ⊕*b*⊕  $\frac{c}{E}$ **a = 10%** (stochastic term for EM shower) dominates at high E) **c = 10 MeV** (noise from

*a*

*c*

 $\sigma(E)$ 

 $\sigma$  = RMS of a single sample (does not take into recount improvement from using 5 samples beam studies beam studies before the final system was installed, a sample of  $\mathcal{L}$ **Figure 9.** Energy resolution versus energy of a representative EMB second layer channel, as measured account improvement from using 5 samples)

**The energy resolution of the LAr electronic readout does not**  significantly contribute to the overall energy resolution  $\vert$  The energy resolution of the LAr electronic readout does not The energy resolution of the EAT electron  $T$  resolution for medium gain is just under  $\alpha$  at the energy of  $25$  GeV, where it takes over  $\alpha$ 

### Energy Linearity and Stability  $\blacksquare$  the combined effects of both the  $\blacksquare$ called  $\sum$  *L*



- ✤ Energy linearity and stability determined from Ramp calibration runs
- ✤ The readout electronics are **linear to ±0.2%** or better (combined effects of front end and calibration boards)
- ✤ Gain variations with time are typically within 0.3%
	- ✤ outliers still under study; no obvious correlation with temperature or magnetic field
- ✤ Crosstalk dominated by capacitive couplings within calorimeter  $(4 - 7\%$  EM 1<sup>st</sup> layer)

# **Timing Alignment & Resolution**



### **Timing Resolution:**

- ✤ Timing jitter per front end board < 20 ps (measured during production)
- ✤ Measured jitter dominated by calibration board TTCrx chip (~70 ps); expected to be lower during LHC collisions *S. Majewski IEEE RealTime 2010*

### **Timing Alignment:**

- ✤ Adjustments can be made by:
	- ✤ setting the delay per 128-channel front end board (applied based on first collision data)
	- ✤ adjusting the phase of the optimal filtering coefficients for each channel (in preparation)
- ✤ Goal: 100 ps (current resolution: ~1 ns)



## **Electronic Readout: Outlook**



### **Figure 2. In this Schematic Current front end design complexities / limitations:**

- 128 channels per board. The data comes from the detectors on the top left. The analog sums exit on the bottom left through the Layer Sum Boards (LSBs) while the digital results are transmitted to the next level ✤ 11 application-specific integrated circuits (ASICs), some technologies obsolete → prevents component-level upgrade
- would be replaced by preshapers, as described in the text. ✤ qualified for 10 years of LHC operation
- ✤ limited #spares (~6%)
- the long tail from the detector response, while the two integrations limit the bandwidth in order to  $\cdot$  L1 trigger rate ≤ 100 kHz, latency ≤ 2.5 µs  $\rightarrow$  super-LHC luminosities (up to 10<sup>35</sup> cm<sup>-2</sup>s<sup>-1</sup>) challenging
- analog summing limits L1 trigger sums to dη × d $\varphi = 0.1 \times 0.1$  grid  $\sim$  investigating more flevible, smaller granularity trigger same  $\overline{\phantom{a}}$  and digitized using a 12-bit Analog to Digitized using a 12-bit Analog to  $\overline{\phantom{a}}$ . To optimize the SCA analog to  $\overline{\phantom{a}}$ → **investigating more flexible, smaller granularity trigger sums**
- consecutive L1 triggers must be spaced > 125 ns apart → difficult to handle bunch trains with shorter spacing

## **Electronic Readout: Outlook**

### **Proposed Design:** "free-running" architecture (L1 pipeline moved off-detector)

### ✤ **challenges**:

✤ digitization at 40 MHz (each bunch crossing) → need faster optical links (~100 Gbps/board)



- ✤ modern technology requires lower voltages (difficult to maintain req'd dynamic range & stringent noise performance) **keeps many options open** es lower voltages (  $\text{unc range} \propto \text{stringent noise performance}\,,$ **Analog Frontier Execute Execute**
- \* critical rad-hard components: analog front end, ADC, optical link, and power supply rico: analog from cha, *i* **upgrade Preamplifier: based on low noise line-terminating**  breams: analog front end, ADC,  $\mathbf{H}$ *Exampler* **accommodate full 16-bit dynamic range**
- $\cdot$  **R&D ongoing**: e.g., IBM SiGe Quad Preamp/Shaper ASIC  $\epsilon$  gaar Frank/ Staper 2010
	- Preamp: based on current low noise line-terminating design • **Ptot = 42mW Shaper**
	- Shaper: 16-bit dynamic range with 2 gain settings, low power consumer that the settings of the set • **En ~ 2.4nV/¥+]** range with 2 gain settings, lo
	- testing completed on hand-wired prototype (all measurements as expected) • **Low power consumption: 130mW (combined 1X, 10X channels)**
- ➡ will also explore other SiGe technologies and feasibility of CMOS-only design



# **Summary & Outlook**

- ✤ The current LAr calorimeter electronics **meets or exceeds the required performance**
	- ✤ the readout performs over a wide dynamic range (and can be calibrated); the calibrations show excellent stability over 6-month periods
	- ✤ the DSP calculations have been optimized and validated, and the processing time meets the specification for the maximum L1 trigger rates
	- ✤ the coherent noise per channel is very low (~2−3% of the total noise)
	- ✤ pulses can be reconstructed with a precision that exceeds the intrinsic energy resolution of the calorimeters
	- ✤ front end board timing has been commissioned to ~1 ns with early 7 TeV collisions; we expect to achieve a resolution of 100 ps

# **Summary & Outlook**

- ✤ The current LAr calorimeter electronics **meets or exceeds the required performance**
	- ✤ the readout performs over a wide dynamic range (and can be calibrated); the calibrations show excellent stability over 6-month periods
	- ✤ the DSP calculations have been optimized and validated, and the processing time meets the specification for the maximum L1 trigger rates
	- ✤ the coherent noise per channel is very low (~2−3% of the total noise)
	- ✤ pulses can be reconstructed with a precision that exceeds the intrinsic energy resolution of the calorimeters
	- ✤ front end board timing has been commissioned to ~1 ns with early 7 TeV collisions; we expect to achieve a resolution of 100 ps
- ✤ After 10 years of operation and with the sLHC expected radiation level, **an upgrade to the front end electronics will be necessary**
	- ✤ this provides an opportunity to modernize components and revise the architecture
	- ✤ **R&D is progressing** on new ASIC designs, radiation-hard optical links, a highspeed FPGA processing unit for the back end electronics, and a new power supply distribution scheme

#### *S. Majewski IEEE RealTime 2010* 19