USE OF A MOTOROLA 68000 VMEbus BASED SYSTEM FOR FAST READ-OUT OF A RETICON PHOTOSENSITIVE ARRAY

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Abstract

The read-out system is built on 9u size boards in a Eurocrate with VMEbus J1 and J2 dataways and uses a Motorola 68000 processor to control the read-out of a Reticon based camera. The read-out normally runs asynchronously at a regular rate to give a constant noise from charge leakage and gives a fast rejection of each frame read unless it is accompanied by an external accept signal.

Accepted events are transferred to an LSI 11/23 computer for display after background subtraction.

Frames are read by DMA directly into the memory at a rate of one pixel per five hundred nanoseconds, which is limited by the speed of available memory, and then only selected events of interest are transferred at relatively low rate to the display. The system has been tested by selecting events from an optical read-out avalanche chamber where a cosmic ray track has passed through the active region. It will be used for the optical read-out of scintillating fibres.

1 Introduction

At Bristol we have developed a fast two dimensional optical readout system. This has been developed to study the light from an electron avalanche chamber and also from scintillating fibres.

The avalanche chamber was constructed as part of a Cerenkov ring imaging detector [1], for which the camera readout system was initially developed. Light from the Cerenkov radiator was focused onto the calcium fluoride input window of the avalanche chamber. The avalanche chamber acts as an image intensifier. Photoelectrons are multiplied to produce avalanches which emit light from atoms excited by the avalanche [2]. This light was then focused onto the photocathode of a Mullard XX1500 type image intensifier. A Reticon integrated photodiode array was coupled to the phosphor screen of the image intensifier via fibre optics and the digitised data from the pixels was read out with the VMEbus 68000 system, Fig 1.

Further developments have lead to the camera being used in a prototype detector constructed from scintillating glass fibres [3]. At present a bundle of fibres made from GS1 glass is used as an interaction target. Light from the fibres was fed away from the beam to a diode type image intensifier. This is an intensifier without a channel-plate; it consists of a thin alkali metal photocathode and a phosphor screen. Electrons liberated at the photocathode are accelerated in an electric field and collide with the phosphor screen to generate light [4]. This diode type image intensifier has a good quantum efficiency and a clean single photoelectron peak, but has fairly low gain. Coupled to the phosphor screen of the diode intensifier is a high gain gated channel-plate type

intensifier, which is normally gated off to decrease any photocathode noise. Coupled to the exit window of this intensifier will be the Reticon device.

2 The data acquisition system

The data acquistion system consisted of an LSI 11/23 computer and a VMEbus based 68000 system, which acted under program control of the 11/23. Communication between the two computers was by means of a 16 bit bidirectional parallel interface.

2.1 The solid state camera

The camera is based on an EG+G Reticon device RA100 or RA256, Fig 2. This is a silicon device with a square array of photodiodes, which can be read out sequentially and is in operation unlike a CCD. The rows of photodiodes are accessed sequentially and each row is shifted only once into a BBD type output register. This circumvents the problems that CCDs have of light arriving while the shifting process is in operation, and consequently appearing in the wrong place in a reconstructed image. The RA256 device has a pixel centre to centre spacing of 40 microns and a total active area of 12mm by 12mm.

The Reticon device had a fibre optic coupling piece bonded to its surface to allow uniform illumination of the whole active surface. Previous use of a CCTV lens had proved inadequate due to severe transmittance variations across the lens surface. The fibre optic protuded about 1 cm from the ceramic chip package to allow easy optical mating with the device to be viewed.

The active elements of the Reticon device are reversed bias photodiodes, Fig 3, with a reset charge stored its inbuilt capacitance while in the reversed biased state. Electron-hole generation by photons falling onto the pixel create a charge deficit on the reset level and this is the signal sensed at the output. Electron-hole pairs are generated thermally, and in the absence of any signal there is still a leakage current across the photodiodes. This gives rise to a fixed pattern noise in the output (assuming the readout time is constant). The problem of this pattern noise was minimised by first taking a background frame (by averaging 16 frames) and subtracting this (online) from every frame transferred to the LSI 11/23.

The signals from adjacent pixels are fed to two output stages on the chip, and then onto an "OUTPUT PROCESSOR" board. This board buffered and amplified them and provided correlated doubling sampling. The signal emanating from the chip consists of the wanted signal and a bias voltage superimposed onto the bucket-brigade reset voltage, which was found to drift with time. To eliminate this drift from the final signal the technique of correlated double sampling was employed. Here this technique was implemented by the first section of the circuit, shown in Fig 4. After the output amplifier of the Reticon has been reset and before the next signal charge is sampled the point B is reset to a clamp voltage by pulsing on the mosfet Tl. Thus when the next signal charge is transferred into the output amplifier the point ´A´ goes to the voltage Vreset-(Vbias+Vsig) and the point ´B´ goes to Vclamp-(Vbias+Vsig); hence the term Vreset is eliminated from the signal amplified by further stages in the "OUTPUT PROCESSOR" board, Fig 5.

Clock and control signals for the chip were provided by a separate camera controller board which was connected to the camera by ECL level twisted pair cable. The clock signals were buffered by a "DRIVER" board before being applied to the chip, bias levels were also provided by this board.

The signals were then fed to a TRW TDC1048E1C flash ADC card, which fed its digitised output down an ECL twisted pair to the camera controller.

The two digitised values for the pixels were latched on the camera controller before being passed via another ECL twisted pair to the VME system. When running the frames from the camera were read continuallly into the VME memory.

2.2 The VMEbus system

The VME system is a mixture of commercially available components and special units built at Bristol. The prototype units were constructed on standard double extended eurocards, but their size proved to be a severe limitation on the functionality of a board. One unit, the DMA controller, was built on two double extended eurocards, interconnected with a ribbon cable, which was far from satisfactory. So a new size, 9U, was adopted for construction.

To allow double extended eurocard components to be used the VME crate was divided into two sections. The left hand half was built to take these cards, and the right hand half to accommodate 9U boards.

The backplane specifications limit the current that can be drawn from the 5 volt line for a single slot to 3 amps, which for a 9U size board filled with TTL logic would prove

insufficient. So an extra power connector was added below the J2 connector, and a separate ´power bus added to the crate. This also allowed for separate analogue power lines to be supplied to a board.

The units for the VME system consisted of an 8 MHz M68000 cpu board and a 1/2 Mbyte dynamic RAM card. The following were specially constructed for this application :

DMA controller.

16 bit parallel interface.

NIM trigger unit.

2.2.1 The DMA Controller

This provided the interface between the camera controller and the VME memory. The board contained logic for bus mastership acquisition and, for handshaking to control the flow of data from the camera controller board, and to write the data into the system memory. The mastership of the bus was gained by the circuit in Fig 6. Under program control the Q output of flip-flop U1 was set. this was fed to the VME signal BR1* to request mastership of the bus. The 68000 responded with the BGACK* signal which was latched by U2 when AS* was high (at the end of current bus cycle). This ensured that BBSY* was not asserted during the bus cycle by the CPU which originally set BR1*.

The DMA was a block transfer of a single frame from the camera, which for the RA256 device consisted of 64 Kbytes. To increase data throughput the data was transferred as words, and at the end of a frame or upon an error condition occurring the bus mastership was relinquished.

The flow of data from the camera controller to the DMA controller was controlled by 'handshake' signals. The handshaking allowed an asynchronous flow of data from the camera to the VME system, the data rate being limited by the system memory speed. In practice the rate was determined by the time taken for a memory write cycle when a refresh cycle was in progress, which in our case was 1 microsecond. The data rate could therefore be vastly improved by using a fast static memory board for the ring buffer data area.

The handshaking between the camera and the controller consisted of four signals, Fig 7.

Two signals 'ENABLE' and 'SEND' are driven by the DMA controller and the 'RECEIVE','EOF' signals by the camera controller. The 'ENABLE' signal signified that a frame of data was required, the 'SEND' signal requested a 16 bit word of data from the camera controller. In response to the 'SEND' signal, the camera controller placed a word of data on the cable, and, after a delay to allow for propagation time on the cable, asserted 'RECEIVE'.

After latching the data on the DMA controller board 'SEND' was removed, which in turn allowed 'RECEIVE' to be removed, and a bus cycle was then initiated to write the data to memory. Upon completion of the bus cycle 'SEND' was again asserted to request the next word of data.

The 'EOF' signalled the end of a frame and arrived after the last pixels were transferred.

Fig 8 shows the relationship between the handshake lines and the data flow.

2.2.2 Parallel interface

This device was also constructed to provide a bidirectional interface between the VME system and the 11/23. A commercially available DRV-11 interface was purchased for the 11/23. The interface constructed interface has TTL logic levels and contains a four line handshake system to control the data flow at a rate of 100 Kwords per second.

2.2.3 NIM trigger unit

As NIM logic is used extensively in high energy physics, a NIM level input/output module was constructed . It consists of four self-latching inputs and four pulsed outputs. The unit can be configured to interrupt the 68000 upon reception of a combination of input pulses (defined by a loadable bit mask) or to latch the lines so the unit can be polled.

In practice the unit was polled because of problems associated with the asynchronous nature of interrupts.

3 Conclusion

The apparatus has been operating reliably for almost 18 months. The readout time for one pixel is 500 nS and a frame from the RA256 can be read in 35 mS. The transfer time of a full frame to the 11/23 is approximately 2 seconds, a compressed frame is transferred considerably quicker.

There are limitiations with its operation : the lack of ability to have a triggered read and the speed of the readout.

It would prove very difficult to provide a triggered read due to the design of the Reticon chip itself. Although it has

a frame-reset control this is not used due to timing requirements in its application.

With the current DRAM in the VME system, the readout speed is limited to 1 microsecond per 16-bit word. This is much slower than the access time of the memory, but allows for increased access time when a refresh cycle is in process.

Cosmic ray tracks and pair production from cosmic rays have been seen in the avalanche chamber, but the camera has not yet been successfully used on the scintillating glass detector.

4 Future improvements

A fast-access static memory board is under construction which will allow the reticon to be clocked at its maximum rate of 5 MHz. A unit which will allow background subtraction and frame compression 'on the fly' is also under construction, and this will speed up the data rate considerably. A stand alone VMEbus system with its own integral 40 Mbyte Winchester hard disk drive and graphics capability is being developed. This can boot an operating system from the hard disk and will allow data acquisition to be independant of the LSI 11/23.

5 References

1. R.S.Gilmore et Al. An optical readout for accurate positioning of UV photons in an avalanche chamber. NIM 206 p189 (1983).

2. T.K. Gooch Ph.D. Thesis. Bristol University (1984).

3. T.K. Gooch et Al. A multistep avalanche chamber with optical readout for use as a 2-dimensional vuv photon or particle track detector. To be published in NIM.

4. R.Ruchti et Al. Scintillating glass fibre-optic plate detectors for active target and tracking applications in high energy physics experiments.

5. Proxifier BV 25 reference sheet. Proxitronic, Rudolf-Diesel StraBe 23, D-6108 Weiterstadt.

6. Reticon RA256 preliminary data sheet. EG+G Sunnyvale California.

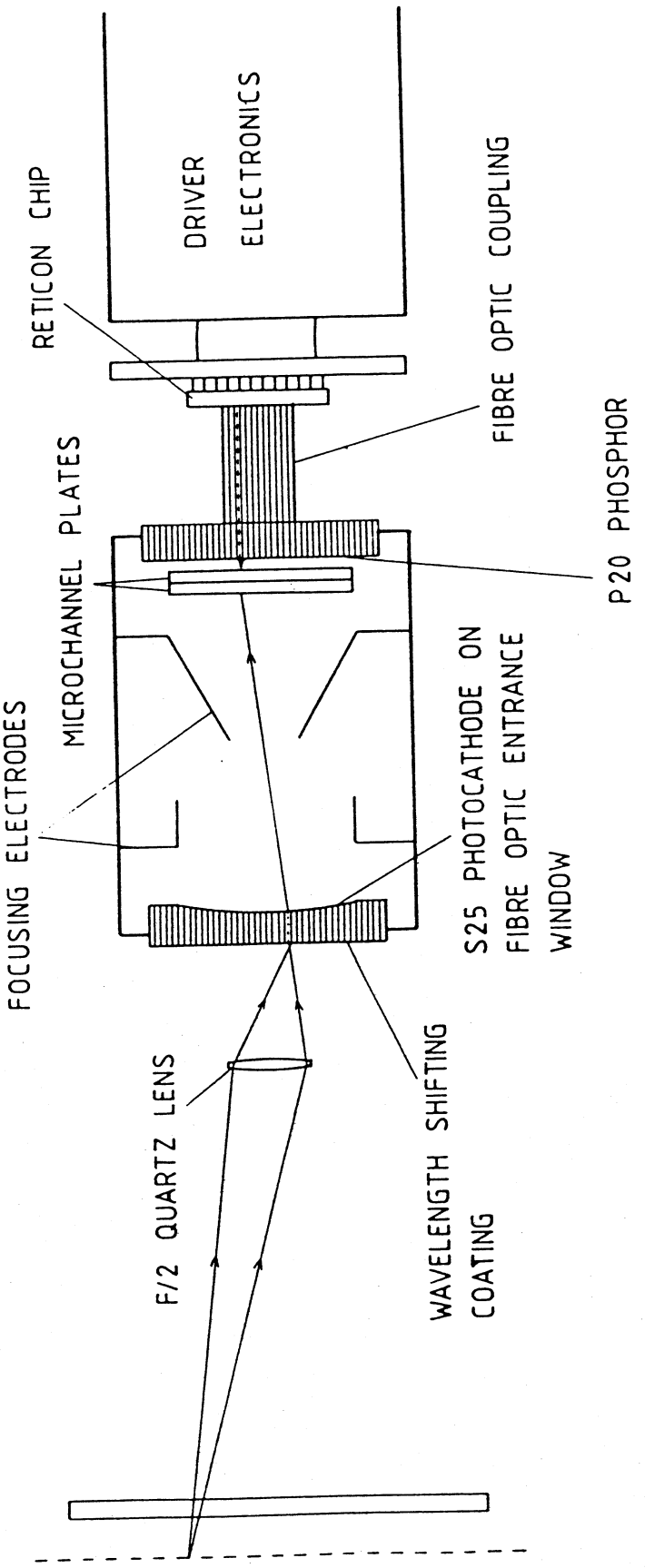
DRIVER ELECTRONICS
RETICON CHIP
FIBRE OPTIC COUPLING
MICROCHANNEL PLATES
P20 PHOSPHOR
FOCUSING ELECTRODES
S25 PHOTOCATHODE ON FIBRE OPTIC ENTRANCE WINDOW
F/2 QUARTZ LENS
WAVELENGTH SHIFTING COATING
IMAGE INTENSIFIER TUBE

Fig. 1

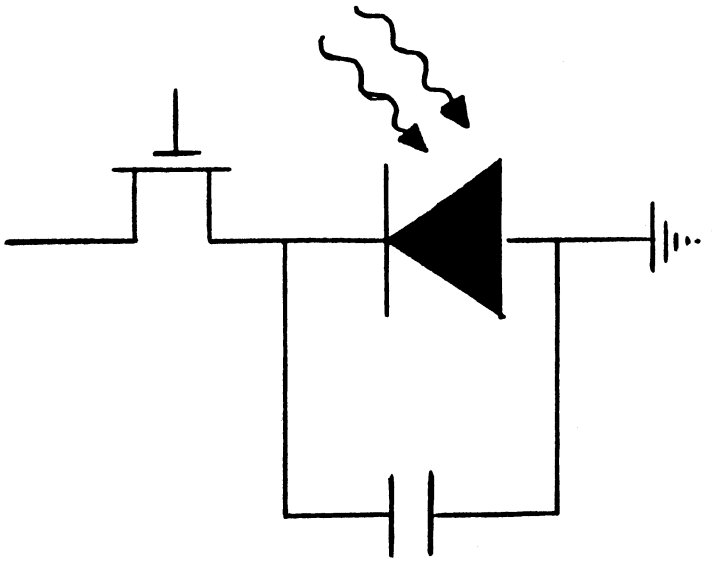

Fig. 3

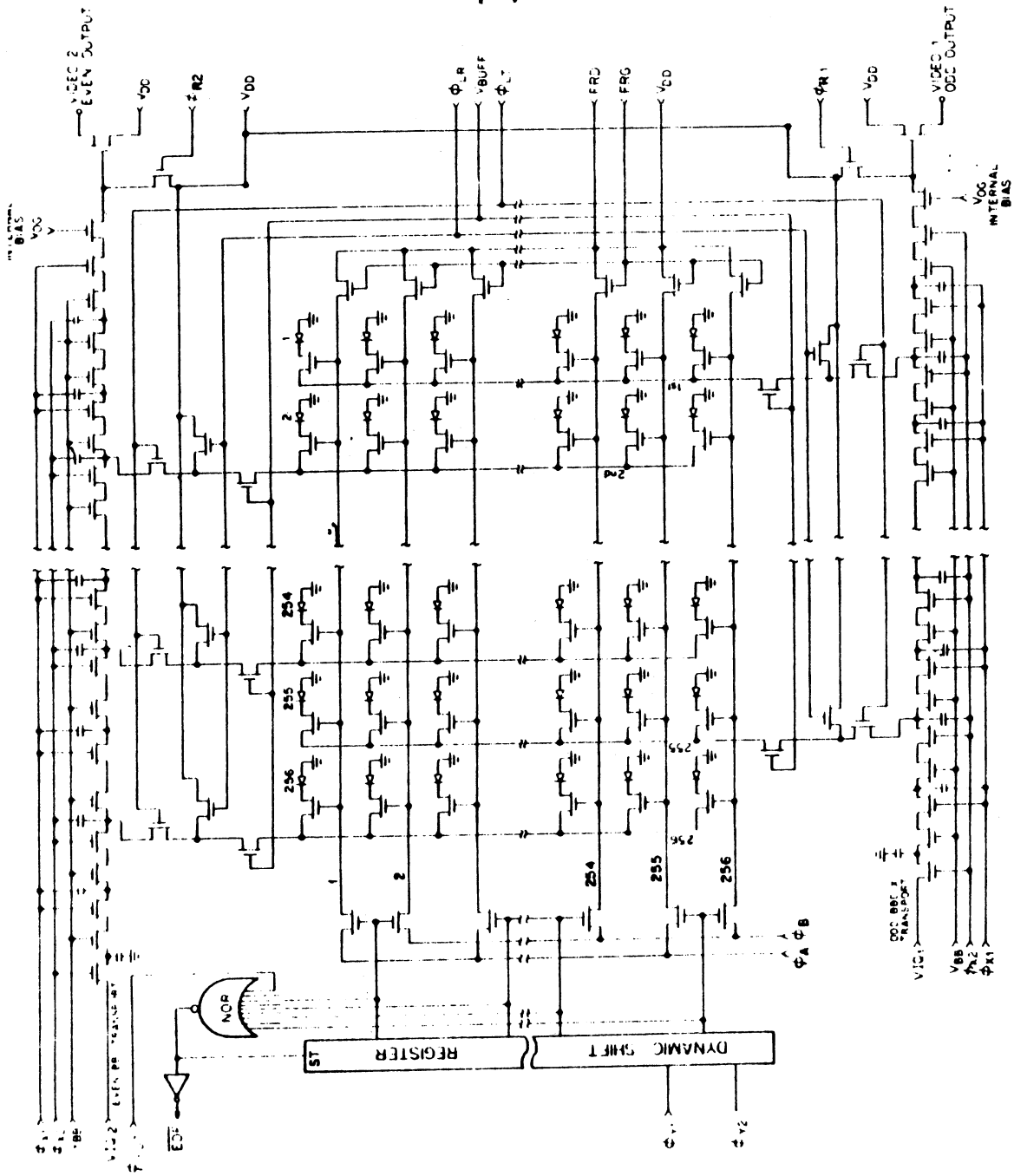
REGISTER
DYNAMIC SHIFT
NOR
ST
VIDEO 2 EVEN OUTPUT
VIDEO 1 ODD OUTPUT
VOG INTERNAL BIAS
VDD
254
255
256

Fig. 2

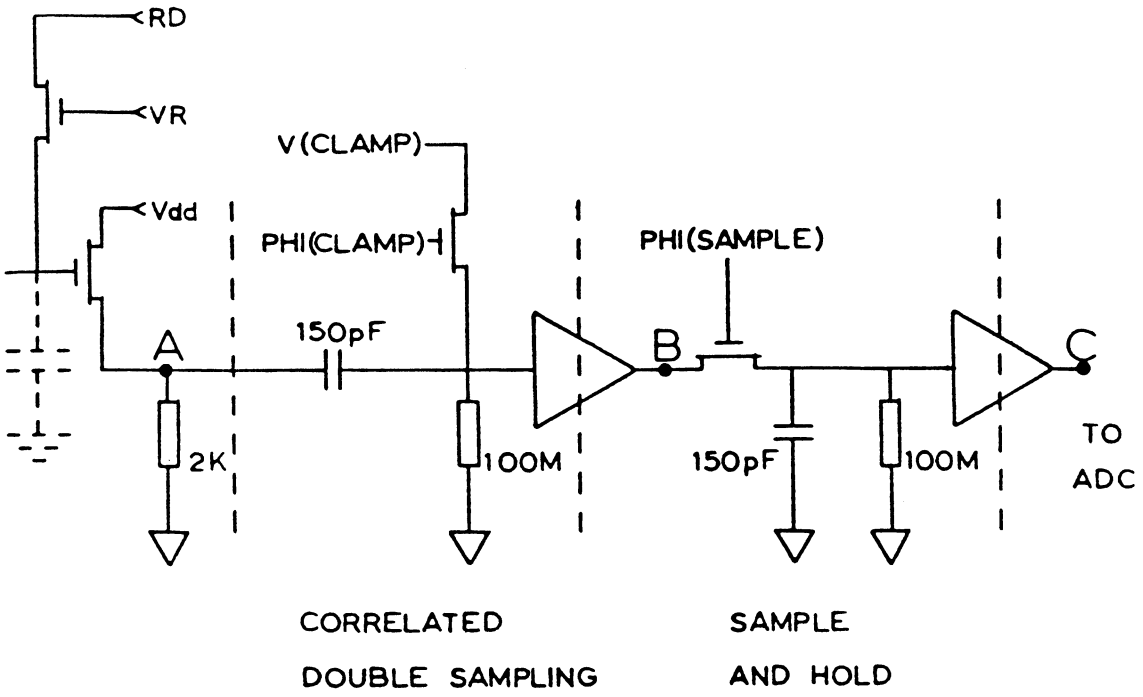
RD
VR
V(CLAMP)
Vdd
PHI(CLAMP)
PHI(SAMPLE)
A
150pF
B
C
2K
100M
150pF
100M
TO
ADC
CORRELATED
DOUBLE SAMPLING
SAMPLE
AND HOLD

Fig. 4

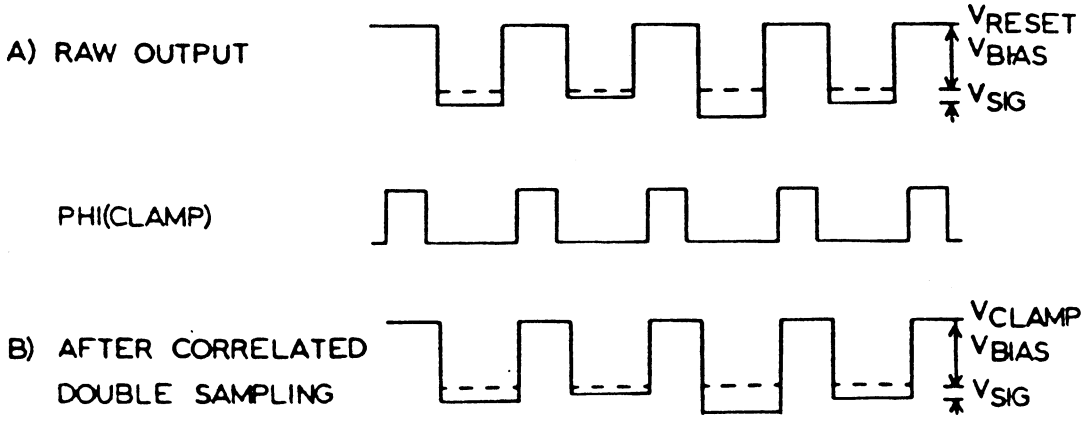
A) RAW OUTPUT
VRESET
VBIAS
VSIG
PHI(CLAMP)
B) AFTER CORRELATED
DOUBLE SAMPLING
VCLAMP
VBIAS
VSIG

Fig. 5

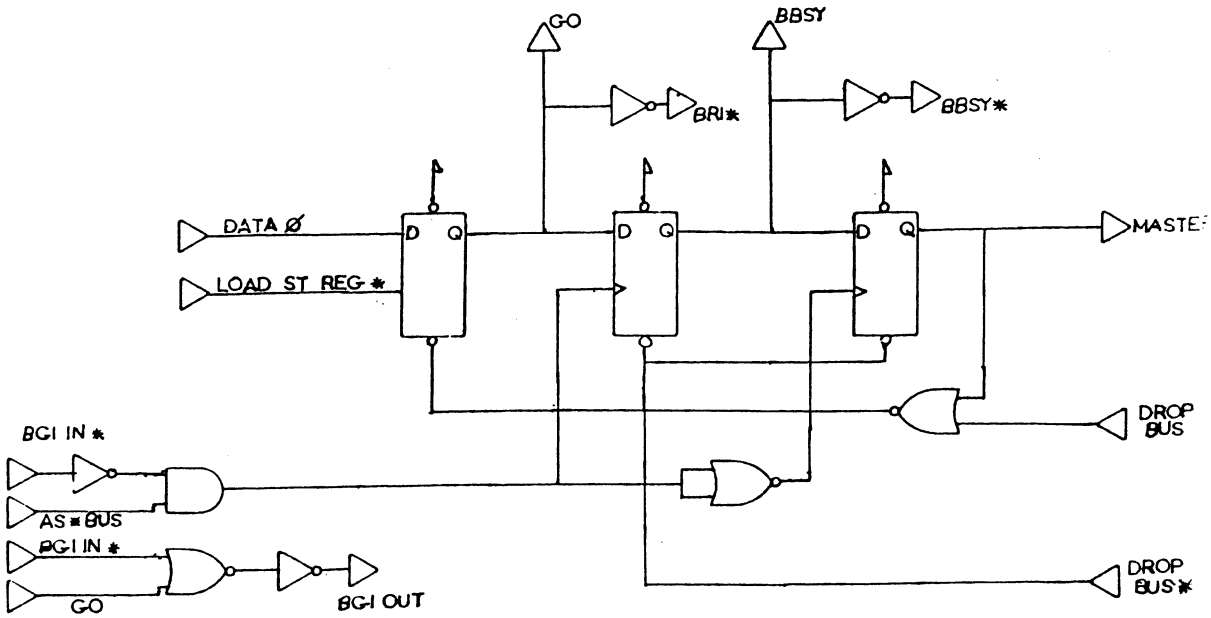

Fig. 6

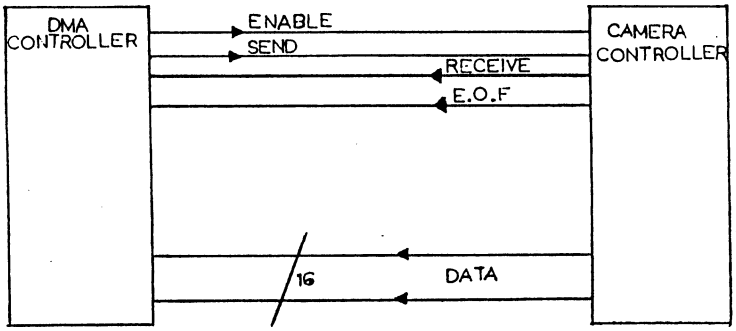

Fig. 7

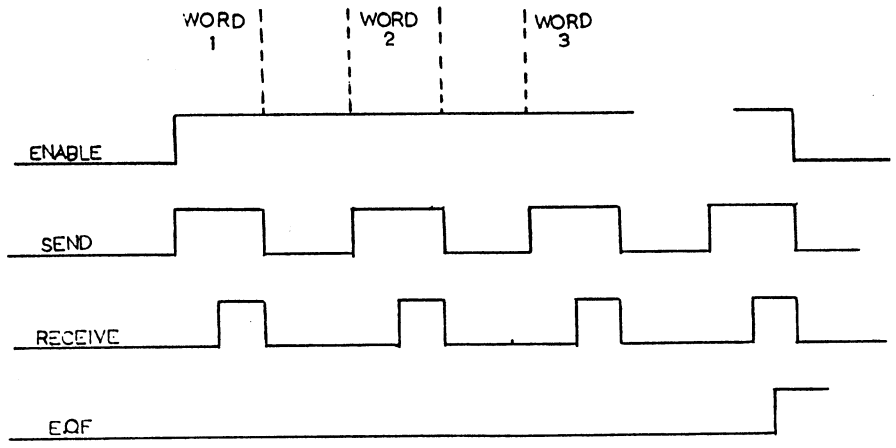

Fig. 8