On-chip Phase Locked Loop (PLL) design for clock multiplier in CMOS Monolithic Active Pixel Sensors (MAPS)

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Abstract

In a detector system, clock distribution to sensors must be controlled at a level allowing proper synchronisation. In order to reach theses requirements for the HFT (Heavy Flavor Tracker) upgrade at STAR (Solenoidal Tracker at RHIC), we have proposed to distribute a low frequency clock at 10 MHz which will be multiplied to 160 MHz in each sensor by a PLL. A PLL has been designed for period jitter less than 20 ps rms, low power consumption and manufactured in a 0.35 µm CMOS process.

I. Introduction

CMOS MAPS are foreseen to equip the HFT (Heavy Flavor Tracker) of the vertex detector upgrade of STAR (Solenoidal Tracker at RHIC) experiment at RHIC (Relavistic Heavy Ion Collider) [1], [2] (Figure 1a). In order to achieve a vertex pointing resolution of about, or better than, 30 µm, two nearly cylindrical MAPS layers with average radii of about 2.5 cm and 8 cm will be inserted in the existing detector. These two layers will consist in 10 inner ladders and 30 outers respectively. Every ladder contains 10 sensors of ~ 2 cm x 2 cm each (Figure 1b).

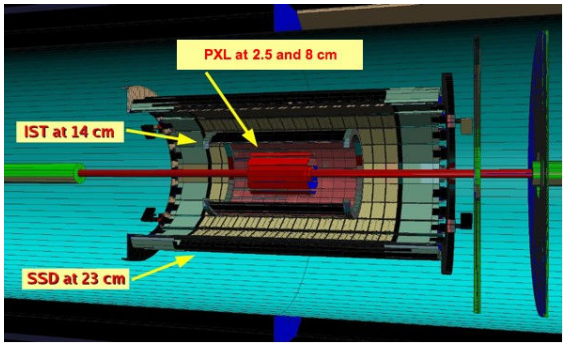
The MAPS named Ultimate will integrate a large area pixel array with column-level discriminator, a zero suppression circuit and a serial data transmission [3]. The sensors readout path requires sending data over a 6-8 m LVDS link at a clock frequency of 160 MHz. Inter sensors data skew and clock jitter have to be controlled precisely in order to ensure the synchronization.

A PLL clock multiplier, which generates the 160 MHz clock frequency from a relatively low frequency input clock at 10 MHz, will be implemented on each sensor. Using a low frequency input clock reduces the problems of electromagnetic compatibility (EMC) related to the integration density, high speed transmission and coupling with the environment. The same clock will also equip an optional 8B/10B data transmission block implemented in Ultimate.

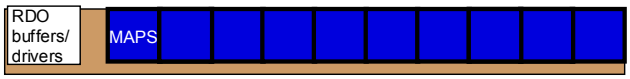
The PLL specifications in MAPS are: a period jitter less than a few tenth of ps rms, low power consumption and specific form factor for the layout.

A first prototype of charge-pump PLL circuit was designed and fabricated in a 0.35µm CMOS process. In order to reduce the PLL noise coming from supply line, two on-chip voltage regulators are implemented to provide stable power supplies for the VCO (Voltage Controlled Oscillator) and the Charge-pump blocks. This technique allows reducing the PLL jitter as long as the voltage regulator has a very good PSNR (Power Supply Noise Rejection) performance.

The first part of this paper presents the PLL architecture (section II) and the main building blocks (III, IV) whereas the second part describes the measurements (section IV).



(a)



(b)

Figure 1: (a) STAR tracking upgrade, (b) Ladder with 10 MAPS sensors (~ 2×2 cm each)

II. The PLL architecture and features

The PLL clock multiplier block diagram is presented in Figure 2.

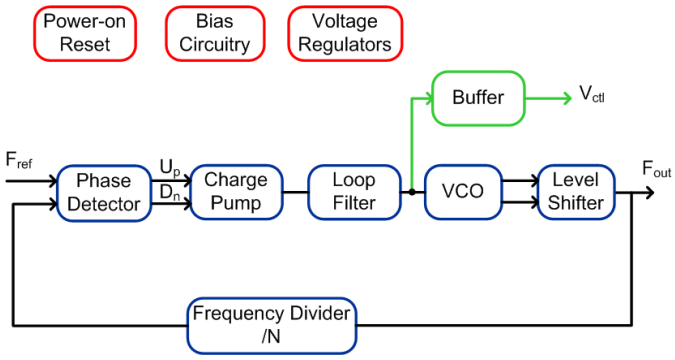


Figure 2: Clock multiplier block diagram

The loop is composed of a phase-frequency detector, a charge pump, a loop filter, a VCO, a level shifter and a frequency divider. A Power-on Reset block generates a reset signal when the power is applied to the PLL. This reset is

provided to the frequency divider and the loop filter in order to ensure that the PLL starts operating in a known state. A bias circuitry provides the currents to the charge pump and the VCO.

Various noise sources within the PLL contribute to the jitter and phase noise. As shown in [4] for high frequencies system, the effect of electronic noise on the jitter is typically much less pronounced than that due to substrate and power noise.

In MAPS sensor, supply and substrate noise is a major noise source. It results mainly of voltage fluctuations on the supply lines due to large current transients in digital and mixed circuitries.

The VCO has the most significant contribution to noise which should be minimized by choosing design architecture less sensitive to supply and substrate noise like differential structure. Electronic noise will also be minimized in the design. Besides, a regulated voltage supply line for the VCO has been implemented to reduce the noise originating from supply line. Moreover, stable dynamics and voltage control range could be obtained as long as the regulated power supply is insensitive to process, voltage and temperature variation.

The charge pump is also sensitive to the supply noise. The ripple noise in the power supply will create ripple on the control voltage of the VCO through charge pump. Providing a stable supply line is also required for the charge pump. In order to get better current matching and a wide enough control voltage range, charge pump needs relative higher voltage headroom than the VCO.

Two voltage regulators were implemented to provide stable voltage supplies to the analogue part as shown in Figure 3. The first regulator with low dropout voltage will provide the supply voltage VDDP for the charge pump. The second regulator with high PSNR performance will generates the supply voltage VDDV for the VCO and the bias circuitry. Using two linear regulators in series allows doubling the PSNR of second regulator if they are identical. VDDD is the digital power supply which provides the first regulator and the other sub-blocks.

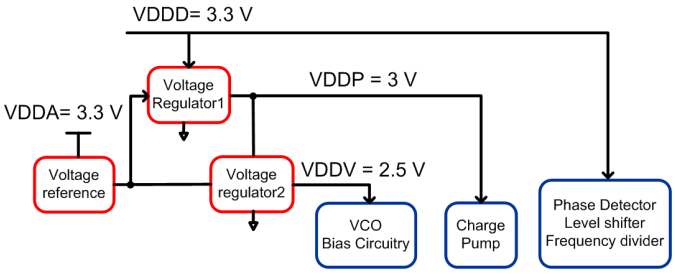


Figure 3: Power supplies distribution of PLL sub-blocks

III. The Voltage Regulator

The Figure 4 shows the schematic of the regulator. It consists of the voltage reference provided by a bandgap reference circuit (not shown), the error amplifier, the pass transistor, the voltage divider R1-R2, and the load capacitor. The loop ensures that the output voltage is always at the appropriate voltage by modulating the gate potential of the pass transistor. The regulator topology is conceptually similar to a two-stage amplifier.

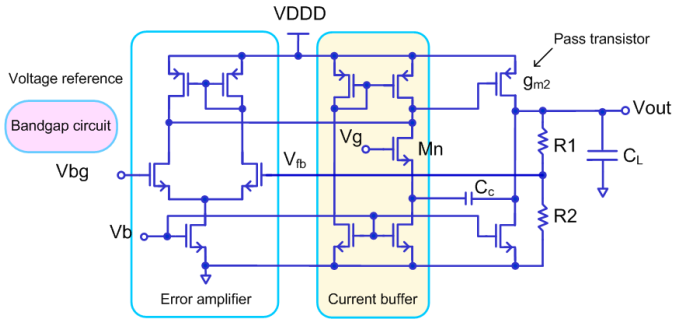


Figure 4: Schematic of the voltage regulator

Several specifications determine the performances of the regulator. For use in the charge pump PLL application, a high power supply noise rejection is required.

In the closed-loop configuration, the output ripple, noted $Vout_R$ can be estimated by:

$$Vout_R \cong \frac{1}{\beta}\left(Vbg_R + \frac{VDDD_R}{PSRR}\right)$$

Where $\beta = R_2/(R_1+R_2)$ is the feedback factor, $VDDD_R$ and Vbg_R are the ripple voltages on the power supply line and the voltage reference, respectively.

A high PSRR (Power Supply Rejection Ratio) for the two-stage amplifier will reduce the output ripple of the regulator. The regulator architecture uses a current buffer in series to the Miller compensation capacitor C_c to break the forward path and compensate the zero [5]. This compensation scheme seems to be very efficient both for gain-bandwidth improvement and for high frequency PSNR. The disadvantages of this technique are a slight increase in complexity, noise and power consumption.

The Figure 5 shows the simulated PSNR for the VCO supply voltage. Table1 summarizes the voltage regulator performances. Figure 6 presents the measured PSNR for the VCO and CP blocks.

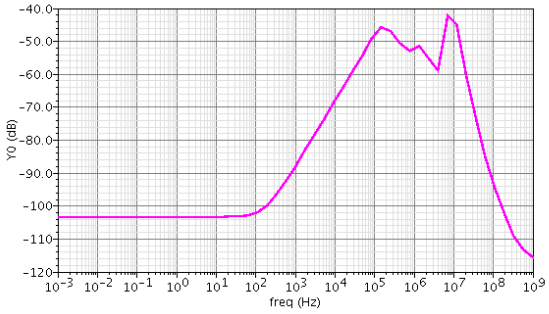


Figure 5: Simulated PSNR of VCO supply voltage

Table 1: Regulator performance for VCO supply

Voltage regulator area	0.15 mm^2
Static current consumption	780 µA
Maximum output current	14 mA
PSNR (measured)	-30 dB

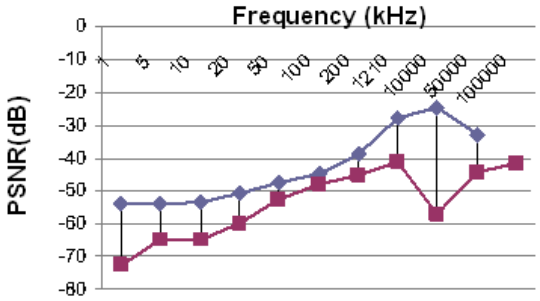


Figure 6: Measured PSNR for the VCO supply (red curve) and CP supply (blue curve)

IV. PLL BUILDING BLOCKS DESCRIPTION

The detailed architecture of the PLL is shown in Figure 7.

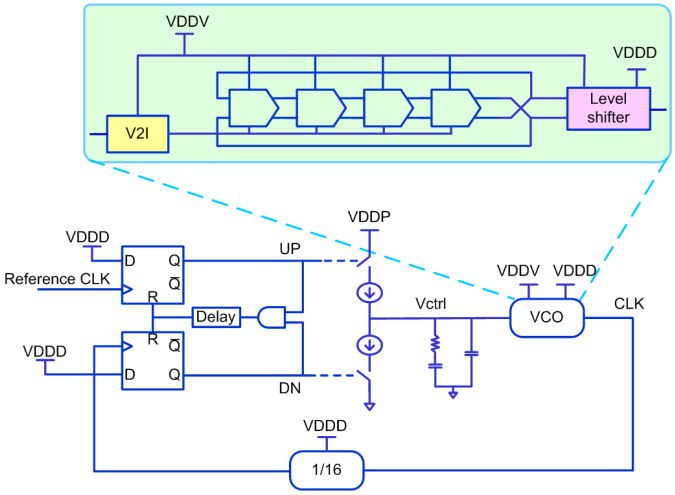


Figure 7: PLL core

A. Phase-Frequency Detector and Charge Pump

The phase-frequency detector uses a tri-state logic block (see Figure 7). The UP and DN signals controls the charge pump. Two D flip-flops with D=1 are triggered by two clock signals which are compared. Ideally, the three states are UP, DN and high impedance. If the reference clock leads the feedback clock, the UP state is generated while DN state is produced for the opposite condition. The filter is in high impedance state at steady state. In order to avoid the dead-zone around zero-phase error leading to increased noise, the forth state where the UP and DN pulses are "high" simultaneously is enlarged by inserting a delay in the reset path. This ensures that the switches in the charge pump could be opened even if a tiny phase error exists between the reference clock and the feedback clock.

The delay time has been optimized in order to minimize the dead zone and to limit the perturbation on the control voltage in the steady state of the PLL.

The charge pump schematic, depicted in Figure 8 (b), uses a dummy switch structure to limit the charge injection and clock feedthrough mismatch [6].

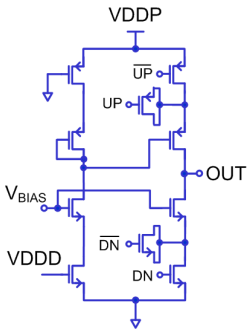


Figure 8: Charge pump schematic

The simulation result of the charge pump phase-detector presented on Figure 9 shows that the dead zone is eliminated and a phase difference (systematic offset) of -2.5 degree exists between reference and feedback clock.

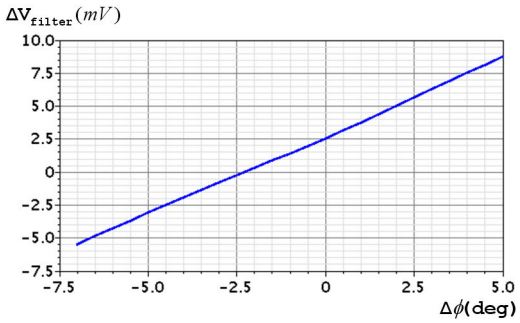


Figure 9: Simulation of charge pump phase-detector

B. Voltage controlled oscillator

The PLL uses a 4 stage differential ring oscillator for the VCO. The design of the VCO was optimized for low noise, low common-mode sensitivity and low power dissipation.

The delay cell, shown in Figure 10 (a), contains a source coupled pair with resistive load elements called symmetric loads [7], [8]. Their I-V characteristics are symmetric around the centre of the voltage swing. Linear controllable resistor loads are desirable to achieve supply noise rejection in differential delay cell because the common-mode noise is converted into differential-mode noise by the non-linearity of the load. The differential-mode would affect the cell delay and then produce timing jitter. By using symmetric loads, the first order noise coupling terms are cancelled out, and then reducing the jitter caused by the common-node noise present in the supply line. The cell delay changes with the VBIAS since the effective resistance of the load elements vary as the VBIAS. With the power supply VDDV as the upper swing limit, the lower swing limit is symmetrically opposite to the VBIAS. The VBIAS is generated dynamically by a replica bias circuit depicted in Figure 10 (b). A controllable tail current in the delay cells and the bias circuit is used to adjust the cell delay. The output voltage swing is relatively maintained constant by varying the active resistance of the loads in such a manner that the variation is inversing to the observed current change. The voltage to current converter is shown on Figure 10 (c). This circuit provides a first-order linear relationship between the oscillation frequency and the

control voltage. An additional current in the converter make the tuning of the VCO more flexible.

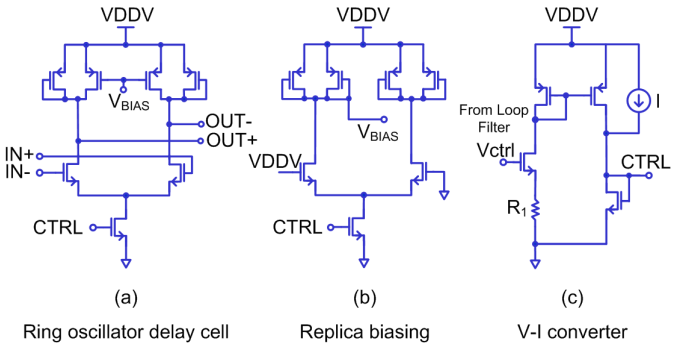


Figure 10: VCO topology

The Figure 11 shows the VCO tuning range from 60 MHz to 230 MHz is obtained by simulation.

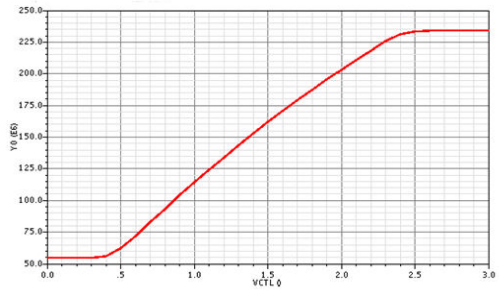


Figure 11: VCO simulation: Freq. (MHz) versus Control Voltage

V. PLL MEASUREMENTS

The proposed PLL with on-chip voltage regulator has been implemented in AMS (Austria-Micro-Systems) 0.35µm CMOS process. The PLL core area is 0.42 mm^2 (1900 µm x 220 µm) (see photograph Figure 12). The regulator's area represents about 35% of the total area.

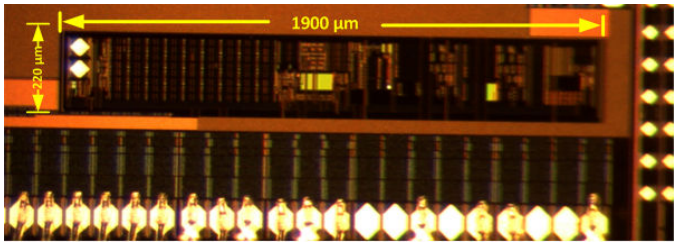


Figure 12: Clock multiplier photography

The PLL locking range is measured from 138 to 300 MHz at room temperature. The frequency range shifts of about 80 MHz upwards compared with the simulation results presented in Figure 11. It might result of the overestimation of the parasitic capacitances in the VCO design. Table 2 shows that the PLL locking range is relatively stable in temperature.

Table 2: PLL locking range as function of temperature

Temperature (°C)	Lower limit (MHz)	Upper limit (MHz)
0	130	295
20	138	298
45	140	297

As shown in Figure 13, the PLL locking time is about 60 µs and is in good agreement with the simulation.

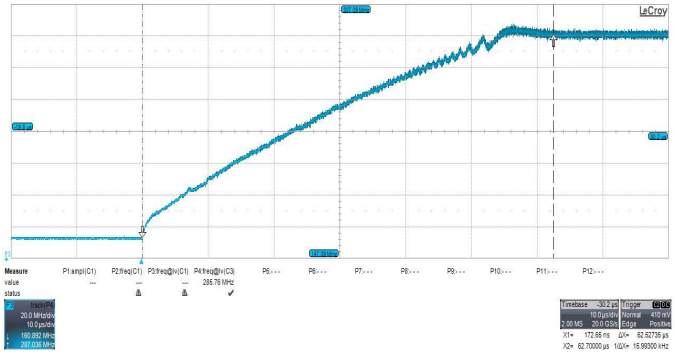
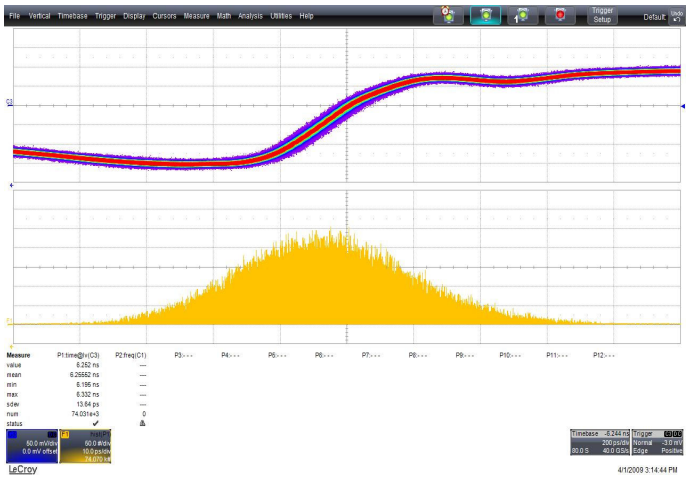
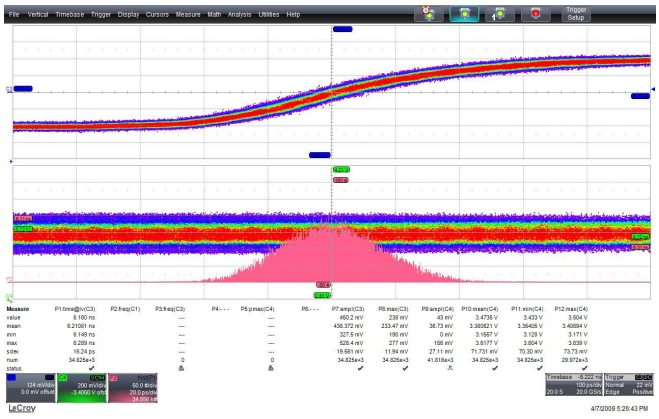


Figure 13: Measured PLL locking time (the reference clock jumps from 10 MHz to 16.7 MHz.) (10 µs / div)

The Figure 14 presents the period jitter measured with a digital scope in two conditions and the Table 3 summarizes clock jitter as function of the reference frequency at room temperature. Table 4 shows period jitter as function of the frequency of the perturbation. The results show that a period jitter of 13.5 ps rms was measured for a stable 3.3 V supply voltage for a 160 MHz output clock. The period jitter with a 400 mV, 10 kHz frequency square wave on the supply voltage is 16.24 ps rms and increases slightly compared with the stable supply voltage.



(a) period jitter with a stable 3.3 V supply voltage.



(b) period jitter with a peak amplitude of 400 mV, 10kHz square wave on the power supply line.

Figure 14: Measured period jitter at 160 MHz PLL clock with and without noise

Table 3: Jitter measurement summary

Reference freq.(MHz)	9	10	12	14	16	18
PLL clock (MHz)	144	160	192	224	256	288
Period jitter (ps rms)	12.8	13.5	11.6	13.2	11.7	12.2
Period peak-peak jitter (ps)	124	126	113	107	97	111
Cycle to cycle jitter (ps rms)	22.7	22.0	23.1	20.6	21.5	21.5
Cycle to cycle peak-peak jitter at 10^{-12}BER (ps)	323	317	326	293	318	307

Table 4: Measured period jitter with a peak amplitude of 400 mV square wave at 160 MHz at different noise frequency

Noise frequency (kHz)	0.1	1	10	100	1000	10000
Period jitter (ps rms)	18.8	18.5	16.2	15.5	15.6	15.3
Period peak-peak jitter (ps)	148	131	140	113	132	127

Table 5 summarizes the PLL performance.

As the PLL prototype shares power supply with the MAPS sensor, it has not been possible to measure directly the PLL supply current. The power dissipation of the PLL has been estimated at 7mW.

Table 5: PLL performance summary

Technology	0.35µm CMOS process
PLL die area	0.42 mm^2
Multiplication factor	16
Locking range	138 MHz – 300 MHz
Power supply requirement	3.0 – 3.6 V
Power consumption (estimated)	7 mW at 160 MHz
Period jitter	13.5 ps rms
Period jitter with noise*	16.2 ps rms
Locking time	60 µs

*a 400 mV, 10 kHz square wave applied on supply power, room temperature

VI. Conclusion and Perspective

A PLL clock multiplier designed for CMOS MAPS has been presented in this paper. On-chip voltage regulators provide two stable power supplies to the VCO and the charge pump. Using the on-chip regulator increases the area of 35% and the power consumption of 20%. The total power consumption has been estimated at 7 mW.

Experimental results showed that for the output clock at 160 MHz PLL clock, the period jitter is 13.5 ps rms and increases slightly in an emulated noisy power supply environment. With this low jitter performance, the PLL can be employed as clock multiplier in MAPS.

In the future, the same PLL clock will also equip a serial transmitter block. In order to ensure the data transmission with low error rate, the PLL should be optimized by characterizing the transmission system with cable connections and receivers. We plan to design a new prototype to enhance the jitter by using a programmable loop bandwidth and by optimizing the VCO.

VII. References

[1] M. Winter et al., Vertexing based on high precision, thin CMOS sensors, in Proceedings of the 8th ICATPP, Como, Italy, October 2003.

[2] L.C. Greiner et al., STAR vertex detector upgrade development, in Proceedings of Vertex 2007, Lake Placid, NY, U.S.A., September 23-28 2007, PoS(Vertex 2007)041.

[3] Ch. Hu-Guo et al., CMOS pixel sensor development: a fast read-out architecture with zero suppression, 2009 JINST 4 P04012doi: 10.1088/1748-0221/4/04/P04012

[4] F. Herzel and B. Razavi, A study of Oscillator jitter due to supply and substrate noise, IEEE Transactions on Circuits And Systems-II: Analog and digital signal processing, vol. 46, N°.1, January 1999

[5] G.Palmisano and G.Palumbo, A compensation strategy for two-stage CMOS Opamps based on current buffer, IEEE Transactions on Circuits And Systems-I: Fundamental, theory and applications, Vol. 44, N°.3, March 1997

[6] V.Von Kaenel et al., A 320 MHz, 1.5 mW at 1.35V CMOS PLL for Microprocessor Clock Generation, IEEE Journal of Solid-State Circuits, Vol. 31, N°.11, November 1996

[7] J.G. Maneatis and M. A. Horowitz, Precise Delay Generation Using Coupled Oscillators, ISSCC 93 / Analog Techniques/ Paper TA 7.5

[8] J.G. Maneatis, Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques, IEEE Journal of Solid-State Circuits, Vol. 31, N°.11, November 1996.