

The Control System for a new Pixel Detector at the sLHC

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Abstract

For the upgrade of the LHC, the sLHC (super Large Hadron Collider), a new ATLAS Pixel Detector is planned, which will require a completely new control system. To reduce the material budget new power distribution schemes are under investigation, where the active power conversion is located inside the detector volume. Such a new power supply system will need new control strategies. Parts of the control must be located closer to the loads. The minimization of mass, the demand for less cables and the re-use of the outer existing services are the main restrictions to the design of the control system. The requirements of the DCS (Detector Control System) and a first concept will be presented. We will focus on a control chip which necessarily has to be implemented in the new system. A setup of discrete components has been built up to investigate and verify the chip's requirements. We report on the status of the work.

I. INTRODUCTION

The innermost part of the ATLAS tracking system for the sLHC upgrade is a pixel detector. The precise layout and geometric dimensions are still under discussion. However an interesting option foresees five cylindric shells around the interaction point in the barrel part and five disks per end cap. A support tube will divide the detector into two parts: an insertable part comprising of shell 0 and 1, and a fixed part containing the rest. In the barrel staves carry the individual detector modules (see Figure 1), in the end caps the modules are installed on disks. Staves, half staves and disks sectors are forming the DCS relevant groups. The smallest unit on which DCS can act on will be one detector module. Typically a detector module will be read out via four front end chips, while the innermost layer likely will have only one front end per detector tile. Depending on the layer up to sixteen detector modules form a half stave.

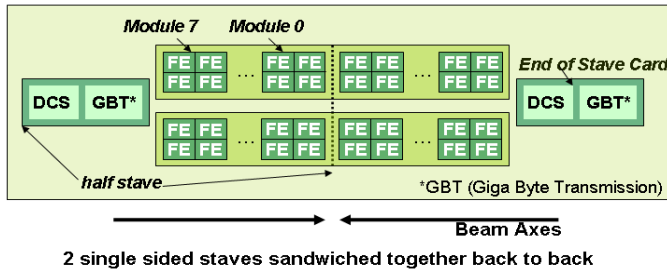


Figure 1: Pixel stave of the outer layers (2,3 and 4)

At first the data collected by the front end chips are transferred to a controller, which is located at the EoS (End of

Stave) card. A possible candidate for the EoS controller is the GBT (Giga Bit Transmission) chip [1]. Finally the opto electrical transceiver, called opto board, which is located a few meters away from the interaction point, sends the data to the control room for further processing and storage.

Besides the detector modules themselves, the End of Stave card with its electronics, and the opto board, monitoring of the environment and of the cooling are subjects of the detector control.

II. REQUIREMENTS

For each DCS subject we identified the parameters which need to be monitored or which require to be controlled (either the set value must be changeable and/or an operator must be able to switch a channel on and off), see Table 1.

For each parameter one has to define its granularity, e.g. whether a value is available per front end chip or just per stave. One has to evaluate where the processing of data takes place, locally inside the detector volume or at the power supply level, which typically will be installed in the counting rooms. In the following we will concentrate on all quantities which can't be controlled in the counting room. Furthermore the level of reliability and the life time – whether an information is permanently available or just for special periods - must be defined for all DCS items.

The control system must operate and react safely in all use cases from the assembly of the detector and qualification tests to the commissioning phase and normal data taking. A limited operation without a working cooling system must be possible. Tuning and calibration must be supported. It might happen that just parts of the system are available and will be operated.

Table 1: Items of the Detector Control System

	to be monitored	to be controlled
detector module	HV voltage & current	selectable voltage on/off
	LV voltage & current	selectable values on/off
	temperature	
end of stave card	voltage & current	on/off
	temperature	
		reset
opto board	voltages & currents	selectable voltage on/off
	temperature	
		reset
environment & cooling	humidity	
	temperature	

III. PROPOSAL FOR A CONTROL SYSTEM

Our starting point is the actual detector where DCS fulfils all needs and supports the data taking in a reliable way. Therefore monitoring and control of the different functions in the new system should be provided with the same reliability and the same level of granularity as for the actual detector. Especially monitoring and control per detector module are essential, e.g. the current consumption of the low voltage tells the operator whether a module is properly configured.

While the high voltage reading and setting will take place outside the detector volume, typically even inside the HV power supplies themselves, the low voltage monitoring and control require a data processing close to the detector modules due to the voltage drops.

Currently two powering methods are under discussion: a parallel powering with DC-DC converters or the serial powering scheme. As the choice of power distribution has a direct impact on the monitoring and control possibilities the two powering schemes must be investigated separately. It would be counterproductive if one studies new powering schemes to reduce the material in the detector and increases the DCS cable volume at the same time. Therefore to both efforts should be the attempt to avoid additional lines in common.

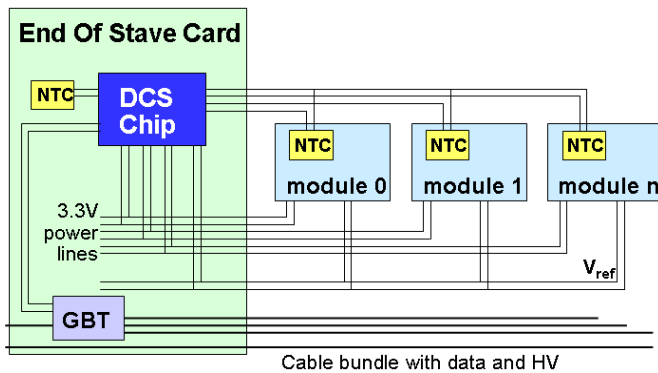


Figure 2: DCS for DC-DC powered modules

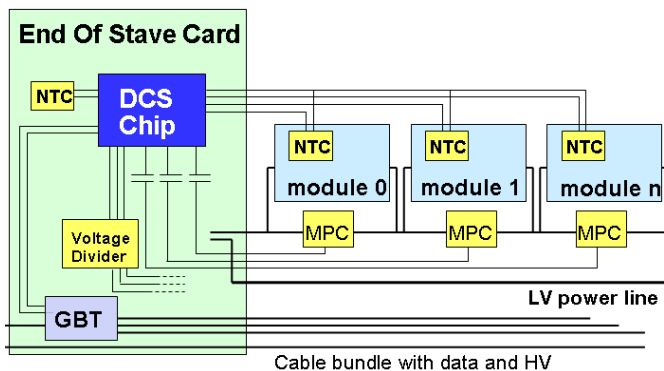


Figure 3: DCS for serial powered modules

A. DCS for DC-DC powered modules

In the case of the DC-DC scheme the power reduction is performed by two stages of DC-DC converters. While the first

stage is located inside the front end chips, the second is foreseen near the detector.

As the voltages are supplied in parallel per detector module and the cable bundle must be routed through the End of Stave card a monitoring of the low voltage per module is possible at the End of Stave card, see Figure 2. Monitoring can be done by a DCS chip, mounted on the EoS card. In this way just very short lines on the EoS card itself are necessary to provide a LV reading per detector module. Monitoring of the reference voltage V_{ref} can be performed in the same way. Because individual lines are routed to the outside, the control and current monitoring can take place at the far end. Just for first system tests it might be useful to foresee a local current monitoring in order to debug the system.

Figure 2 depicts also the temperature monitoring of the detector modules. Each detector tile is equipped with an NTC (Negative Temperature Coefficient) sensor. The monitoring of the NTCs will require $(n+1)$ lines for n detector modules. These lines are routed locally between the detector modules and the EoS card. As these lines are just monitoring connections, very small cable diameters are sufficient.

B. DCS for serial powered modules

In the case of serial powered modules all modules of a chain are supplied by one power line and its return. They are connected to a current source, which will be located outside the detector most likely in the counting room. Shunt and linear voltage regulators inside the front end chips produce the required voltage. In this way serial powering reduces the power lines and hence minimizes the passive material inside the detector volume. Furthermore the power losses in the cables are reduced. The principal functionality of a serial powered pixel stave has already been proven some years ago, see [2].

Drawback of the serial powering is that an individual disabling per module from the outside is not possible anymore. A local mechanism is required to switch on/off single modules. The MPC (module protection chip developed by Bonn University [3]) bypasses the module and provides an overvoltage protection. Its bypass circuit must be locally steered. A capacitive coupled DCS chip at the end of stave would be a good candidate. Just one line per module is required, see Figure 3.

Due to the different DC levels of the detector modules their LV monitoring requires a voltage divider between the monitoring lines and the DCS chip inputs. Different from the DCS chip and the MPC, which can be developed in the same deep submicron technology as the front end chips, the voltage divider must be developed in a technology which stands higher DC levels, up to 20 V depending on the number of detector modules which are serialized.

To avoid additional sense lines between the detector modules and the EoS card different 'spying' methods are under investigation. As the HV return line, the data lines and the bypass control line are either on the DC level or depend on the DC level of the dedicated module, they principally offer the possibility for the LV monitoring. As these methods even allow a monitoring closer to the load, it must be

investigated in how far also a DC-DC scheme could benefit from these plans.

As the temperature monitoring is completely independent of the LV powering scheme, it can be the same for both powering schemes. This gives in total $(2n+1)$ DCS lines between detector modules and the EoS card for n serial powered modules.

C. Overview on the DCS architecture

Besides the detector modules the EoS card, the opto board, and the monitoring of the detector volume and of the cooling are subject to the control system.

The EoS card houses mainly the GBT. Monitoring of its supply voltage and the EoS card's temperature are necessary, additionally a reset to the GBT should be available. These tasks can also be handled by the DCS chip, which is mounted on the EoS card, see Figure 2 and Figure 3.

The DCS needs of the opto boards are similar. Monitoring of the voltages, which supply the different components of the opto electrical transceiver, a reset and the temperature supervision can be performed by a DCS chip installed on the opto board or close to it.

In the case of the environmental and cooling monitoring, which mainly consists of temperature and a few humidity sensors, a DCS chip installed in their vicinity reduces the number of cables, which must be routed to the exterior.

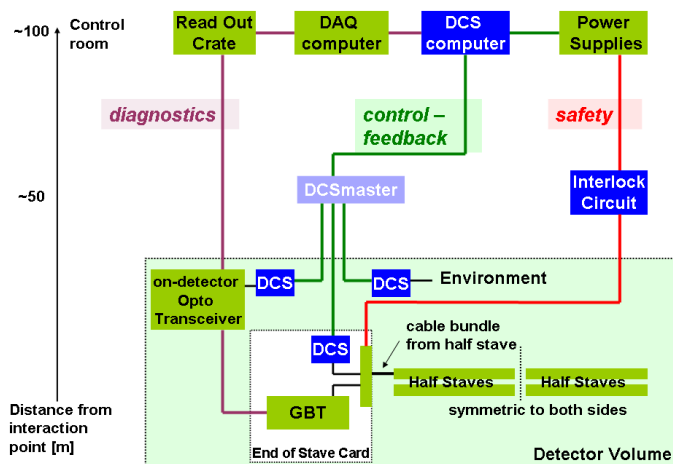


Figure 4: DCS architecture

Figure 4 summarizes the supervision of all DCS items and gives an overview on the general DCS architecture. Three independent paths are built: diagnostics, control and safety.

By the diagnostics path detailed information can be merged into the data stream on request. A temperature and low voltage reading per front end chip could be useful additional information. Several global registers are foreseen in the front end chips, which could also be used for DCS. The DCS data will be merged into data stream. In the off-detector readout processors routines search for DCS data and transfer them to the correct system. It will be a powerful tool to debug, understand and tune the detector, but this information will only be available when the front end chips are correctly configured.

As the control and feedback path contains all parameters which are essential for the operation of the detector, it must be available for all use cases and therefore can't rely on the functionality of the read out chain. It contains setting of values and their monitoring, allows to switch channels on or off, sends a reset to components which are stuck, and monitors temperatures. A high reliability is required. Obviously control and its feedback should have the same granularity. A detector module will be the smallest unit which can be handled independently. The information will be processed either by the power supplies or directly close to the detector modules. Major parts are described in the previous sections. The core of the on detector control will be a DCS chip, which handles the data.

The DCS master as shown in Figure 4, which might act as a middleman between the front end, the DCS chip, and the DCS computers, can be defined when investigations on the protocol of the DCS chip are further advanced (see also next section).

The safety path is based on interlock circuits. Specially irradiated silicon sensors can be irreparably damaged by heat-ups. To protect the detectors against overheat due to errors in the cooling system, delamination or thermal run-aways a hardwired interlock system is necessary. This independent interlock system should ensure the safety of the detector. As the highest level of reliability is required its active components should be located outside the detector and act directly on the power supplies.

As neither high precision nor high granularity are required two to four temperature sensors could be combined to create one interlock signal. While the average temperature is measured by the interlock system, the temperature per detector module can be measured by the DCS chip [4].

Summarizing, while the level of reliability will be highest for the safety path, it will be high for control and can be lower for diagnostics. The required granularity behaves vice versa. This stands in close relation to the required lifetime. Highest reliability goes with a permanent availability. For values which require a lower level of reliability, normally an intermittent availability is sufficient.

D. Cable balance

As the control should be available for all use cases, the DCS chip should have its own powering lines. Together with the communication lines this results in three to five cable pairs which must be routed from the DCS chip to the external world. Additionally one cable pair per four detector modules should be foreseen for the interlock. The questions, to which location the cables must be routed and where they will be further bundled, are still under discussion. Compared to the actual detector, where three cable pairs per detector module are led towards the outside, this gives an impressive reduction in the number of DCS cables as can be seen in Table 2.

Table 2: DCS cables [pairs] from the end of stave to the exterior

	8 detector modules/DCS chip	16 detector modules/DCS chip
current detector	24	48
DCS chip	3-5	3-5
Interlock	2	4
sum	5-7	7-9

The future detector will be built by a much larger number of detector modules as the current detector: 5888 compared to 1744 modules. However, as the number of cables per detector modules is much smaller, the re-use of the existing external cables, which is one of the boundary conditions for the system design, should be possible. A more detailed analysis should consider the DCS cables of the environmental monitoring and of the on-detector opto transceiver.

Also the number of internal cables from the modules to the EoS card is smaller than in the current detector, where there are 6 lines per detector module compared to a maximum of $(2 + 1/n)$ lines per module, if n modules form a half stave. ($1/n$ is given by the common return line which is shared by n modules). In the case of a DC-DC powering scheme even less cables are necessary. This results in a reduction of at least 50% for the internal DCS cabling.

IV. THE DCS CHIP

As shown in the previous sections a DCS chip would be a good tool to reduce the material inside the detector volume while it supports the new powering schemes in the best way.

A. Requirements

From the units which are supervised by the DCS chip, like the detector modules, the EoS card, the opto board or the environment, the features of the chip follow directly. As one chip design should cover all tasks, the requirement list is a set union of the individual lists:

- about 35 differential ADC channels, 10-12 bit
- about 17 digital outputs
- local clock and V_{ref} for the ADC
- optionally supply of NTCs
- 2 x 16 bit counters
- communication interface, which is able to drive long cables
- all input/output signals should be differential
- chip ID
- low power consumption to allow an operation without cooling
- radiation level $1.3 * 10^{16} n_{eq}/cm^2$, 570 MRad

The harsh radiation environment [5] of the pixel volume is obviously the largest challenge. We aim to use the same deep

submicron process as used for the front end read out chips in order to benefit from the large experience and knowhow, which already exists in this field. Besides the overall radiation hardness special efforts will be necessary to protect the registers of the digital outputs against SEU (single event upsets). It could be fatal for the operation of the detector if a module is switched on or off by error.

To make the DCS chip as fail-safe as possible the minimum of functionality should be foreseen. If possible, complex data processing should be done outside the detector. The smaller the number of active circuits will be, the more robust the design can be. Additionally this will reduce the power consumption. Also the ADC accuracy and the speed of data processing should be further investigated under the aspect of power consumption and possibilities to reduce it.

The main design criterion for the communication interface will be its robustness, while the speed of data transfer is of low importance for slow control data. A good compromise between baud rate and cable length must be found. For the moment we think that SPI and I2C are possible candidates. While SPI might be a bit more robust, I2C has the advantage of less lines.

B. First prototype

As a starting point we defined a DCS prototype chip, whose functional blocks can be seen in Figure 5. As the choice of the communication protocol is still open, an I2C as well as an SPI interface is foreseen. To study the behaviour of the chip in detail all in- and outputs are routed to the outside.

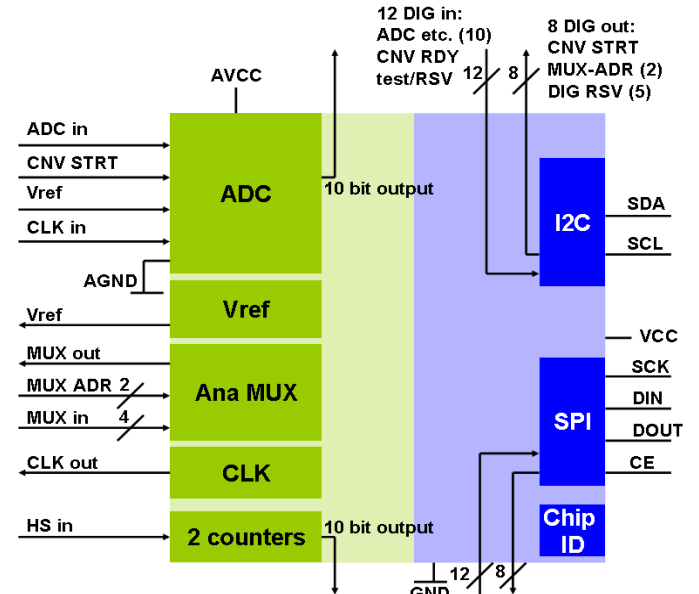


Figure 5: Block diagram of DCS prototype chip

For the first prototype we concentrated on the chip interface. While we implemented a standard I2C protocol, the SPI is modified in so far that it contains slave addresses. Besides that five digital outputs, two counters for the read out of capacitive humidity sensors, and the connections to an external ADC are available. Because almost all components are digital circuits, this first prototype is submitted in a standard (non radiation hard) 350 nm CMOS technology.

The tests which are planned with the prototype can be grouped in two categories, choice of the communication interface and system aspects, which will be described further in the next section. Foreseen tests are:

- Verification of SPI and I2C protocols,
- study impact of cable length,
- build a DCS network,
- control external ADC,
- test digital outputs,
- read out of humidity sensors.

V. THE CONTROL BOARD FOR THE STAVE EMULATOR

To investigate and understand all aspects of a complete pixel stave a stave emulator setup has been developed at Bonn University[6]. This test-bench allows to evaluate the various aspects of data coding, management, and transmission as well as to study questions concerning powering and detector control. The detector modules and the EoS controller are represented by emulator cards. The DCS emulator, called COBOLT (COntrol BOard for the stave emuLaTor) and developed at Wuppertal University, can be connected via an adapter card.

All functionality, which should be inside a later DCS chip, is placed on the small printed circuit board of COBOLT. In the first iteration individual components are used. The aim is to verify that all DCS functionality is covered. Core of the board is an ATmega640V microcontroller including a 16 channel 10 bit ADC. Several plug-ins allow to adapt further measurements, studies of a voltage divider etc..

While continuously testing the interaction between DCS and the overall stave system, the DCS emulator will be replaced step by step by more realistic and final components.

First tests concerning the steering of the bypass control, which is required for a serial powered stave, have been successfully performed. Studies how the monitoring of the module's LV can be done for a serial powered stave are ongoing. As soon as the DCS prototype chip is delivered, it will also be inserted into the emulator system, replacing the microcontroller. A prototype of the DCS master, which will be required to establish the communication to the outer world, is also under development.

VI. SUMMARY & OUTLOOK

The pixel detector which is planned for the sLHC, will require a completely new DCS architecture. Support of the new powering schemes, serial powering or a DC-DC scheme, and the reduction of material inside the active detector volume are the main design criteria.

The DCS items are identified and first requirements defined. We propose a new DCS architecture based on three independent paths: diagnostics provided by the read out system, control and feedback mainly performed by a DCS chip and safety ensured by an hardwired interlock system. From the boundary conditions of the on-detector control the necessity of a DCS chip follows. Its required characteristics are presented.

A first prototype DCS chip has been submitted. The aim is mainly to evaluate the communication interface and to study a DCS network. Furthermore a new prototype will be developed in a radiation hard CMOS technology in order to investigate strategies for SEU save registers and a bit flip resistant data transfer.

At the same time the definition of the DCS master must go on and it should be evaluated in how far the design of a pixel DCS chip can be merged with other developments.

VII. REFERENCES

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