A 5 Gb/s Radiation Tolerant Laser Driver

in CMOS 0.13 μm technology

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Abstract

A laser driver for data transmission at 5 Gb/s has been developed as a part of the Giga Bit Transceiver (GBT) project. The Giga Bit Laser Driver (GBLD) targets High Energy Physics (HEP) applications for which radiation tolerance is mandatory.

The GBLD ASIC can drive both VCSELs and some types of edge emitting lasers. It is essentially composed of two drivers capable of sinking up to 12 mA each from the load at a maximum data rate of 5 Gb/s, and of a current sink for the laser bias current. The laser driver include also pre-emphasis and duty cycle control capabilities.

I. THE GBT PROJECT

The GBT project [1] aims to design a radiation tolerant optical transceiver for High Energy Physics (HEP) experiments. The GBT will provide a bi-directional connection between the front-end electronics and the DAQ, trigger and DCS systems. Therefore experimental data, trigger, timing and control informations will be transmitted over the same physical link.

Fig. 1 shows the GBT architecture. On the detector side the electronics has to be radiation tolerant for both total dose and single event upset (SEU) effects, and therefore a full custom ASIC development is required. In this case the GBT will be based on four ASICs : a photo-diode receiver (GBTIA), a laser driver (GBLD), a main chip with serialiser, deserialiser and protocol handling and a slow control interface (GBT-SCA). On the counting room side, where radiation is not an issue, the GBT functions can be implemented either by the same chip set or by a commercial driver and receiver and by an FPGA-based implementation of the GBT functions.
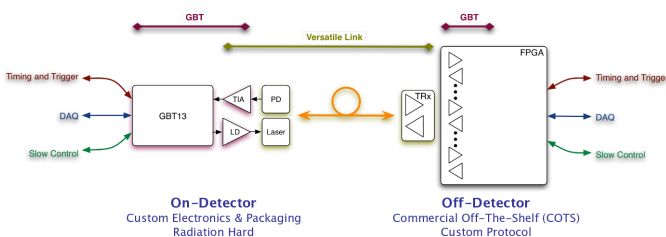

Figure 1: The GBT architecture

II. GBLD REQUIREMENTS

The GBT chip set includes a laser driver targeted at driving both VCSELs and some type of edge-emitting lasers at a maximum data rate of 5 Gb/s, named GBLD.

VCSELs are characterized by a dynamic impedance of the order of tens of ohm and currents of the order of few mA, while edge-emitting lasers have lower impedance (few Ω) and requires higher currents (tens of mA). Therefore a large range of modulation and bias currents is required in order to address both laser types.

The GBLD has to provide laser modulation and bias currents that are programmable in the $2 \div 24$ mA and $2 \div 43$ mA range, respectively, with a 0.16 mA resolution. In order to compensate for high external capacitive loads or asymmetries in the laser diode response, independently programmable pre-emphasis and de-emphasis of the rising and falling edges are also required. The emphasis current has to be in the range $0 \div 12$ mA with a 0.8 mA resolution.

The different requirements from the two laser types has been addressed by splitting the output stage into two identical drivers. Each driver can provide up to 12 mA to the load and has a 50 Ω internal termination. Both drivers are controlled by the same driving signals and the same control DAC. With such an arrangement a VCSEL can be driven by a single driver while the other one can be switched off to reduce power consumption, while an edge emitting laser will be driven by the two drivers in parallel. In the latter case the input impedance is halved, thus obtaining a better impedance matching with the lower dynamic impedance of the edge emitting lasers.

The GBLD is driven by an AC-coupled differential signal. The differential input dynamic range is between 100 mV and 1.2 V_{PP}. The input stage has to be internally biased and terminated.

A 2-wire I^2C protocol has been chosen as the control and configuration interface between the GBLD and the counting room. The configuration registers and the control logic must be protected against SEU.

The GBLD will be packaged in a 4×4 mm^2 QFN24 package. Such a small package limits the maximum die size to 2×2 mm^2.

III. GBLD ARCHITECTURE

The most critical part of the GBLD is the modulator, depicted in fig. 2. The input stage is followed by a pulse width modulation circuit, which allows to change the signal duty cycle by ±15% @ 5 Gbps. The output signal is then split into two path. The first one goes to the pre-driver, which drives the two output stages *A* and *B*. In the second one a delay stage generates a delayed signal which is used by the following differential AND gates to create the emphasis pulses for the rising and falling edges. In this prototype the emphasis driver is connected to the driver B only in order to evaluate the influence of the parasitics added by the driver itself.
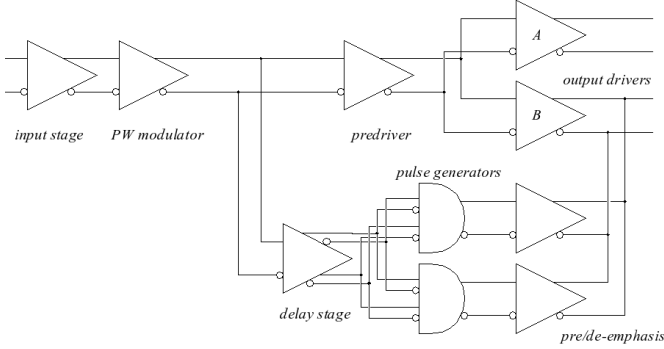

Figure 2: Modulator block diagram

All the stages have been designed as nMOS only differential pairs with resistive load in order to maximize speed. It has been shown [2] that, independently from the technology, the maximum speed can be obtained when the transistor current density is around 0.25 mA/µm. All switching transistors have been sized following this criteria.

A critical point is to be able to switch large current while keeping the parasitic capacitors, and therefore the transistor size, as small as possible. This implies that V_{GS}-V_{TH}. has to be maximized. Resistive load allows to pull V_G up to the power supply voltage, while triple well transistors with the source connected to the bulk have been used to get rid of the bulk effect on the threshold voltage.

The power supply is 1.5 V for all the stages with the exception of the two output and emphasis stages, which are powered at 2.5 V. This second power line is required in order to accommodate the voltage swing across the laser in all conditions of driving currents and laser differential impedance.

A. Pre-driver and output stages

The schematic of the pre-driver and of one of the two output stages is depicted in fig. 3. Here V_{DDmod} and $V_{DDlaser}$ are the 1.5 V core and the 2.5 V output power supplies, respectively.

The pre-driver is a differential stage with a resistive load. Inductive peaking has been used in order to increase the stage bandwidth. In order to limit the jitter the frequency dependence of the phase shift has to be minimized. It can be shown [3] that for best group delay the maximum obtainable bandwidth increase is 60%. The integrated inductors have been realized as two parallel spirals with octagonal shape. The inductors use the two uppermost metal layers for minimum

series resistance and an high resistivity substrate underneath (via a p-well implant block mask) to decrease the parasitic capacitance to the substrate.

The output stages are cascoded differential stages directly driven by the pre-driver. The two cascode transistors M_{2A} and M_{2B} in fig. 3 are thick oxide transistors. These transistors can withstand a voltage of 2.5 V and therefore can be safely connected to the higher power supply. The gate of these transistors is connected to 1.5 V, thus protecting the thin oxide transistors M_{1A}, M_{1B} and M_3 from the higher voltage.
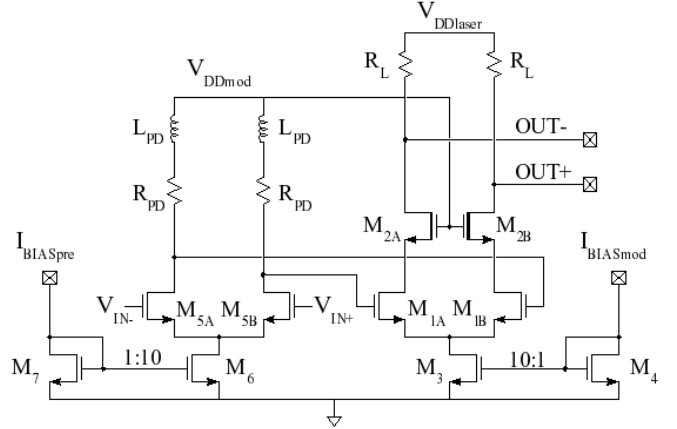

Figure 3: Schematic of the pre-driver and output stage

B. Pre/de emphasis circuit

The pre-emphasis principle consists of an increase of the signal amplitude for a very short time in correspondence of the signal transition, in order to increase the system bandwidth. It can be used when the RC limitation come from a component which cannot be improved (typically long wires that cannot be replaced). The de-emphasis works in the opposite way by decreasing the system bandwidth. Both cases are shown in fig. 4 for the rising edge.

An example of application to optical transmission where both techniques are required is when a laser is biased under its threshold. In that case the optical response can be characterized by a sharp rise followed by relaxation oscillations, while the falling edge is rather slow. Therefore it can be required both to speed up the falling edge (via pre-emphasis) and to slow down the rising one (via de-emphasis).
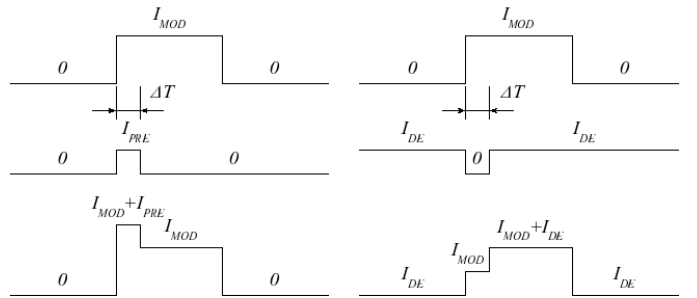

Figure 4: Pre-emphasis and de-emphasis

In order to obtain a pre-emphasis on the rising edge, a current pulse synchronized with the signal transition can be simply added to the output signal, as shown on the left part of

fig. 4. However, due to the fact that the driver can only sink current, the de-emphasis function cannot be implemented by subtracting a pulse. In the proposed architecture such a function has been implemented by adding a de-emphasis current in steady state and removing it during the emphasis pulse, as shown on the right part of fig. 4. Such a current has to be considered when the laser bias current is set. Pre-emphasis and de-emphasis on the falling edge use the same two techniques (just reversed).

The emphasis output driver, shown in fig. 5, is composed of two stages which are scaled versions of the main output stage, one for each signal transition. Each differential stage has two cascode transistors connecting the differential pair to the output either with direct on inverted polarity, on the base of the voltage on the cascode gate terminals. This voltage is controlled by one configuration register and allows to independently select pre-emphasis or de-emphasis for each of the two edges.
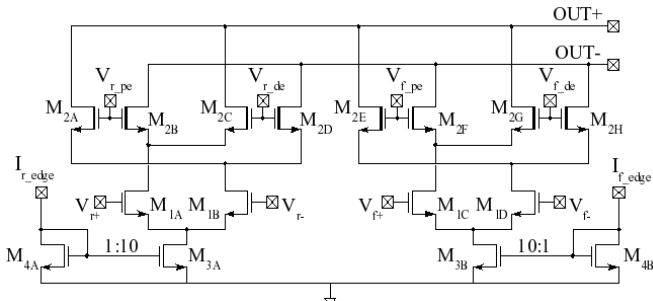

Figure 5: Emphasis driver

The two pulses used to drive the emphasis driver are generate by a differential AND gate [4]. A delayed copy of the signal is generated via a delay line. The original signal is then ANDed with the inverted delayed signal to obtain a pulse in correspondence to the rising edge. The falling edge pulse is obtained in a similar way with the inverted input signal and the direct delayed signal.

C. Bias current generator

The bias current generator stage resembles the output stage, where both sides of the differential pair are connected to VDD and the two outputs are shorted together. Again, triple well transistors with the bulk connected to the source are used to avoid the bulk effect and thick oxide transistors are used to protect the rest of the circuit from the 2.5 V supply.

D. Control logic

The GBLD configuration can be done via a I^2C slave interface. In the current version seven 8-bit register are used, to control the modulation, bias and emphasis current and to disable the non-used circuits in order to save power. Two mask registers are provided to protect the laser diode against erroneous settings excessive modulation and bias currents.

For correct driver operation, it is important that the contents of the configuration registers will not be upset by SEUs. To avoid malfunction, the I^2C controller uses Triple

Modular Redundancy (TMR) logic. However, since the I^2C interface operates with a gated clock (i.e. the clock is only active during the data transfers) TMR alone can not prevent corruption from the registers since errors can accumulate during inactivity periods thus eventually leading to data corruption. To avoid this problem, the scheme shown in fig.6 is proposed. It operates as follow : when no error is present or during a load cycle, the register behaves as a common triple voted register. However, when a corrupted bit is detected by the error correction circuit, a clock rising edge is generated loading the registers with the output of the majority voters. Once the register content is corrected the clock signal is cleared. The circuit is thus self-timed.
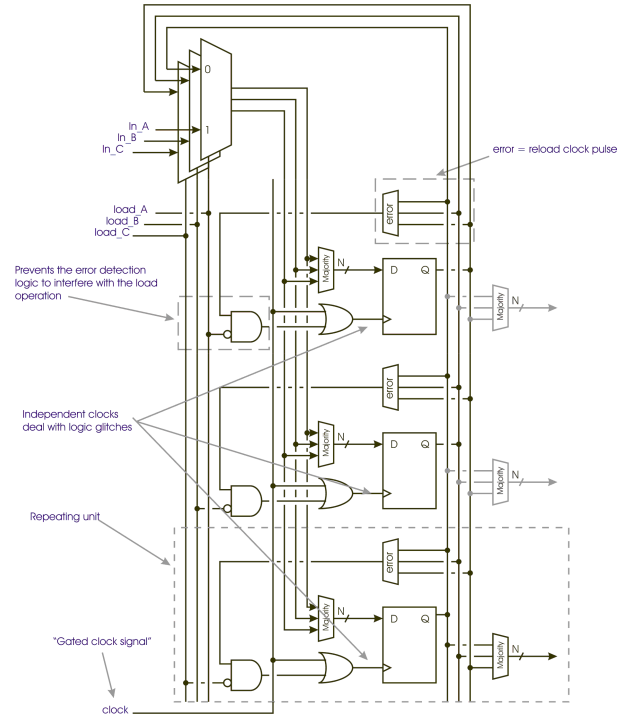

Figure 6: Majority voting of clock gated registers

E. DACs

Current mode steering DACs based on a matrix of current mirrors are used to generate the modulator and bias currents. The reference currents are generated from a 644 mV bandgap reference voltage.
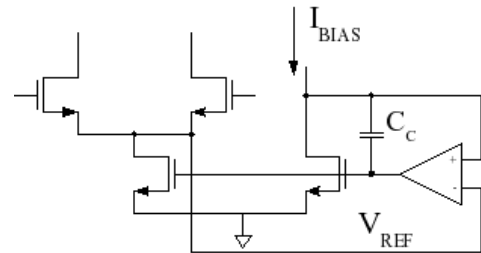

Figure 7: Bias scheme

Due to the large range of currents foreseen for the output, emphasis and laser bias stages, the V_{DS} of the tail current source of the corresponding differential pairs will vary

significantly. Therefore a simple diode-connected transistor cannot provide the required accuracy for these current sources. In the proposed solution an OTA compares the drain voltage of the tail current transistor with the drain voltage of the bias transistor in order to compensate for the channel length modulation effect. Fig. 7 shows the bias scheme.

IV. LAYOUT CONSIDERATIONS

The described GBLD prototype has been designed in a CMOS 0.13 μm technology and tested. The adopted technology features 8 metal layers, 2.5 V compatible thick oxide transistors and triple well nMOS transistors. The die size is 2×2 mm^2. Fig. 8 shows the chip layout.
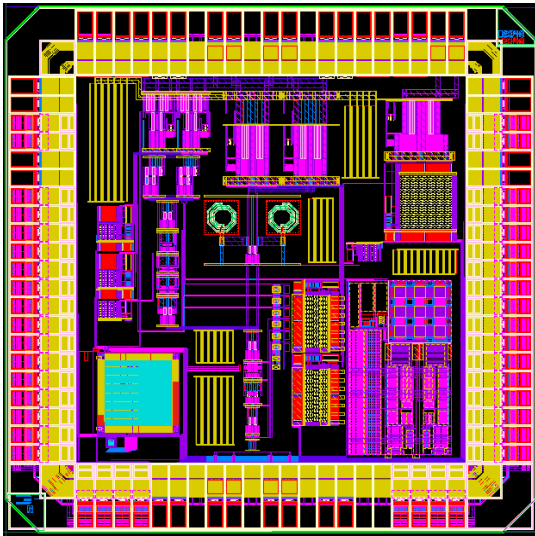
Figure 8: GBLD prototype layout

On chip decoupling capacitors have been used to prevent switching noise on the supply. A combination of MOS capacitors and vertical metal capacitors has been used in order to maximize the capacitance density. Approximately 630 pF of MOS capacitors and 50 pF of metal capacitors have been placed for each power supply.

V. TEST RESULTS

A first group of tests has been performed with only driver A bonded to the package output pin. Figures 9 and 10 shows the eye diagram at 2.4 Gb/s and 4.8 Gb/s, respectively.
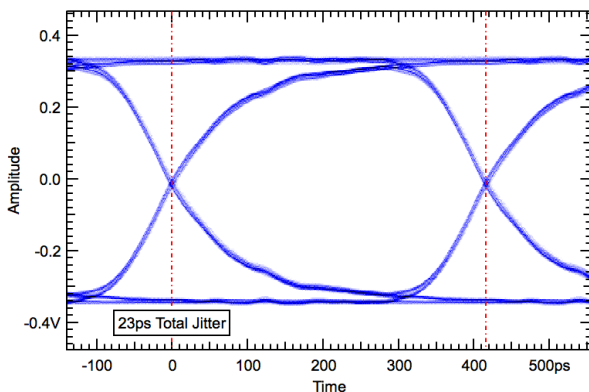
Figure 9: Eye diagram @ 2.4 Gb/s

It can be observed from fig. 9 that at 2.4 Gb/s the eye is open and the jitter is quite low. However, it can be already noted that the rise and fall times are not sufficiently fast for 5 Gb/s operation. Indeed, at that frequency (fig. 10) the eye is still open but a significant jitter is present.
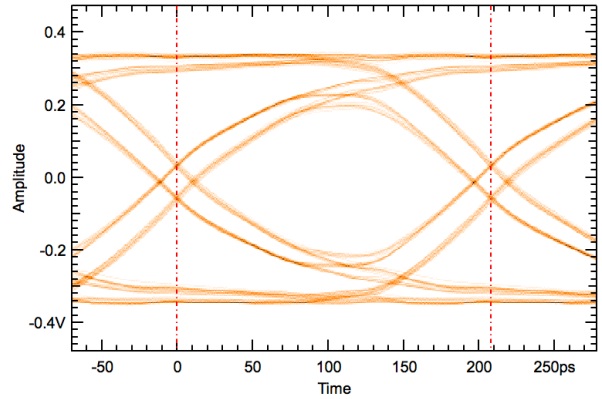
Figure 10: Eye diagram @ 4.8 Gb/s

Figures 11 and 12 shows the deterministic and random jitter, respectively. As expected, deterministic jitter is the dominant part while random jitter remains into the specifications. It can be concluded that the dominant jitter component is due to Inter-Symbolic Interference (ISI) related to the bandwidth limitation.
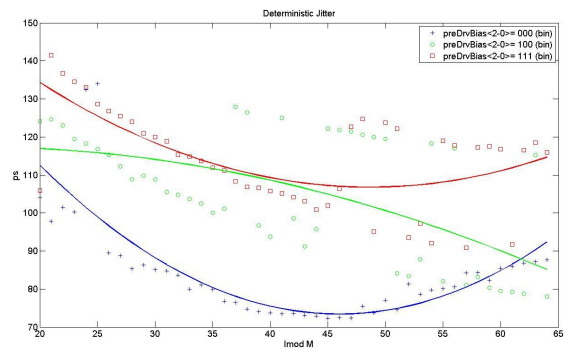
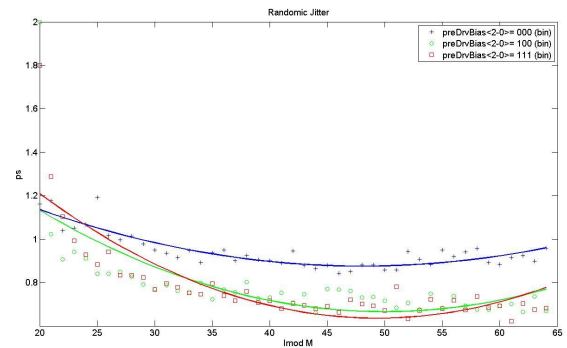Figure 11: Deterministic jitter vs modulation current

Figure 12: Random jitter vs modulation current

The three curves of fig. 11 and 12 correspond to three different values of bias current in the pre-driver stages. It can be observed an improvement in the jitter performances when the pre-driver is biased with a 40% higher current. Successive simulations with a complete layout parasitics extraction have

confirmed that the capacitive load of both the pre-driver and the output stages is much higher than expected and therefore limits the system bandwidth.

A second group of tests has been performed with both drivers bonded to the package output pads. The obtained results are summarized in fig. 13, where the three rows correspond to enable bits set for driver A, B and both A and B, respectively, while the three columns corresponds to different pre-emphasis values.
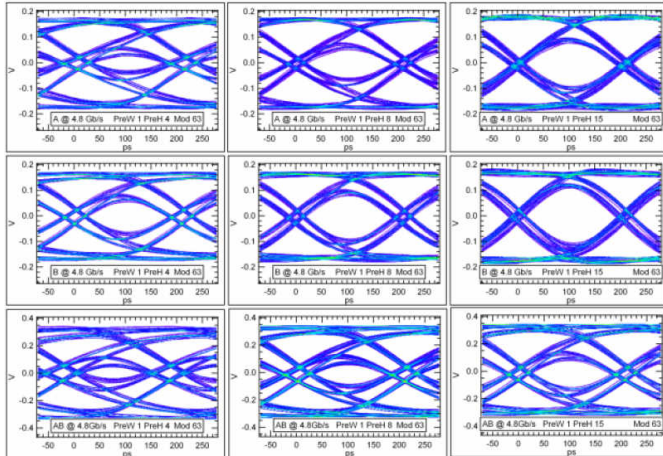

Figure 13: Eye diagrams @ 4.8 Gb/s

As expected, the higher capacitive load at the output, due to the presence of both drivers, significantly worsen the system bandwidth; however, the pre-emphasis technique allows to partially compensate the effect. The high jitter observed when both drivers are on can be attributed to asymmetries in the two drivers.

The best parameters setting has been used to connect the laser driver to a 850 nm VCSEL. The corresponding optical eye diagram is shown in fig. 14.
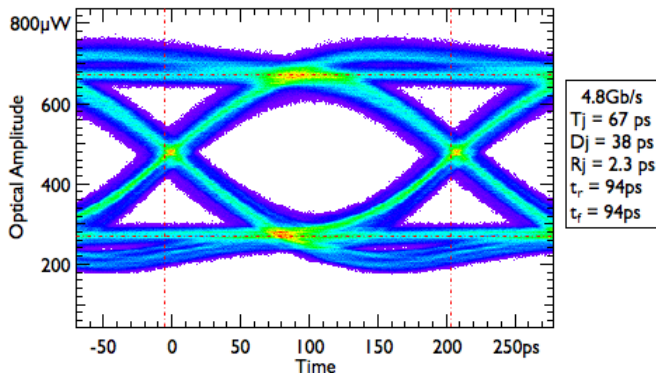

Figure 14: Optical eye diagram @ 4.8 Gb/s

The GBLD was also qualified against a commercial SFP+ transceiver. Fig. 15 compares the electrical eye obtained by the transceiver in loop-back configuration (top) with the eye obtained with the GBLD (bottom). It can be observed that a comparable eye was obtained in the two configurations, though more jitter can be observed when using the GBLD.

VI. CONCLUSIONS

A 5 Gb/s laser driver prototype in a commercial CMOS 0.13 μm technology has been designed and tested. The prototype is functional in all components but fall short of specifications in term of bandwidth.

Test results show that 5 Gb/s operation is possible only with the pre-emphasis function active. Even in this configuration, however, the jitter is relatively high even though it is fairly close to the specifications.

Accurate simulations on the full modulator layout with complete parasitic extraction showed that the bandwidth limitation is due to the parasitic capacitances introduced by the large lines required to drive the modulator current. An improved version will be submitted in the near future.
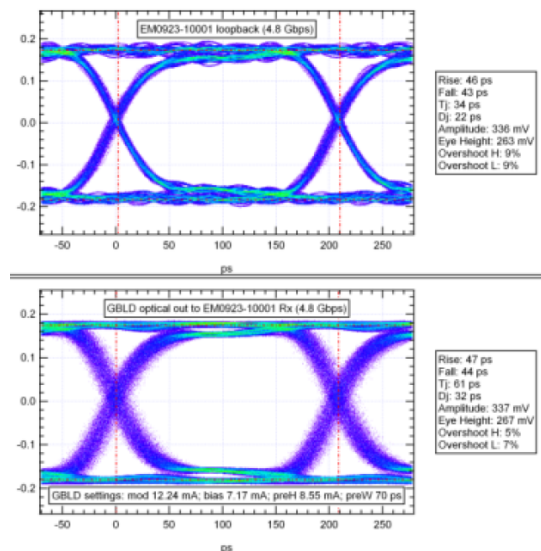

Figure 15: Optical eye patterns of commercial transmitter and GBLD @ 4.8 Gb/s

VII. REFERENCES

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