

Development of New Readout Electronics for the ATLAS LAr Calorimeter at the sLHC



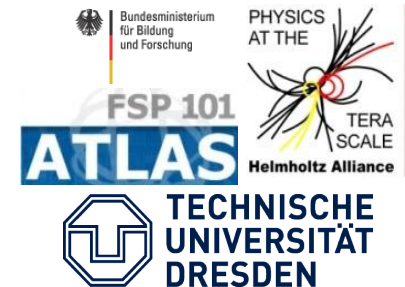
Arno Straessner – TU Dresden

on behalf of the ATLAS Liquid Argon Calorimeter Group

Topical Workshop on Electronics in Particle Physics

Paris

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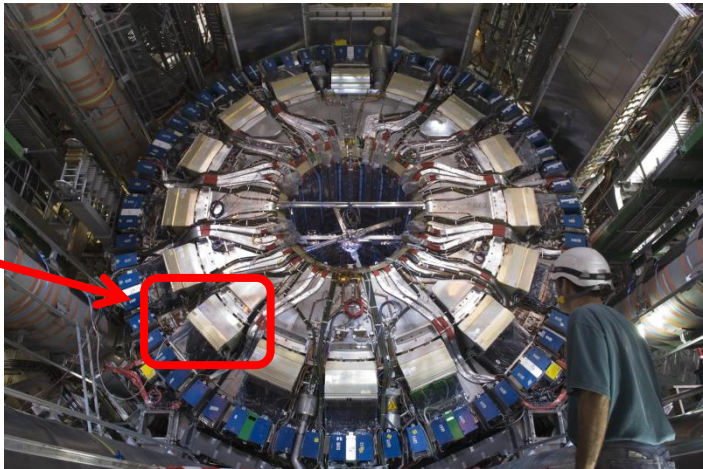
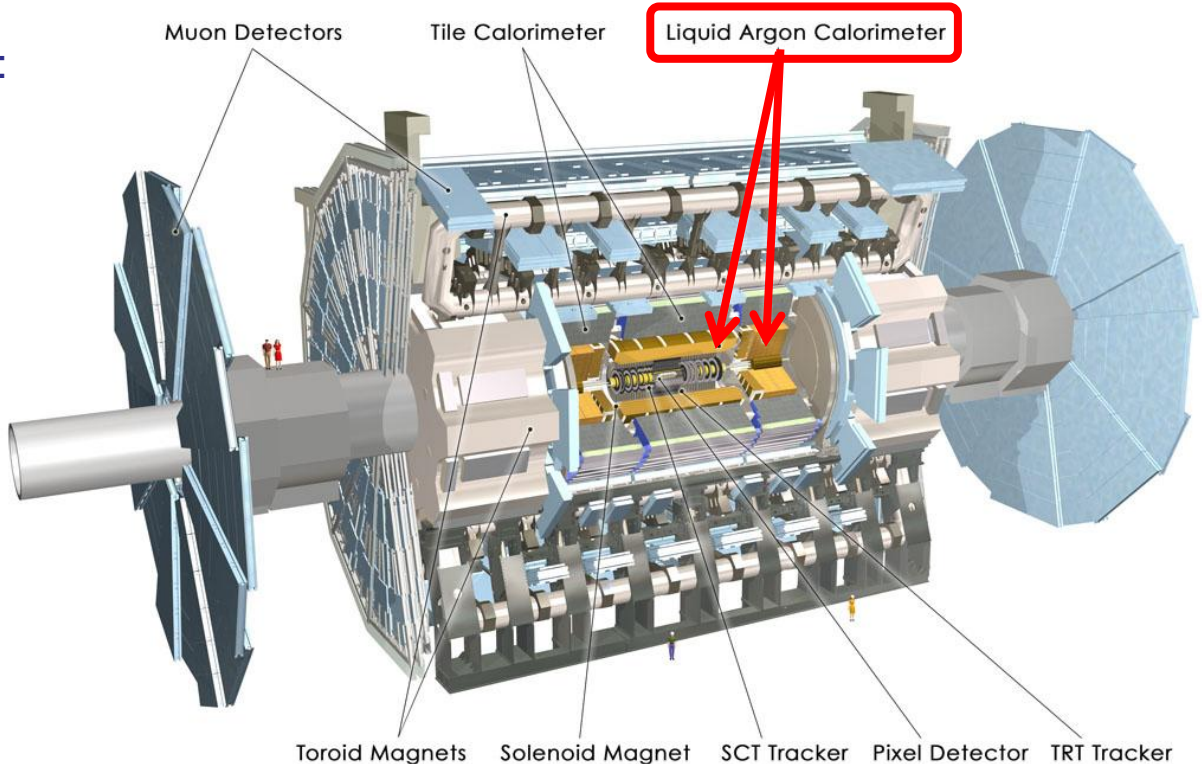
- The ATLAS Calorimeter Readout
- Upgrade Scenario and Readout Architecture for the sLHC
- Radiation Hard Front-end Electronics
- High Bandwidth Back-end Electronics
- Outlook

- 4 high granularity LAr calorimeters:
 - e.m. barrel Pb/LAr
 - e.m. endcap Pb/LAr
 - had. endcap Cu/LAr
 - forward calorimeter Cu/W/LAr



accordion structure

- 182486 readout channels
- 40 MHz proton-proton collision rate
- front-end and trigger-sum electronics
 - on-detector in radiation environment
- back-end electronics and more trigger logic
 - shielded counting room





- 1524 front-end boards (FEB)
 - up to 128 channels
 - preamp, pulse shaping, buffer and sampling
- in 58 front-end crates
 - low-voltage power supplies (LVPS)
- connected to off-detector electronics by 1600 optical links

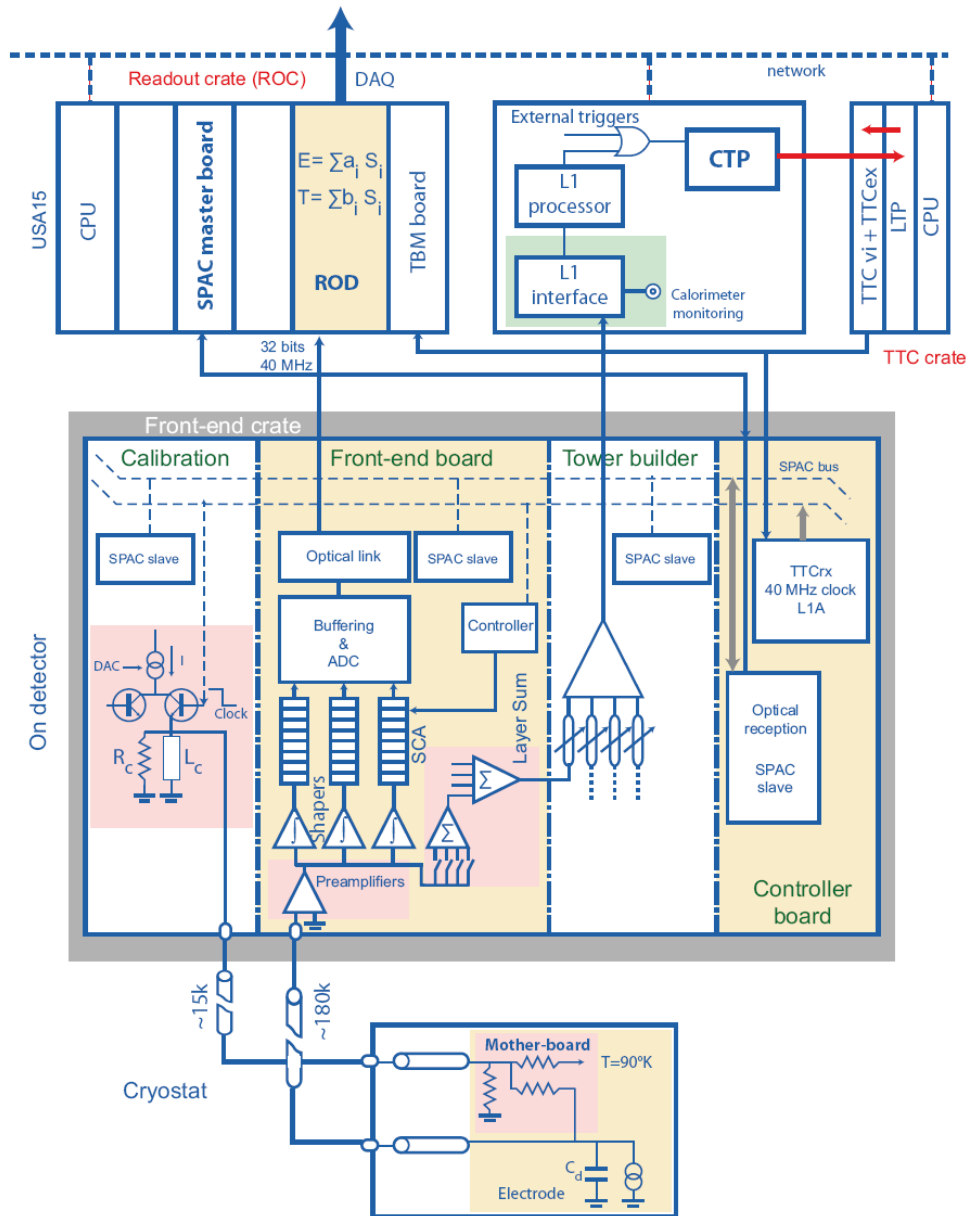


- 192 read-out driver boards (ROD)
 - digital filter

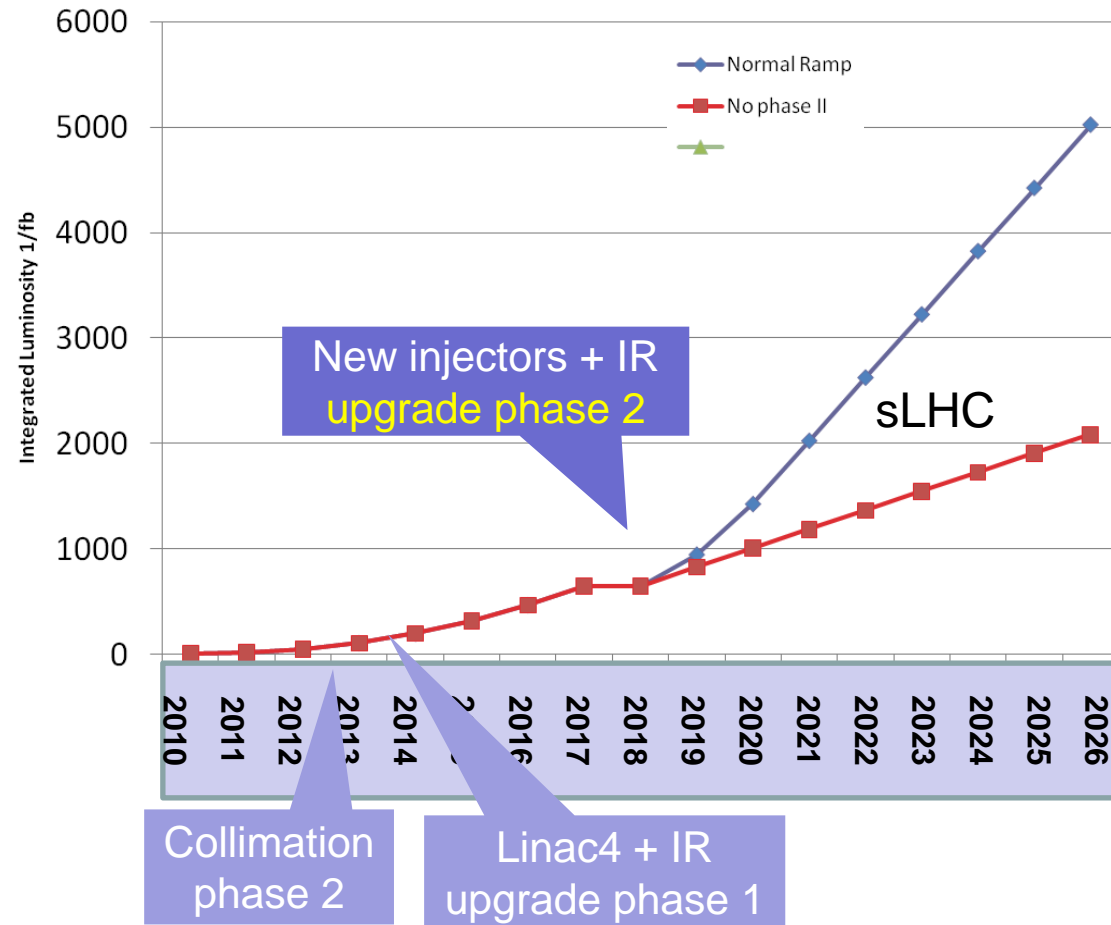
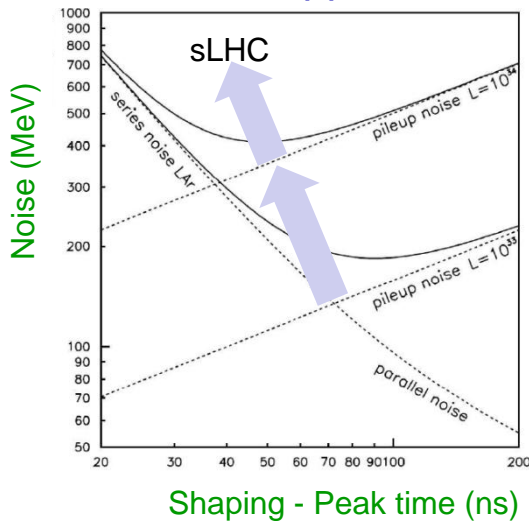


- 800 optical links to DAQ PCs

- 68 read-out system PC's (ROS)
 - DAQ and high-level trigger buffer

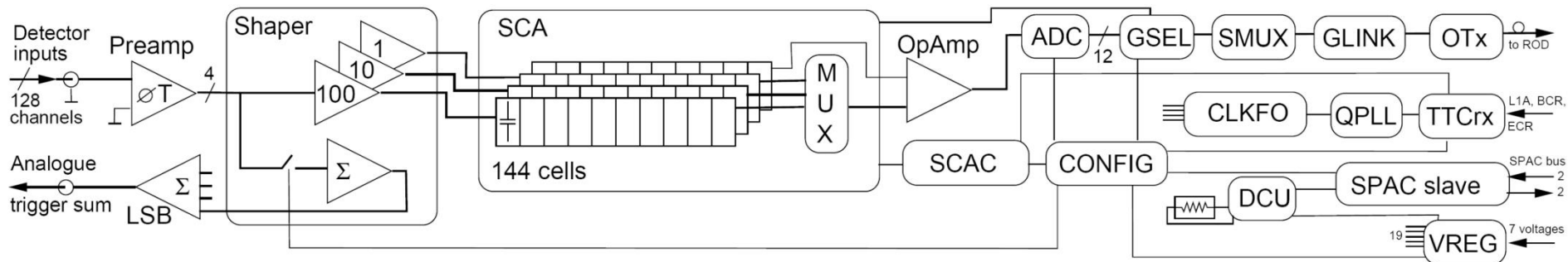


- LHC upgrade in 2 phases
 - sLHC starts in ~2019/20
- sLHC challenges
 - 10x more radiation
 - up to 20 times more pile-up events
- readout challenges
 - rad. hardness
 - same power consumption
 - same physics performance
 - same dynamic range
 - noise suppression



peak luminosity:
 $10^{34} \text{ cm}^{-2}\text{s}^{-1} \rightarrow 3 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1} \rightarrow 10 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$

- new calorimeter readout for 2019/20



- complex board architecture:
 - 11 ASICs with different technologies
 - some obsolete (DMILL, ...)
 - 19 voltage regulators
 - analog pipelines (SCA)
 - 80 W/board
 - water-cooled

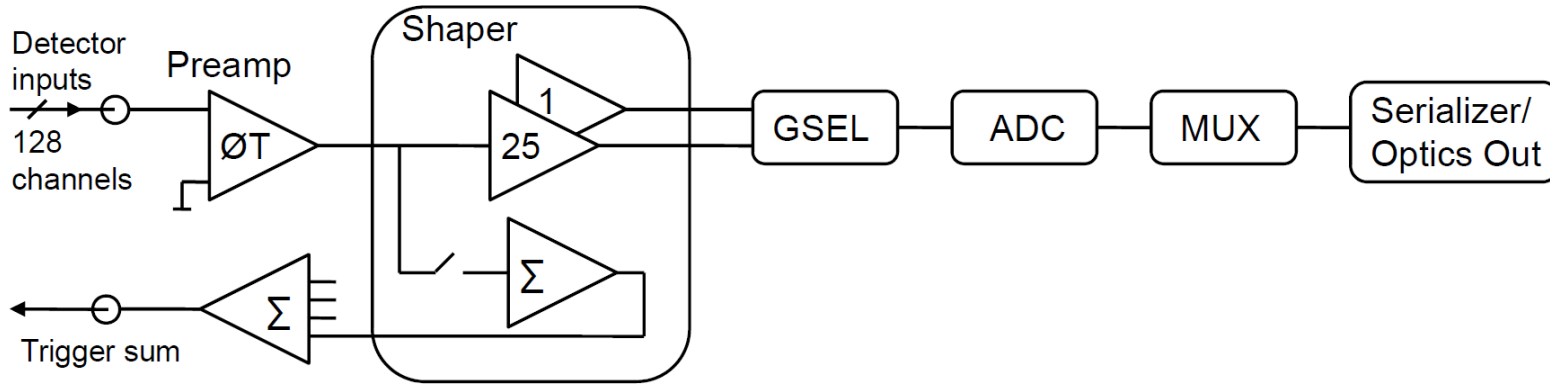
- performance limitations:
 - level-1 trigger rate only up to 100 kHz
 - max. latency 2.5 μ s
 - min. level-1 intervals 125 ns
 - fixed analog trigger sums (8-32 channels/trigger tower)

- main concern:
 - qualified for 10 years of normal LHC operation (incl. safety factors)
 - sLHC: 300 Krad and 10^{13} neq/cm²
 - small number of spares (6%)

LHC Radiation Tolerance Criteria

Radiation		Estimated	DMILL	Commercial Process
Type	Units	Level	RTC	RTC
TID	Gy	50	525	1700
NIEL	1 MeV equiv. n/cm ²	1.6×10^{12}	1.6×10^{13}	1.6×10^{13}
SEE	Hadrons (> 20 MeV)/cm ²	7.7×10^{11}	7.7×10^{12}	7.7×10^{12}

- replacement of single components impossible
- new front-end boards based on today's technology with same power budget



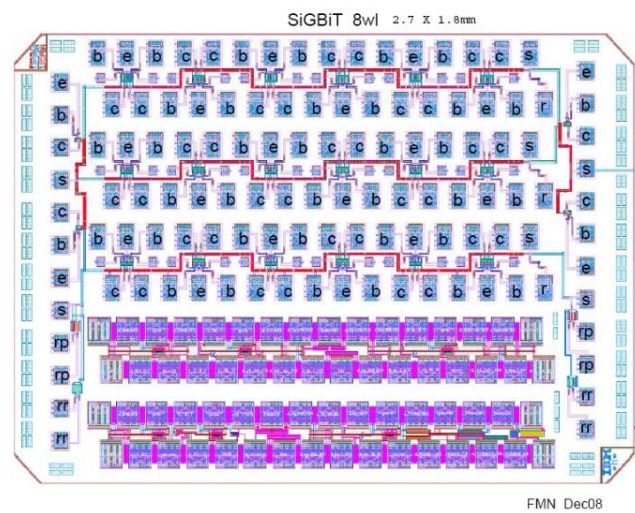
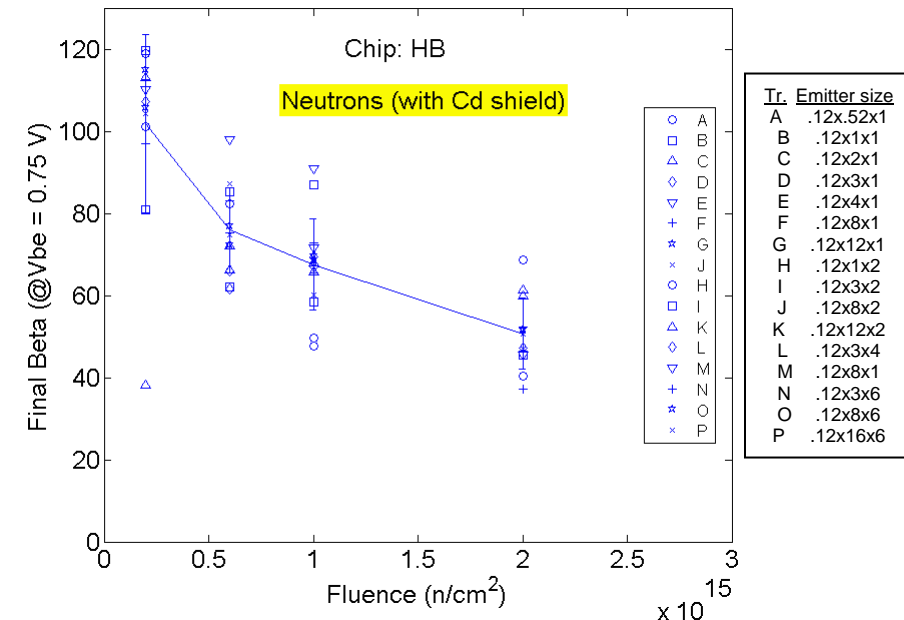
- evaluate different options:

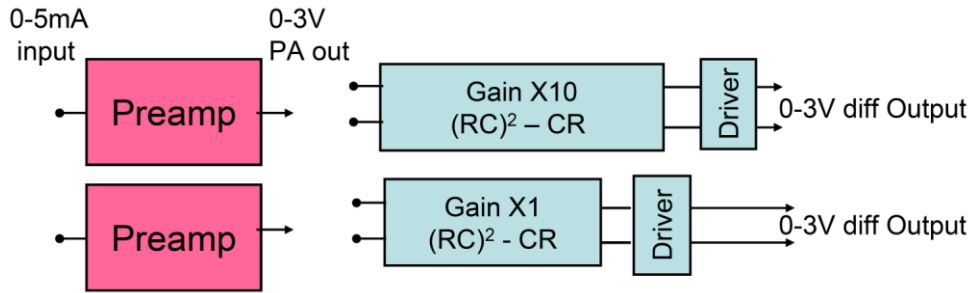
- shaper and gain settings
- analog ↔ digital pipeline
- on-detector ↔ off-detector pipeline
- analog ↔ digital gain selector
- analog trigger sums
→ possibility to keep current level-1 trigger system

- R&D baseline:

- shaping and digitization at high rate
→ 128 channels at 40 MHz
- transfer rate → 100 Gb/s per FEB
- rad. hard optical links at ~10 Gb/s
- fully digital off-detector trigger
→ digital pipeline on ROD
→ trigger sums on ROD and calorimeter trigger
→ more flexible and higher trigger granularity

- SiGe IBM 8WL BiCMOS process (0.13 micron)
 - technology also studied for ATLAS silicon strip tracker readout and ILC detectors
- irradiation tests with spare IBM test structures
- example: final gain after neutron irradiation:
 - $\beta > 50$ at 10^{14} neq/cm²
 - dispersion due to irregular test structure
- own chiplet submitted end of 2008
- irradiation program finished and data is being analysed

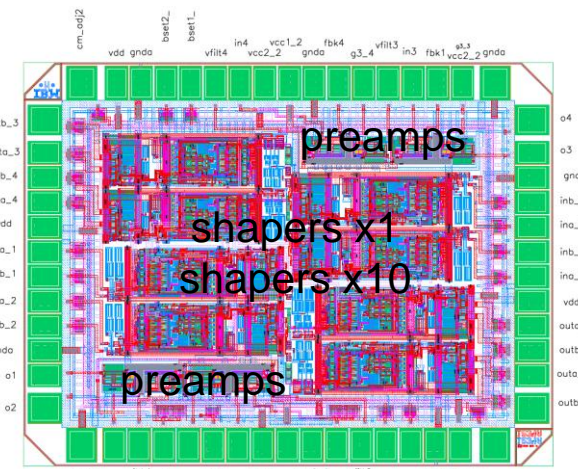
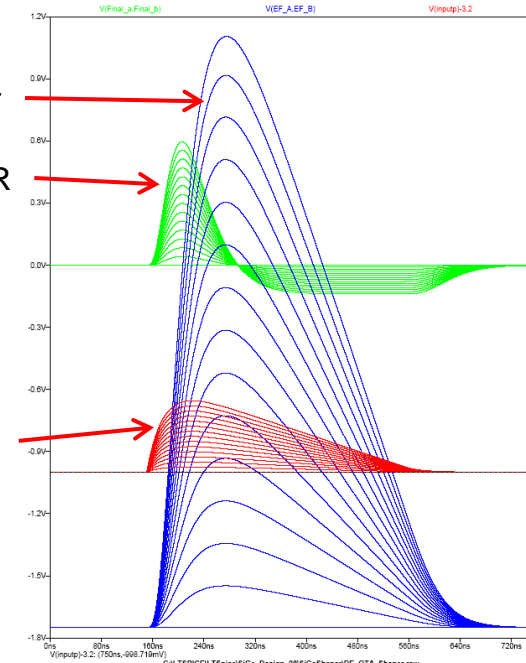




(RC)² 10X Shaper

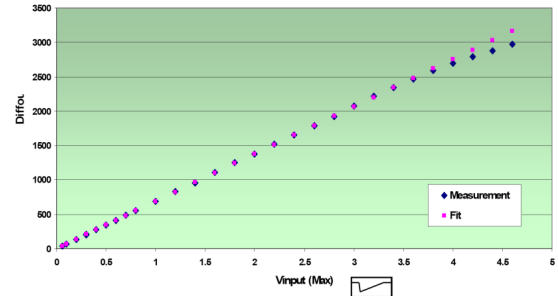
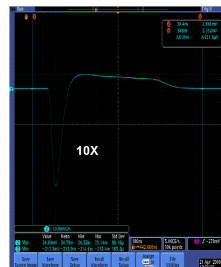
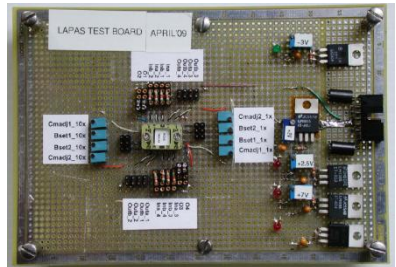
(RC)²-CR

Preamp out
0-700 μ A into preamp



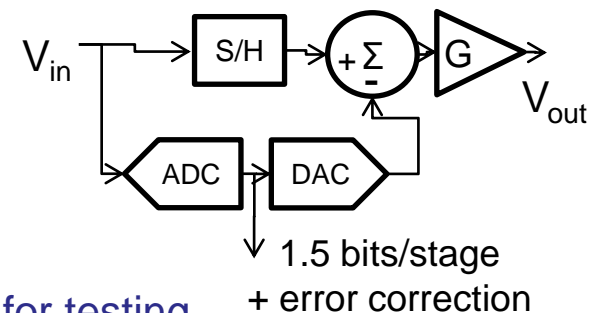
LAr Chiplet
2mm X 2mm

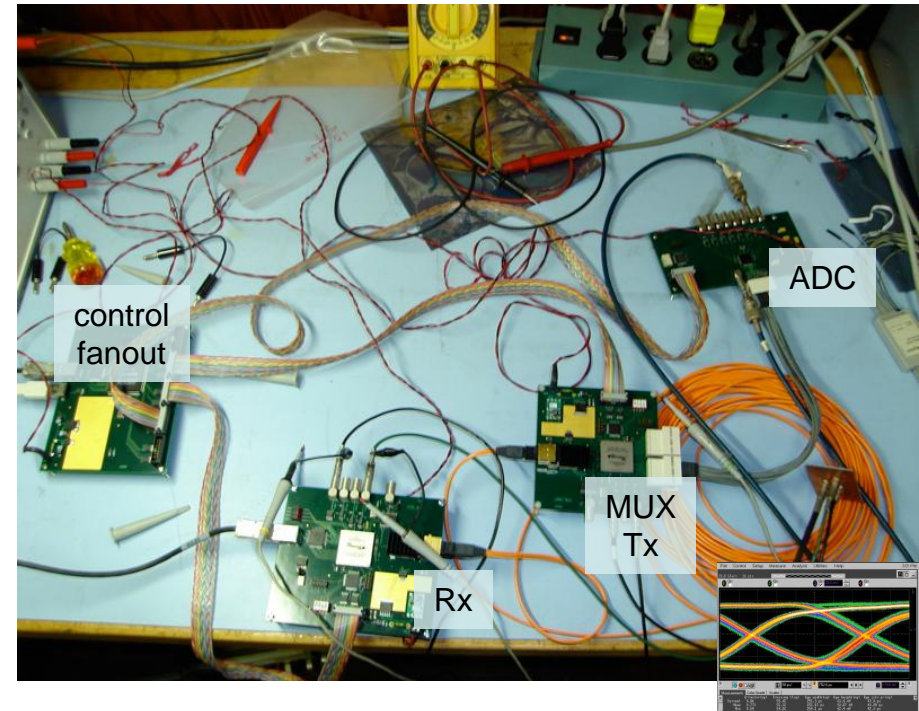
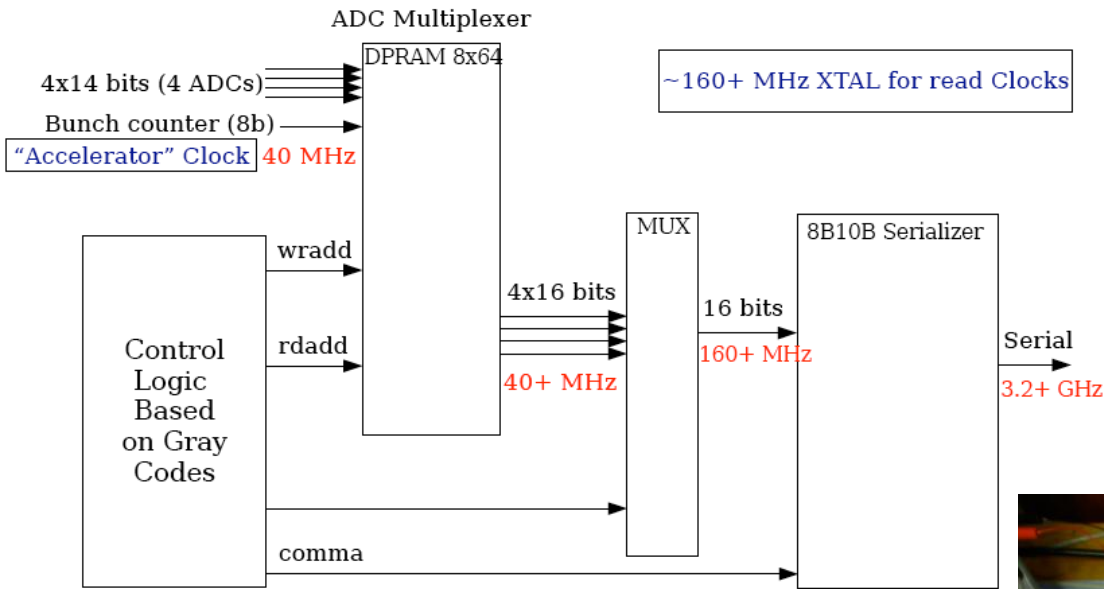
- Preamp
 - low noise $\sim 0.25\text{nV}/\sqrt{\text{Hz}}$, high dynamic range
 - based on low noise line-terminating preamplifier circuit topology presently used in ATLAS LAr calorimeter
- Shaper
 - fully differential
 - robust performance in low signal environment, excellent pickup rejection on and off chip
- < 0.2% non-linearity
- power $\sim 40\text{ mW}$ / preamp and $\sim 100\text{ mW}$ /shaper

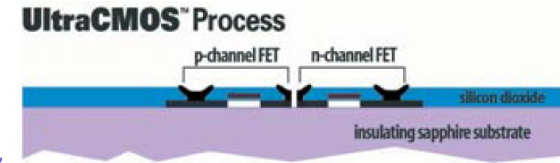


• see: Parallel session A2 – ASICs – Mitch Newcomer

- ADC is the most challenging component in the new “baseline” architecture
 - 15(16) bit dynamic range - 12 bit resolution – 40 MSPS
 - radiation tolerant and immune to single event effects (SEE)
- R&D strategies:
 - evaluate commercial parts
 - planning to test several COTS ADCs:
 - AD9259 (14/12 bit), ST-RHF1201 (12 bit), TI ADS5281 (12 bit)
 - development of a custom ADC
 - started with IBM 8HP SiGe → 8RF CMOS is now the candidate technology
 - shown to be radiation hard
 - lower cost compared to SiGe
- 12 bit pipeline ADC with 1.5 bits/stage and digital error correction
 - on-board correction will require rad-hard redundant memory for calibration constants
- main building blocks of custom pipeline ADC:
 - operational trans-impedance amplifier (OTA)
 - core for the S/H and Multiplying DAC subsystems
 - S/H capacitor important since noise $\sim \sqrt{kT/C}$
- chiplet submitted to CERN/MOSIS with OTA + cascade of 2 T/H for testing
- expected back by late October

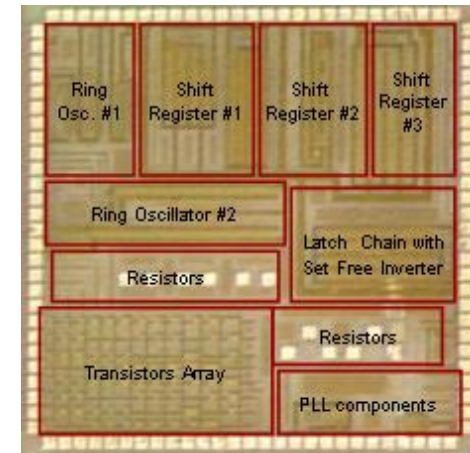
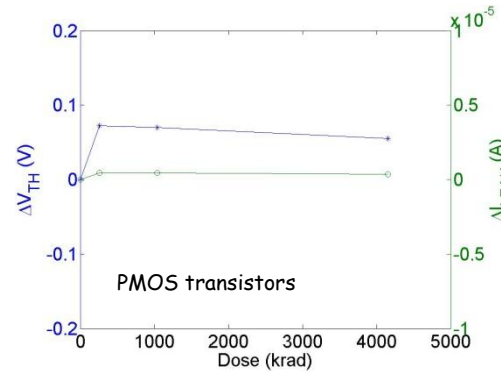
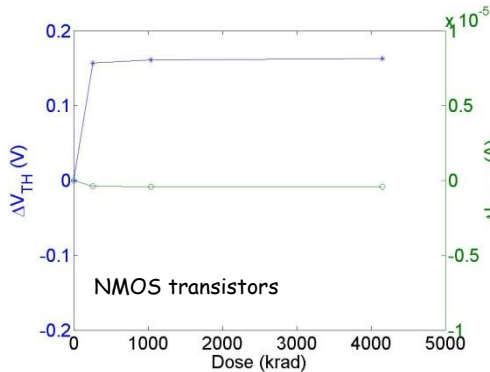






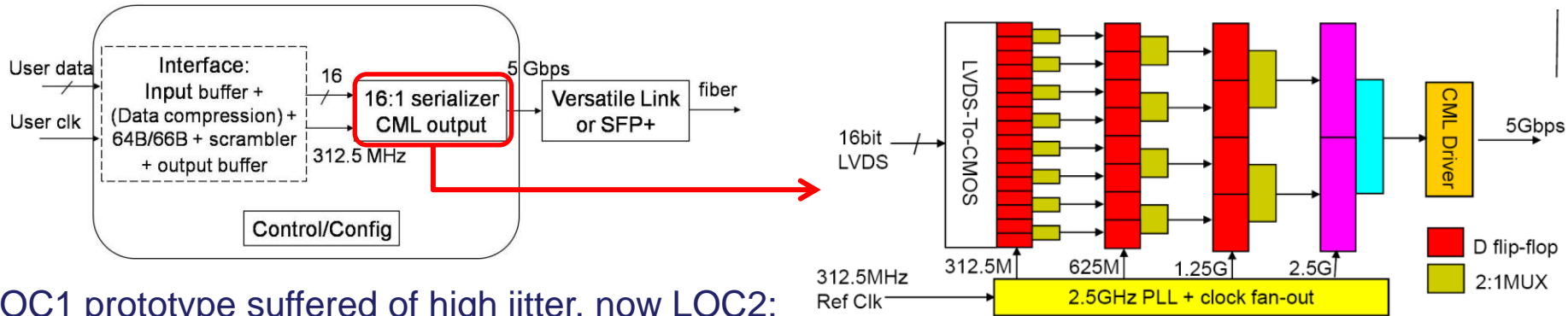
- Silicon-on-Sapphire (SoS) technology:
 - 0.25 μm UltraCMOS by Peregrine Semiconductors
 - low power, low cross talk \rightarrow good for mixed-signal ASIC designs
 - economical for small to medium scale ASIC development

- TID and SEE radiation tests performed in 2007:
 - gamma irradiation with ^{60}Co source up to 4 Mrad

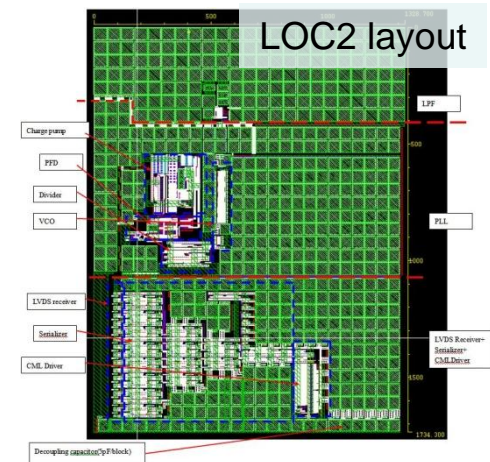


- with grounded substrate: small leakage currents (250 nA) and small threshold voltage increase
- irradiation in 230 MeV proton beam
 - no SEE observed in shift registers at a flux of 7.7×10^8 proton/cm²/sec
 - still correctly functioning after total fluences of 1.9×10^{15} p/cm² (106 Mrad(Si))

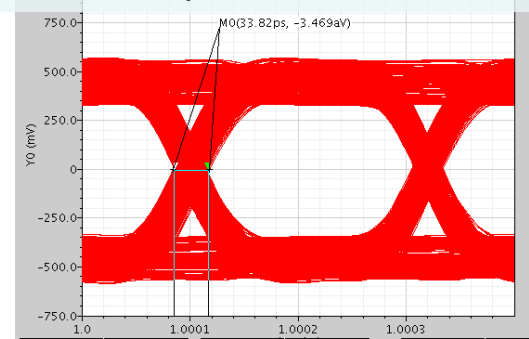
Link On Chip Prototype #2 (LOC2)



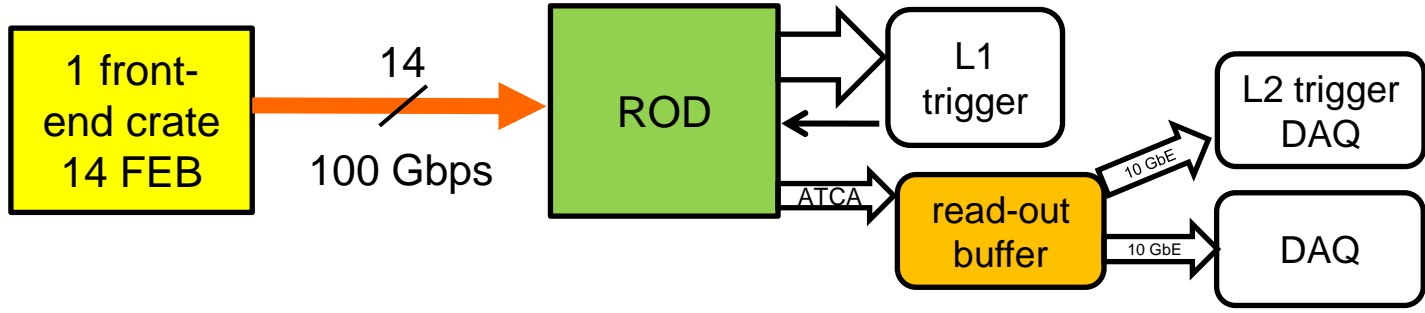
- LOC1 prototype suffered of high jitter, now LOC2:
- 5 Gbps 16:1 serializer
 - 3 stages of 2:1 MUX
 - last stage: 2 fast transmission gate D-flip-flops
- input data and ref. clock in LDVS
- output in CML at 5 Gbps → CERN Versatile Link
 - [Parallel Session B5 - Optoelectronics and Links: Paulo Moreira, Jan Troska](#)
- transmission bit error rate lower than 1×10^{-12}
- power consumption is below 500 mW or less than 100 mW/Gbps.
- post-layout simulation show that critical components meet LOC2 requirements (PLL, DFF, CML driver)
- user interface will be implemented in FPGA for tests
- effort towards a 5 GHz LC-tank based PLL:
 - random jitter < 1 ps (RMS) achieved in simulations
 - needed for ultimate goal of a ~10 Gbps link



with ideal power source: $T_J = 34$ ps



- 218 RODs in non rad-hard environment
- 1524 FEBs x 100 Gbps continuous data stream → 150 Tbps



- 12-fiber optical connectors  MPO/MTP style → each 100 Gbps

- Xilinx & Altera FPGA embedded SERDES
- evaluate reduction of number of links by
 - latency lossless data compression/decompression algorithm
 - less bits at ADC

} front-end challenges

- FPGA based Digital Signal Processing
 - advantage of parallel data processing
- system level architecture: AdvancedTCA
 - take the advantage of industrial standard
 - shelf management protocols, power management, fast fabrics
- perform level 1 trigger sum digitally
 - flexible and fine granularity

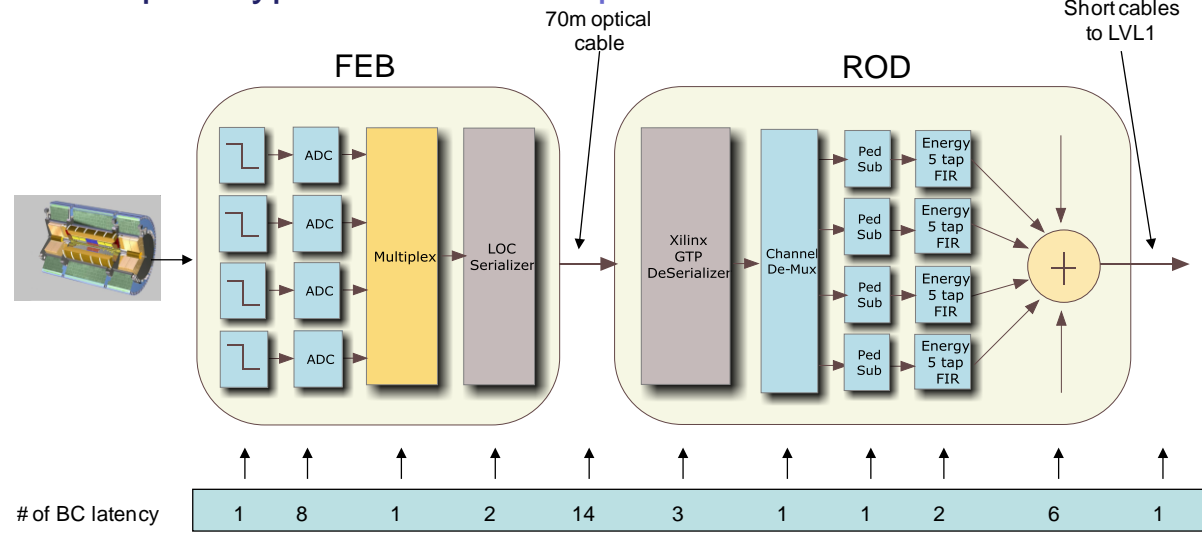
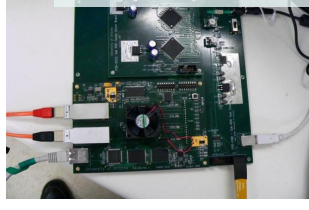


- ROD prototypes with Xilinx Virtex 5 FX (XC5VFX70T)
- 75Gbit/s fiber optic transceiver Reflex Photonics + SNAP 12
- ROD injector test with Altera Statix GX II
- 6.5 Gbps/fiber transfer rate possible
→ with previous prototype: stable 2.4 Gbps/f. on 12 fibers

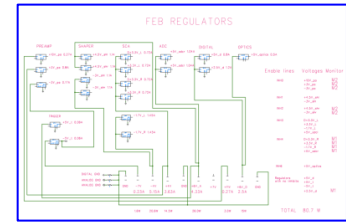
ATCA ROD prototype



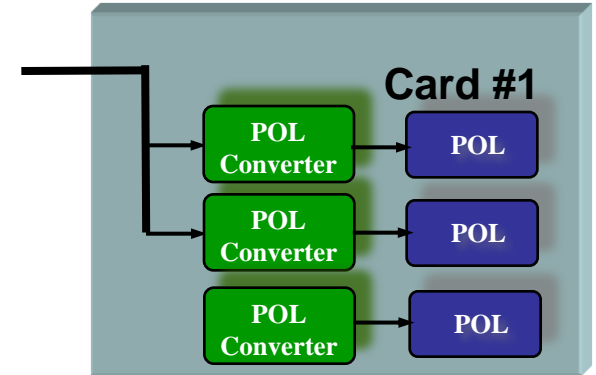
ROD injector



- digital linear FIR filter → FPGA embedded parallel DSPs (Xilinx Virtex 5 FX series, XC5VFX70T)
- digital level-1 trigger sums
 - pulse height and timing extracted from digitized pulse
 - time alignment to be evaluated → current ROD has only asynchronous data transfer
- total latency: 40 bunch-crossings → $\sim 1 \mu\text{s}$ < currently allowed $2.5 \mu\text{s}$
- more system level tests ongoing (level-1/2 digital buffers on ROD/ROB, remote DMA, ...)



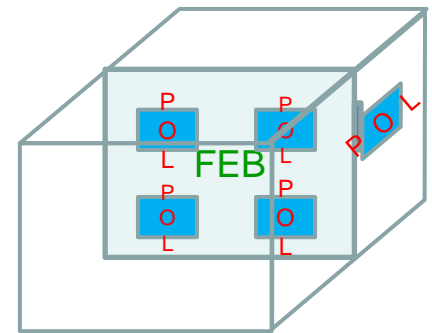
- current power supply scheme:
 - 380 VAC/3 phases → 280 V DC → DC-DC converter w/ 7 voltages → 19 voltage regulators on FEB
- power budget remains approximately the same
- rationalization of the number and levels of the voltages
- use of point of load (POL) regulators



- new LVPS architectures:
 - Distributed Power Architecture
 - main converter + POLs
 - Intermediate Bus Architecture
 - higher main voltage + 2nd bus voltages + POL converters

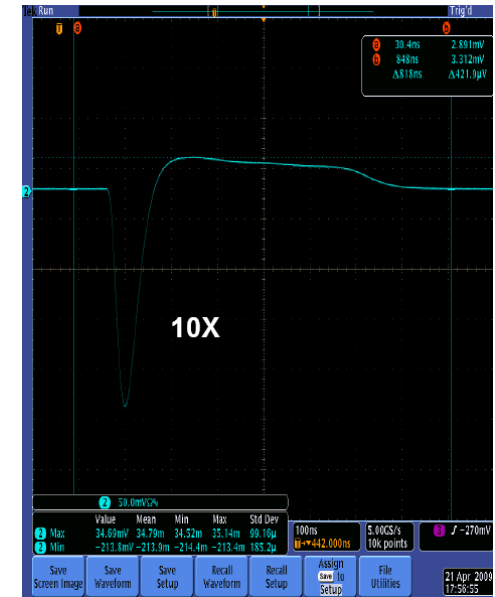
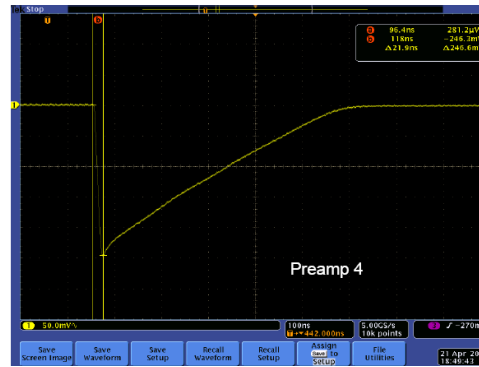
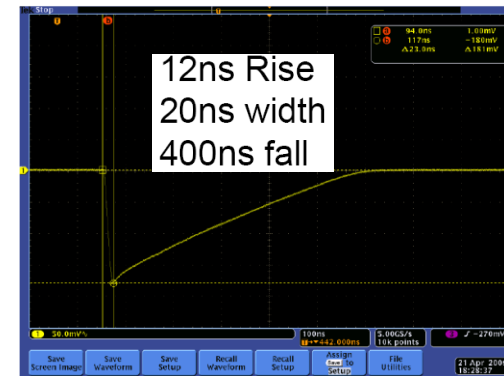
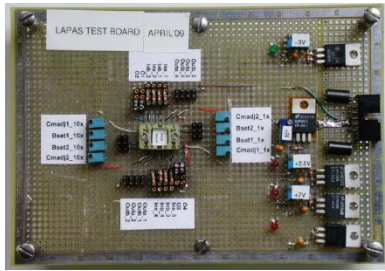


- 2 POL tested in different positions inside front-end crate (FEC):
 - LTM4602 – 6A High Efficiency DC/DC μ Module
 - IR3841 – Integrated 8A Synchronous Buck Regulator
- noise shielding necessary if inside FEC → ready for radiation tests



- Radiation levels and physics performance at sLHC requires replacement of front-end electronics of the ATLAS Liquid Argon calorimeter
- opportunity to apply modern technology and revise architecture:
 - trigger-less data transfer to off-detector electronics
 - fully digital trigger
- several major R&D challenges:
 - fast, rad-hard preamp, ADC and serial links
 - high bandwidth off-detector readout
- progress in all R&D activities
- more results expected soon, also on radiation and performance tests of recently submitted or received 8RF CMOS, SiGe and SoS chiplets

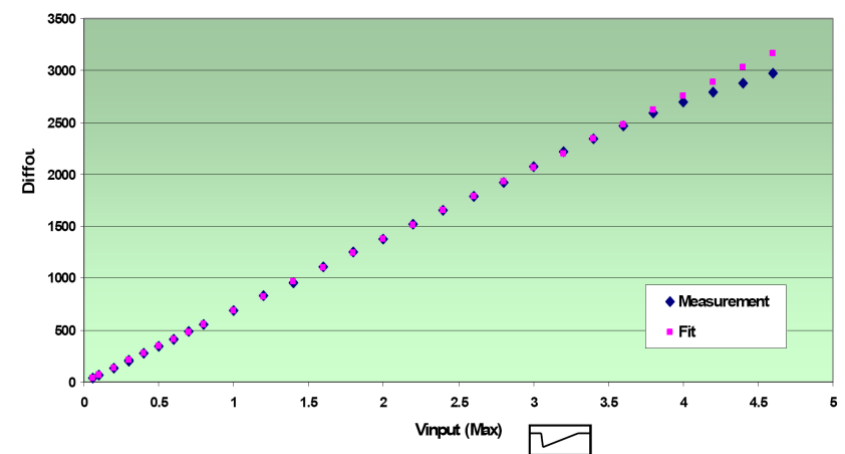
- Test board:



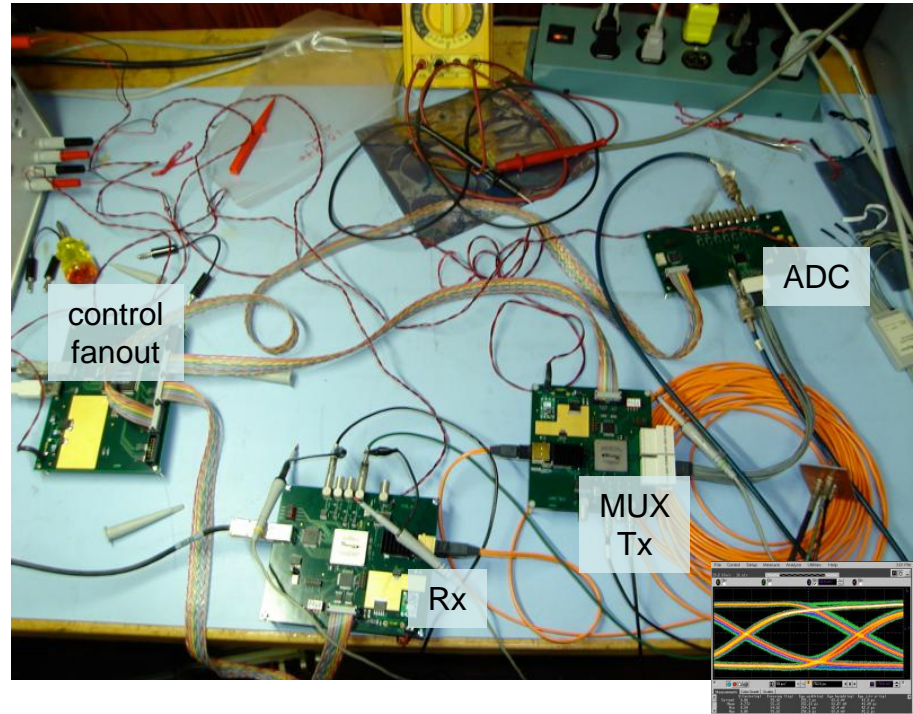
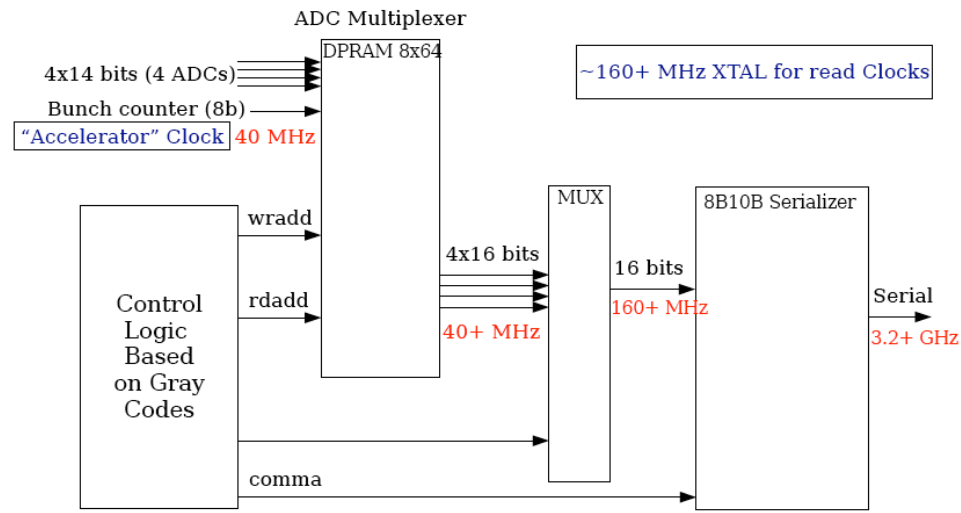
- Input
- preliminary linearity measurements:
- goal:
 - < 0.2% non-linearity
 - power ~ 40 mW / preamp
 - ~ 100 mW /shaper
- radiation testing and data analysis is ongoing

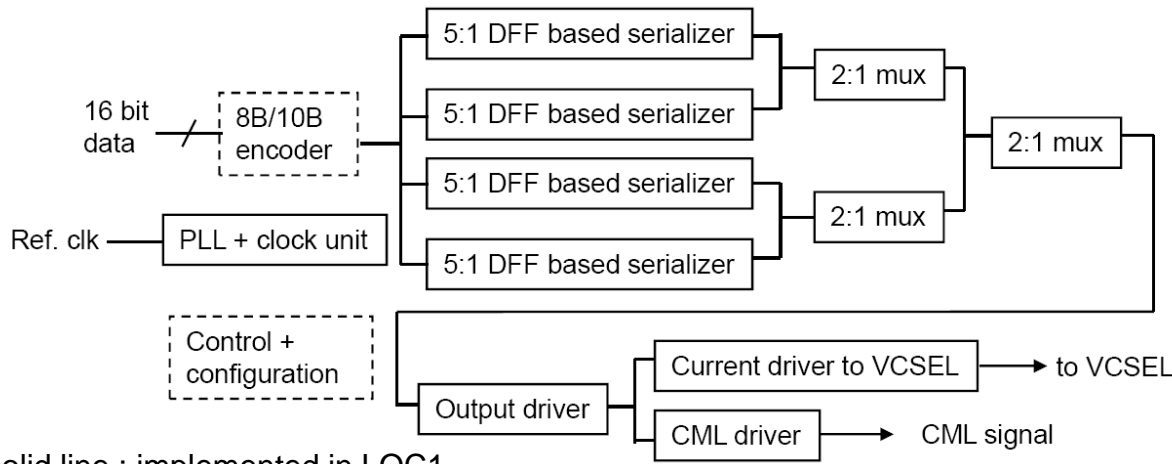
• Preamp

• Shaper

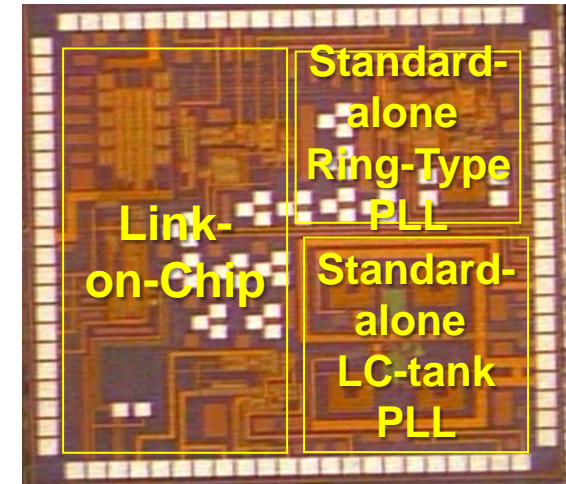


- 2 independent clocks
 - “TTC”-like clock for ADC and ADC multiplexer
 - crystal derived clock for high speed components (MUX, serializer)
 - provides much better jitter control
- Gray code control to manage multiplexer addresses
 - minimize effect of upsets
- data spends less than 8 bunch crossings in ADC multiplexer
 - minimize upsets
- triple redundant MUX
- 8B/10B encoding at level of the serializer
- full DAQ chain tested with commercial components and debugged successfully

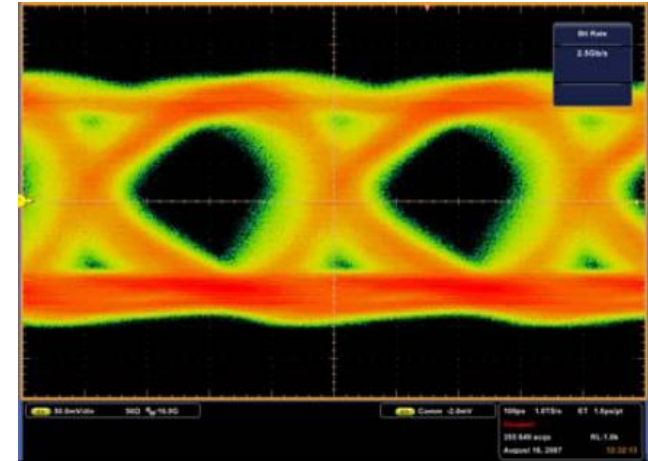




solid line : implemented in LOC1
dashed line: implemented in FPGA



- output rate at 2.5 Gb/s with 62.5 MHz reference clock
- power consumption ~200mW
- large jitter is observed and understood
 - deterministic jitter from 4-arm 2-stage MUX serializer
 - random jitter comes mostly from the PLL
 - will be corrected in the second prototype → LOC2
 - best BER reached $\sim 10^{-11}$
- SEE test with 200 MeV proton beam
 - error free for a fluence of 9×10^9 p/cm²
 - SEE cross section less than 10^{-10} cm² (p)
 - less than 1 error/link/h at sLHC
 - data analysis is ongoing and more tests are needed



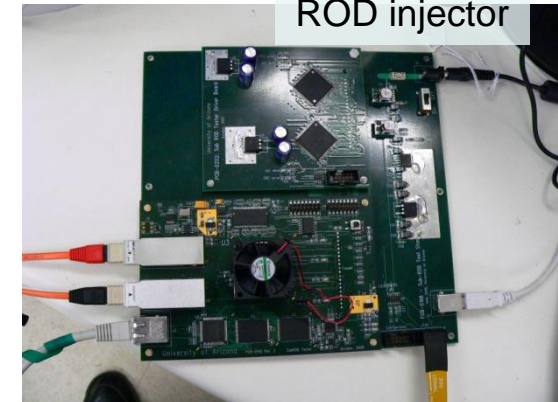
Eye diagram of a 2^7-1 pseudo random input data, UI = 400ps

- AdvanceTCA 8U Module
 - fabric interface to implement 1/10 Gbit Ethernet, RapidIO or PCI Express protocol
 - update channel to facilitate the communication between adjacent modules
 - rear transition module interface for off-crate communication
- Xilinx Virtex 5 FX series FPGA (XC5VFX70T)
 - 6.5 Gbps RocketIO GTX transceiver
 - PowerPC 440 microprocessor up to 550MHz operation
 - 550MHz DSP48E slices
- 75Gbit/s parallel fiber optic transceiver
 - Reflex Photonics 75Gbit/s SNAP 12 InterBOARD parallel fiber optic transmitter and receiver
 - channel data rate of up to 6.25Gbit/s
- expansion slot on board
- ROD injector
 - Altera Statix GX II FPGA is capable of running 6.375 Gbit/s (and more) → next version in AMC mezzanine format
- performance test with previous prototype version:
 - 2.4Gbps link running stably
 - fixed pattern data transmission of 36 channels (over 12 fibers)

ATCA ROD prototype



ROD injector



→ more tests soon
with ATCA-format ROD