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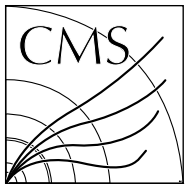

The Compact Muon Solenoid Experiment

CMS Note

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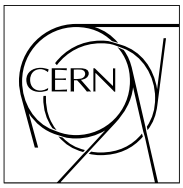

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Signals and Power Distribution in the CMS Inner Tracker

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Abstract

This Note describes how the interconnection between the 3540 modules of the CMS Inner Tracker has been approached, focusing on the signal, high voltage and low voltage line distribution. The construction and tests of roughly a thousand interconnects called "Mother Cables" is described.

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1 Introduction

This Note describes how the distribution of all the control signals together with the low and high voltage supply lines for a huge number of silicon detector modules located in a very tight geometry such as that of the CMS Inner Tracker [1] has been managed.
A compact solution was designed in Bari and a huge number of multi-layer and multi-geometry Kapton cables called "Mother Cables" (MC), described in the following, were fabricated in the same place.
In Sect. 2, an overview of the Inner Tracker geometry is given. In Sect. 3, the CMS Tracker readout and control system are very briefly described. In Sect. 4 an exhaustive description of the MCs, and in Sect. 5 of their topology, are given. In Sect. 6 the set-up to test the MCs after production and in Sect. 7 the testing procedures adopted to check their quality, are described.

2 TIB and TID structure

In the context of this note the sub-set of layers of the CMS Silicon Tracker called Tracker Inner Barrel (TIB) and the sub-set of the disks called Tracker Inner Disks (TID) are considered. A detailed description of the CMS Tracker layout can be found in [2].
The TIB consists of four cylindrical layers, each of which is made of four carbon fibre (CF) half-shells. On the inside and outside of the half-shell surfaces, the silicon modules are mounted in strings of three. These modules mount a sensor 320 μm thick and with strip pitch of 80 μm (layers 1 and 2) or 120 μm (layers 3 and 4). The TID is built with three carbon frame disks per beam direction, each disk is further partitioned in three concentric rings. Rings are populated with wedge shaped silicon modules which mount a sensor 320 μm thick and with strip pitch ranging from 81 to 158 μm.
On both TIB and TID structures, the modules are mounted with a staggered tile arrangement so that the areas occupied by electronics on the internal side are covered by silicon on the external side, and viceversa.
Furthermore the innermost TIB layers 1 and 2, are equipped with double-sided modules consisting of two single side modules glued together on their backs, one of which has the silicon sensor with the strips aligned to the Z axis (coincident with the beam line) of the experiment, while the other has its sensor tilted 100 mrad in either direction from the Z axis, thus providing two-dimensional localization of the hits. On the two smaller-radius rings of each TID disk double-sided modules are mounted on both the front and back sides. In Figures 1 and 2, a TIB shell and a TID ring are shown, respectively.

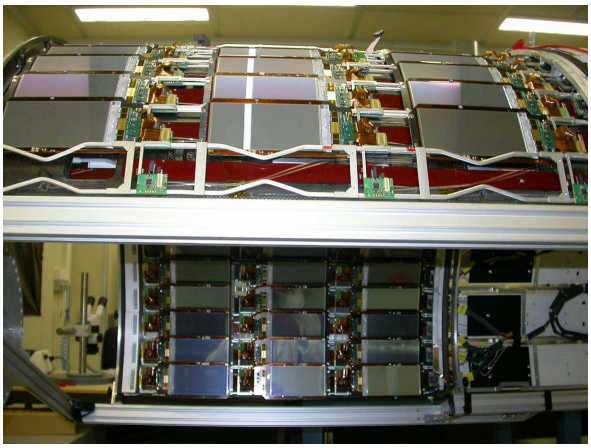

Figure 1: A TIB shell

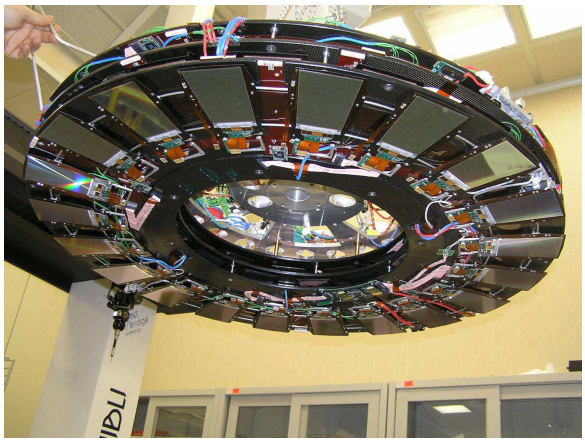

Figure 2: A TID ring

3 The CMS Tracker readout and control system

The CMS readout system was designed to amplify, to shape and to acquire the signals coming from the detectors, with a sampling frequency of 40 MHz, corresponding to the time interval between two consecutive bunch crossings of the LHC beams (25 ns). In Figure 3 a block diagram of the Tracker readout and control system is shown, where the frond-end module, the control module, the Frond End Controller (FEC) and the Frond End Driver (FED) are

represented.
The analog signals coming from the silicon detectors are elaborated by the readout hybrid containing the APV25 readout chips and constituting the frond-end of the detector. A detailed description of the APV25 can be found in

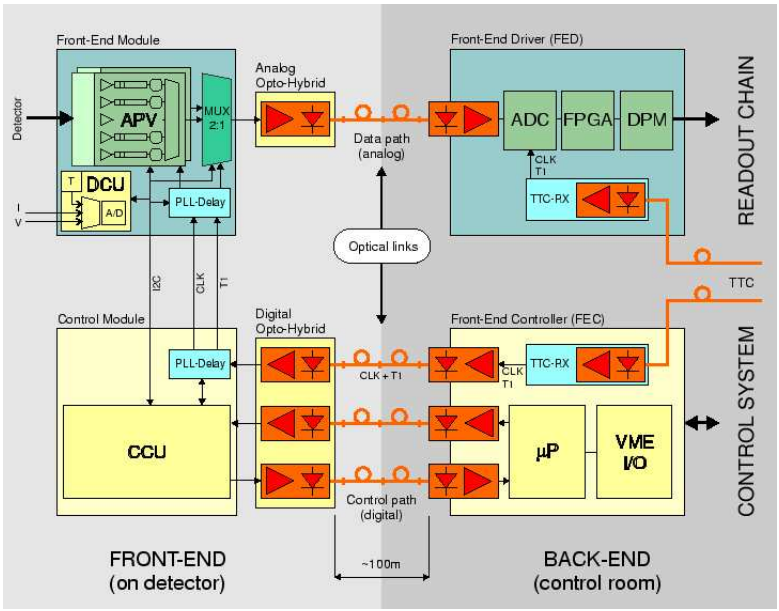

Figure 3: Block diagram of the Tracker readout and control system

[3].
The analog signals are sent through a Kapton cable 6 cm long with a characteristic impedance of 100 Ω, to the Analog Opto Hybrid (AOH) which converts them into light pulses. These pulses are then transmitted via optical fibres, to the control room, placed far away from the transmitter, under the supervision of a special control system.
Looking at the above mentioned diagram, it can be noted that the separation of the data readout channel from the one devoted to the control transmission of the clock (40 MHz) and trigger signals, needed for the operation of the front-end electronics, is implemented in a thoroughly at all levels.
Such signals are transmitted by a special electronic chain and in particular from the FEC, placed in the control room, which pilots the Control Module via signals transmitted on opto-fibres.
The opto-digital lines, based on laser transmitters, identical to those used for the analogical data, transmit the control data with a frequency of 40 MHz.
In the CMS Tracker, the modules have been grouped together electrically. The basic group consists of three modules which sit on any given cooling loop (see Figures 4 and 5 for TIB and TID, respecitvely) and are interconnected through Kapton multi-layer cables called “Mother Cables”, through which power, detector bias and controls are distributed, as will be described with greater details in the following sections, and are electrically joined in a more complex group called Control Ring, which distributes trigger, clock and slow control signals.
Control rings in the TIB/TID make use of a unit called the Digital Opto-Hybrid Module (DOHM) [4], which receives all the signals from the optical fibres coming from the FEC, converts them to electrical LVDS (Low Voltage Differential Signals) signals and distributes them to up to 45 detector modules (15 Mother Cables) via the Communication and Control Units (CCU)[5].
Given the high number of modules belonging to a control ring, TIB/TID has implemented redundancy in its DOHM hardware.

4 Mother Cable

The APV25, already mentioned in the previous section, needs certain slow control signals, namely “clock” and “trigger” (a special clock sequence), which are transmitted by the CCU-Module (CCUM) to the modules through the MC itself. The CCUM, on which the CCU device sits, is physically located on the top side of the MC. In Figure 6, a scheme of the distribution of the “clock” and “reset” lines on the MC to the modules is shown.
Also the Low Voltage (LV) and the High Voltage (HV) powers are supplied to the modules, and the signals coming from the CCUM to the DOHM are routed through the MC. The CCUM receives the signals from the FEC through

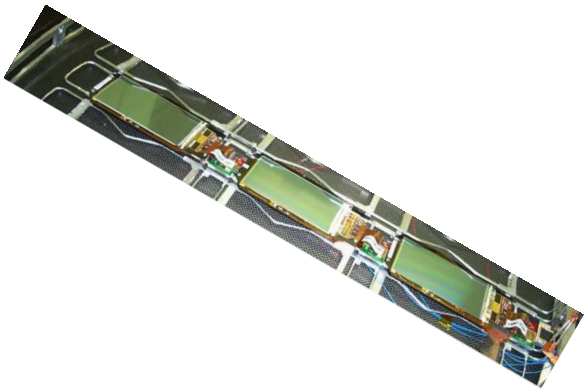

Figure 4: Three TIB modules mounted on a layer 3 shell. The Kapton Mother Cable runs underneath.

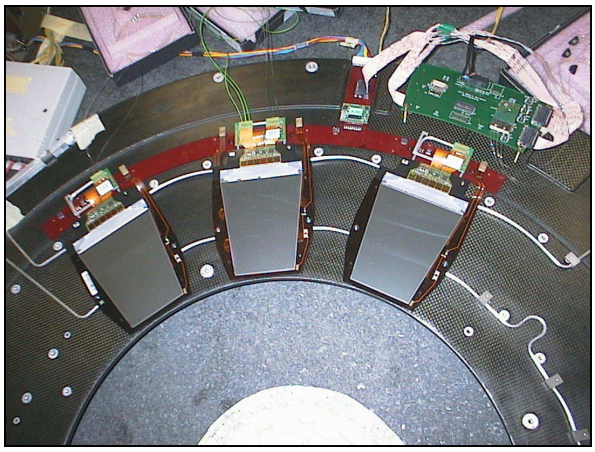

Figure 5: Three TID modules on a TID ring

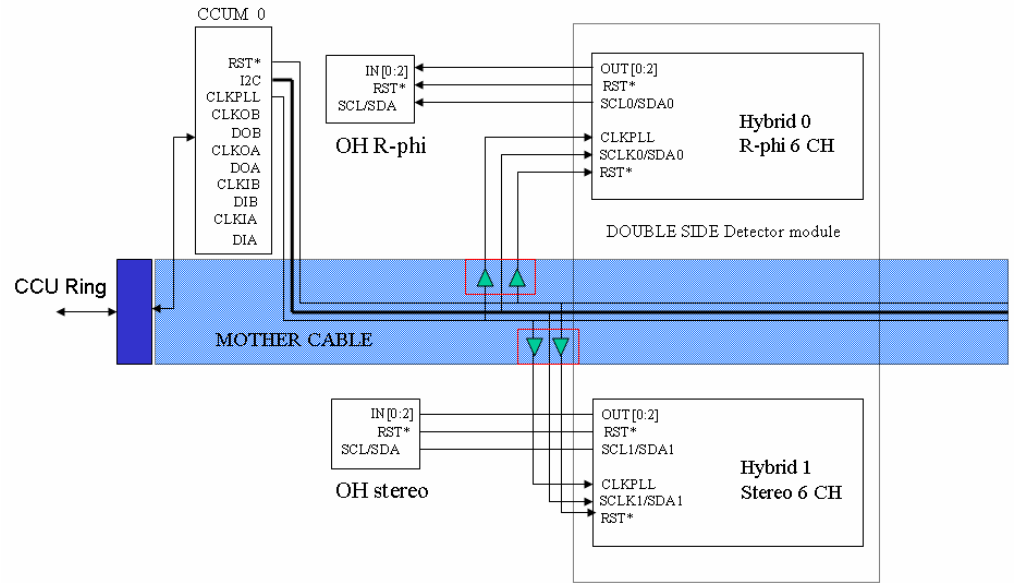

Figure 6: Clock and Reset lines distributed on Mother Cable to a double-sided module

the DOHM and distributes them to the various front-end modules. During this operation, potentially serious problems of impedance adaptation and signal reflection can occur. These phenomena influence the signal rise times producing a series of distortions, thus preventing a correct operation of the frond-end electronics.
For this reason, each signal was distributed in the cable as a single transmission line terminated at the other end of the cable itself, and then sourced to every front-end hybrid via a custom integrated circuit with high impedance input, mounted on the cable.
For what concerns the powering of the Tracker modules via the MC, since they sink a relatively high current (1-2 Amps), it is mandatory that the resistance of the various sections of the cable is small enough to avoid the associated voltage drop causing the front-end operating voltage to be lower than the minimum admissible one.
This drawback has been avoided by making the cable with a thicker copper section, but not too thick, as this would imply adding more material budget in the Tracker, thus degrading its performances.
Finally these cables drive slow control signals with I^2C standard. For this purpose, on the MC there is an I^2C bus for each single connected module. This choice is due to the limit on the maximum number of devices that can be connected to the bus (15 at most) but also allows to avoid operational problems. Indeed if more devices are connected in a single bus and one of them jams for any reason setting one of the two lines on “Low” state, the master cannot communicate with any of the connected devices anymore.

The CCUM can pilot fifteen buses in total. In the TIB/TID structures equipped with double-sided modules, six of them go to the modules through the MC, while one reaches the interconnection-card (DOHM). These buses are slow and the devices connected to them are “open-collector” so they need a “pull-up” resistance to be operational. In total on the MC there are twelve lines that go out of the CCU and reach the six modules and three “reset” lines, one for each pair constituting a double-sided module. In the TIB/TID structures equipped with single side modules, on the MC six lines connect the CCUM to the modules, and three “reset” lines reach one module each. The “reset” signal is not directly sent to every silicon module, but through a section of the same chip used to buffer the 40 MHz clock; this solution increases the safety margin of the system in case of a breakdown of one of the modules.
The MC, realized in multi-layered Kapton (copper layers and polyammide glued and pressed), is a system compatible with the normal industrial production of multi-layer circuits. Kapton is chosen because this material features: better flexibility in comparison to other materials, low emission of harmful gas in case of fire, stability with aging and, moreover, because it can be packaged in an isolated structure.
The structure of the cable is shown in Figure 7. Here three sections can be seen that connect three single side

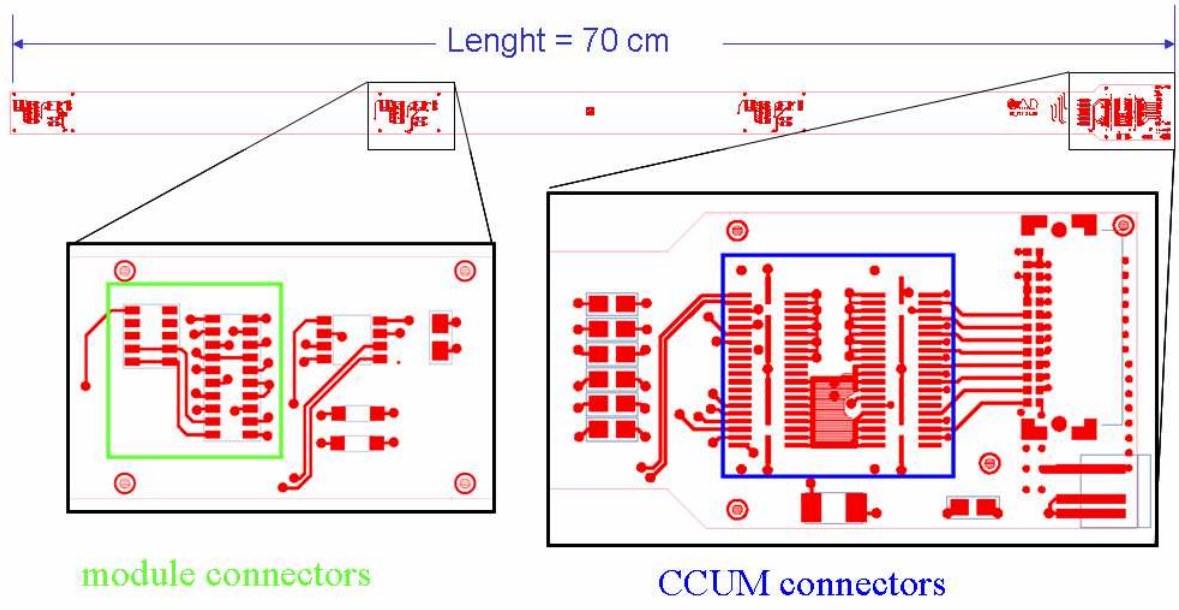

Figure 7: Mother Cable layout

modules and one section, on the extreme right of the cable, where the CCUM is located, close to the connector of the interconnection card.
The MCs used for the double-sided modules are almost the same, but obviously with more connectors on the three

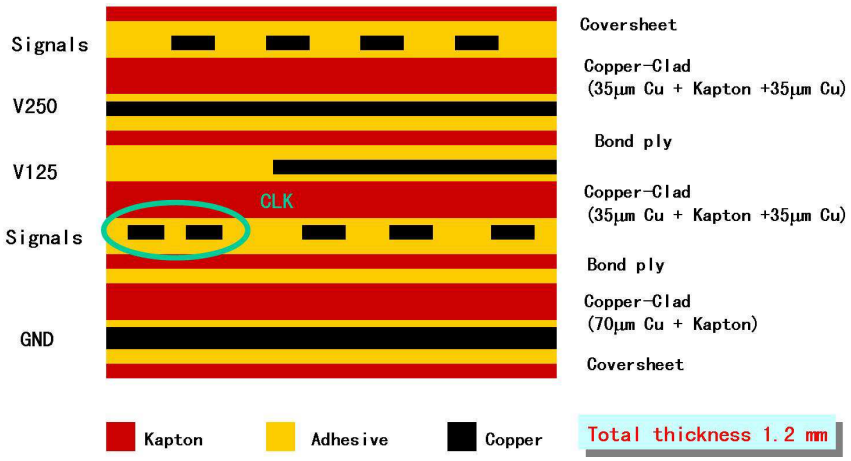

Figure 8: Mother Cable stack-up

sections.
In Figure 8, the stack-up of the cable is shown. It is possible to distinguish a top signal copper layer with its Kapton "coversheet" to protect the signal lines, leaving uncovered the pads for the components soldering. Then there is a first inner copper layer, 35 μm thick, where the power voltage of 2.5 V is distributed. In a second inner copper layer the power voltage of 1.25 V is distributed. Then a third internal layer is used to route the signals and a bottom layer is devoted to give the reference ground (GND).
In Figure 8, it is possible to note that the copper side of the V125 layer does not cover the entire surface so that the "clock" differential line is referenced to the V250 and GND planes. This feature allows to use strips with larger width that indeed otherwise would have to be narrower than the minimum feasible.
The final thickness of the MC is 1.2 mm and its final shape was designed in order to be compatible with the mechanics of the Inner Tracker. The amount of the copper budget was evaluated after an electric simulation based on

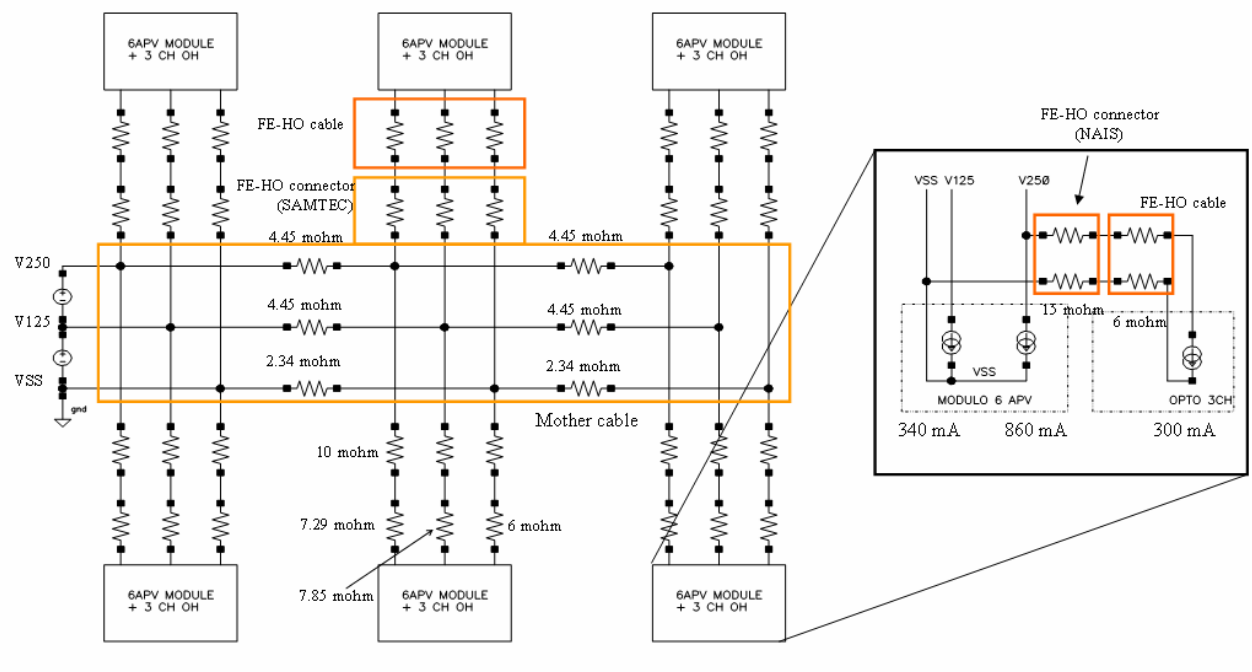

Figure 9: Mother Cable DC model

the equivalent DC model shown in Figure 9.
This model is related to the system composed by double-sided modules connected on a MC. The best resistor values were evaluated tuning the thickness and width of the copper traces on the MC, in order to keep within their prescribed limits the working parameters of the electronic components. The power consumption, the connectors resistance and the Front-end hybrid flexible connection resistance and the geometrical parameters were the known data during the simulation.
The MC has been fabricated using seven copper clad Kapton layers, pressed together during a thermal cycle including a pre-heating step of each layer to remove the moisture absorbed during the chemical etching. In fact, the non perfect dryness of the layers sometimes caused their ungluing during the reflow soldering. Moreover the dimensions of the MC were too large to allow intervention with an automatic tool during the dispensing of the soldering paste and the positioning of the discrete elements on the cable, thus needing manual handling. The position of the MCs for the double-sided modules is shown in Figure 10. Both the front-end hybrids and the biasing circuits (Isol Top and Isol Bottom) are connected to the MC.

5 Mother Cable typologies for the CMS Inner Tracker

Concerning the mechanical constraints to which the MC production was subject, it must be noticed that on each Tracker layer the Z position of the module is different due to the tracking overlapping requirement. In the same layer the Z+ modules are in a different position compared to the Z- modules so there are 8 half layers with modules inside and outside the mechanical structure generating a total of 16 different mechanical configurations. This requires 16 types of MC geometries with different length, shape and positions of the discrete components on them, among which two examples are shown in Fig. 11. In Table 1, the multiplicity, the main geometrical parameters

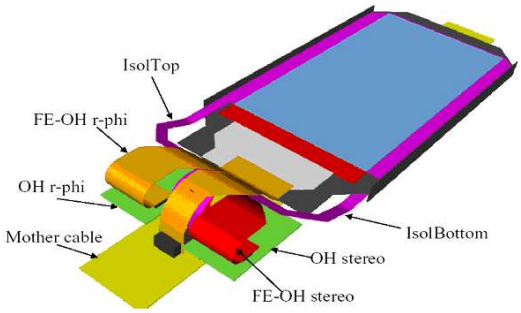

Figure 10: Mother Cable and a double-sided module

and information about type and number of modules connected through each MC type are shown for each TIB layer. The same information but for the TID MCs is shown in Table 2 for each ring (DS=double-sided, SS=single side).

TIB Layer	Name	mult	length(mm)	max width(mm)	modules per MC	module type
1	MC Forward Inner	31	679	32	3	DS
	MC Forward Outer	38	560	32	3	DS
	MC Backward Inner	34	599	32	3	DS
	MC Backward Outer	30	688	32	3	DS
2	MC Forward Inner	40	607	32	3	DS
	MC Forward Outer	47	700	32	3	DS
	MC Backward Inner	41	668	32	3	DS
	MC Backward Outer	47	552	32	3	DS
3	MC Forward Inner	53	674	32	3	SS
	MC Forward Outer	67	561	32	3	SS
	MC Backward Inner	51	589	32	3	SS
	MC Backward Outer	58	696	32	3	SS
4	MC Forward Inner	63	603	32	3	SS
	MC Forward Outer	67	699	32	3	SS
	MC Backward Inner	64	670	32	3	SS
	MC Backward Outer	67	560	32	3	SS
TOTAL		798				

Table 1: TIB Mother Cable types

6 Production tests

A group of dedicated devices was setup to automatically test the MCs after their production. The environmental conditions in which the MCs operate in the experiment were carefully reproduced in the laboratory, in order to verify their correct behavior.
In the following section a description of the used instrumentation, handling codes and the general utilities to setup and perform the verification tests of the circuit is given.

TID Ring	Name	mult	arc length(mm)	max width(mm)	modules per MC	module type
1	MC R1A	30	577	32	3	DS
	MC R1B	30	582	32	3	DS
2	MC R2	54	646	32	3	DS
3	MC R3A	27	516	32	5	SS
	MC R3B	27	529	32	5	SS
TOTAL		168				

Table 2: TID Mother Cable types

6.1 Hardware setup

A suitable hardware structure was developed in order to supply the MC with all the necessary electric references for its operation (bias, clock, trigger, etc.), and to guarantee the possibility of inserting all the measuring instrumentation used in the tests and to verify the operation of the MC.

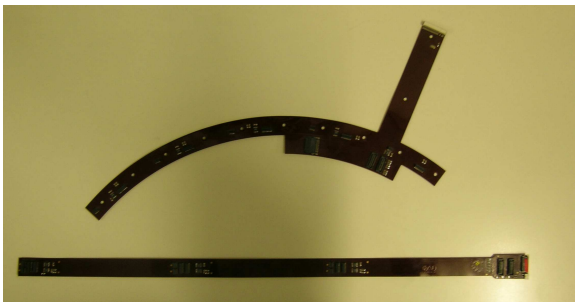

Figure 11: Mother Cables

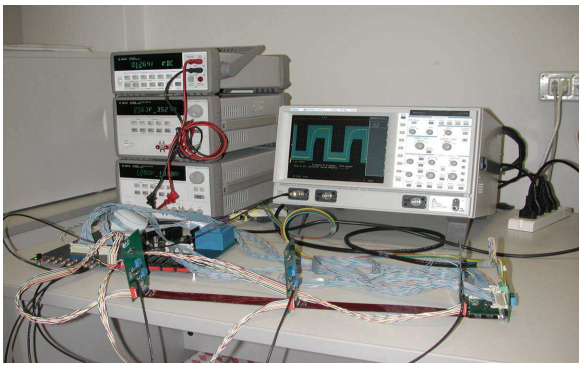

Figure 12: Test setup

In Figure 12 a picture of the test setup is shown. The two power supplies, the multimeter and the oscilloscope were connected to the computer by a standard GPIB bus (in this way it was relatively easy to develop a set of tasks running on a PC under a LabView environment using VI files), in order to control the simulation of the real tools. In addition to the dedicated software, a series of custom made electronic cards was designed and fabricated in Bari to give to the MC all the necessary inputs for its operation and to allow to comfortably insert all the measuring instrumentation used during the tests. The I/O card NI 6503, inserted in the PC bus, allowed the control of the operation of the custom electronics.

The set of custom made boards is composed by the Cable Test Board (CTB), shown in Figure 13, designed to coordinate and sort the signals used during the tests, and by three other different types of circuits directly connected to the MC as shown in Figure 14.

The first of these circuits, the Interconnect Board Probe (IBP), is a small card placed at the extremity of the mother cable, simulating the DOHM; it allows to power the cable to 1.28V and 2.56V and simultaneously pick-up the signals arriving on the connector which would go toward the Interconnection card.

On the IBP, in addition to the connectors for connection with the Mother Cables there are others that allow connection with the CTB and with the power supplies. The second circuit, CCU Probe (CCUP), has been designed to simulate the CCU. On the CCUP, a series of connectors is present. These allow to connect all the signal pins expected for the CCU in the CTB. A 40 MHz quartz is also present with a LVDS (Low Voltage Differential Signal) driver for the injection of a 40 MHz LVDS “clock” signal on the “clock” line. The third circuit, namely Frond End

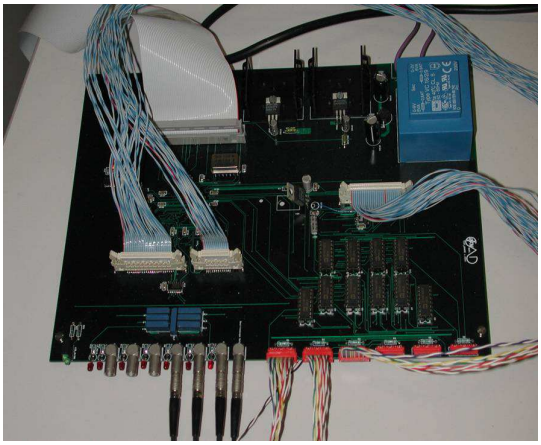

Figure 13: Cable Test Board (CTB)

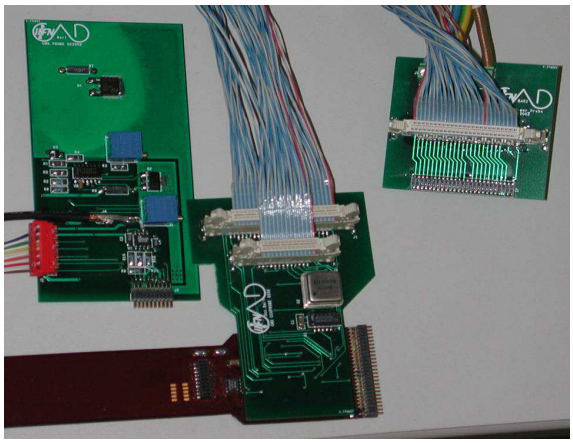

Figure 14: Cards to simulate real electronic Units: on the right side the IBP, on the center the CCUP, connected to the MC and on the left the FEP.

Probe (FEP), was inserted on the dedicated connectors, simulating the frond-end hybrid.
On the FEP two constant current generators are present. They are calibrated in such a way that on both power supplies supplies there is an absorption equal to the maximum one foreseen for both the opto-hybrid and the frond-end hybrid.
An operational amplifier chip is also present, that picks-up the LVDS 40 MHz "clock" signal, converts it to a "single-ended" one and sends it through a screened small cable to the CTB. One more function of the FEP is to pick-up all the signals of the I^2C lines and to send them to the CTB to check them.
The three circuits are shown in Figure 14. Going back to Figure 13, it can be seen, on the CTB, a power supply (blue box) that allows to have an independent 220 V system powered.
A series of coaxial connectors are connected by seven relays to the input of the oscilloscope, so the signal coming from each of these inputs can be selected to be displayed on the oscilloscope. Six of such relays have the function of monitoring the 40 MHz clock lines while the seventh one allows to connect the oscilloscope to another commutation matrix to monitor the I^2C signals arriving from another series of connectors.
The relays were controlled by the I/O card through custom logic using a FPGA (Field Programmable Gate Array). Setting by software on the I/O port a certain value on some of the configuration pins, the FPGA translates it into a series of logical levels "on" or "off" for the several relays, then the 40MHz "clock" signal is picked-up from the MC and visualized on the oscilloscope. The seventh relay, checked in the same way as the six previous ones, allows to connect the oscilloscope inputs to another analogical multiplexer. The latter is checked in turn by the C port of the I/O card and allows to monitor the entire series of the slow inputs. The signals of these inputs did not need coaxial cables to be transmitted, but simply 100 Ω lines. In this way the system allows to check all the I^2C lines and to verify the connection of all the CCU lines to the DOHM. On the CTB one more analog multiplexer is present, that takes care of the commutation of the inputs of the multimeter among the test points; precisely among the voltage sensing points on the connectors of the frond-end hybrid, and on the lines of the temperature sensors and high voltage power supplies.
This multiplexer is also controlled by a digital I/O port. Also in this case the FPGA translates the configuration written on the I/O port into a series of logical levels that activate or not some integrated circuits and select their inputs. Moreover the FPGA has been programmed to produce two types of signals: one open-collector signal to solicit the I^2C lines and another one in CMOS logic. The latter serves to solicit and then test all the other signals such the "reset" one, distributed to all the cards, and the signals that go toward the interconnection card. Through the FPGA it is possible to inject a signal on the line specified through the A port of the I/O card, holding all the others inactivated so that by a suitable software it can be checked that the signal is really present on the sensing points where it is expected while being absent on all the other points. In this way it is possible to detect the presence of short-circuits and/or cable defects.

6.2 Testing procedure

In this chapter we will describe the non-destructive tests performed in order to certify the correct operation of the MC before its integration in the CMS Tracker structure. To do that, a bias test, a "clock" signal test, an I^2C lines test and a HV test were performed. Since the MCs that connect the single side modules contain a smaller number of connectors in comparison to those that connect the double-sided modules, it was necessary to make two separate codes for each type of Mother Cable.

6.2.1 Test of low voltage distribution

This test is devoted to verify the correct working of the bias lines on the MC. Since the MC is composed by several copper and polyammide layers glued and pressed together, some copper layers may have a thickness smaller than the minimum allowed one. Moreover, during the production phase, a too aggressive chemical etching of the copper after being layerized may reduce its section below the expected values. The "vias" located on the MC which assure the connection with some of the different layers could be defective and finally also the existing connectors could have some imperfections, original or due to the soldering. Each of these issues might cause a voltage drop which could reduce the bias voltage of the active components of the readout hybrids, thus preventing them from working correctly. During this test, two power supplies are connected to the two ends of the cable via the IBP (which replaces the Interconnection Card), while each Front-end module is replaced by a FEP. As the front-end electronics needs a precision on the bias voltage value of $\pm 5\%$ of the nominal one, to simulate correctly the real experimental conditions, an input voltage of 2.5% higher than the nominal one (1.25 V and 2.5 V) was applied in order to verify if the measured voltages on the connectors are higher than 97.5% of the nominal one. After setting the two voltage values, using a special VI test program, the related currents were measured, verifying that they were within the expected tolerance.

6.2.2 Test of "clock" signal

The test of the "clock" signal was necessary for several reasons: the transmission line through which the signal propagated could be defective, or the amplifiers located on the MC could be defective as well and might have soldering problems, and so on. During this test two power supplies give the two operating voltages 1.25 and 2.50 V. The CCUP allowed to inject a 40 MHz signal on the "clock" line, then the signal was checked on the oscilloscope, overlapped with an acceptance mask previously set on the instrument (see Figure 15) with a special program called Mask Maker, taking into account the electrical characteristics of the signal: a minimum amplitude of $\pm$ 200 mV and a maximum rising time of 3 nsec. This test was repeated activating the various relays on the CTB in order to switch the input channel of the oscilloscope to test each connector.

6.2.3 Test of slow-control signals

This test is devoted to verify the correct transmission of the I^2C signals on the MC together with the detection of short circuits, if any, against ground, power planes and adjacent lines. From the CCUP card a slow signal was injected and visualized on the oscilloscope. The special relays on the CTB allow to connect the input of the oscilloscope with a bench of analog switches which had less bandwidth than the relays but are sufficient for the visualization of this kind of slow signals. With a dedicated VI program, after setting the two power supplies, the oscilloscope and the acceptance mask, the I/O port was configured to observe on the oscilloscope all the I^2C signals to be tested together with the acceptance mask (see Figure 15 again). This mask was built using the standard values which require a low level amplitude of 0.3 times the V250 voltage and a high level amplitude of 0.7 times the bias voltage with a rising time of 1 μsec and a falling time of 300 $nsec$. These values were the same as the ones used for the "reset" line and the lines of the interconnection card. The short circuit detection on the adjacent lines was done injecting a signal only on one of the CCUP output lines, expecting to see the same signal on the remaining ones in case of short circuit. The same procedure was applied for the "reset" and interconnection lines, injecting a slow signal through the CCUP and verifying its presence on each connector.

6.2.4 Continuity test of HV lines

In order to avoid the addition of new custom cards, the electrical continuity of the HV lines was tested in a different way compared with of the previous mentioned tests.
On the pin of each connector corresponding to the HV line powering the modules connected on the MC, a resistor was inserted simulating the effective load on the line. These resistors were connected in parallel. Then, with a

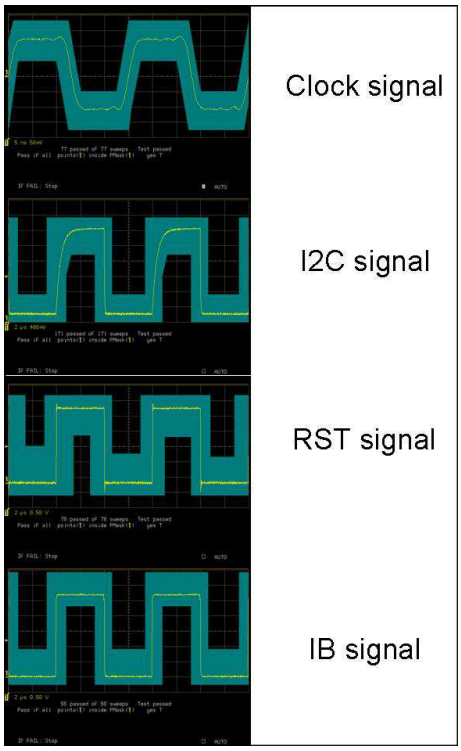

Figure 15: Signals on the oscilloscope and their acceptance mask (green area)

precision multimeter, the value of the resistor parallel was measured on the HV line. If that value was compatible with the expected one the line was considered as conductive and the test declared passed.

7 Conclusions

In this note several aspects related to the construction of about 1000 special cables called "Mother Cables" used to power and inter-connect the about 4000 modules of the CMS Inner Tracker has been described. A set of custom-made devices and custom-designed tests to check their correct behaviour before the installation on the Inner Tracker structure has been illustrated.

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