The Commissioning status and results of ATLAS Level1 Endcap Muon Trigger System

Y. Okumura[a], S. Hasegawa[a], T. Sugimoto[a], Y. Takahashi[a], M. Tomoto[a],
C. Fukunaga[b], M. Ikeno[c], H. Iwasaki[c], K. Nagano[c], M. Nozaki[c], O. Sasaki[c], Y. Suzuki[c], S. Tanaka[c], Y. Yasu[c],
Y. Hasegawa[d], H. Oshita[d],T. Takeshita[d], M. Nomachi[e],Y. Sugaya[e], S. Hirayama[f], M. Ishino[f],
N. Kanaya[f], F. Kanega[f], T. Kawamoto[f], K. Kessoku[f], T. Kobayashi[f], T. Kubota[f], H. Nomoto[f], H. Sakamoto[f],
T. Hayakawa[g], A. Ishikawa[g], T. Kadosaka[g], K. Kawagoe[g], H. Kiyamura[g], H. Kurashige[g],
T. Matsushita[g], H. Nakatsuka[g], T. Niwa[g], A. Ochi[g], C. Omachi[g], H. Takeda[g] ,
N. Lupu[h], S. Bressler[h], S. Tarem[h], E. Kajomovitz[h], S. Ben Ami[h], A. Hershenhorn[h],
Y. Benhammou[i], E. Etzion[i], D. Lellouch[j], L. Levinson[j], G. Mikenberg[j], A. Roich[j]

[a]Nagoya University, Nagoya, Japan
[b]Tokyo Metropolitan University, Hachioji, Japan
[c]KEK, High Energy Accelerator Research Organization, Tsukuba, Japan
[d]Shinshu University, Matsumoto, Japan
[e]Osaka University, Osaka, Japan
[f] ICEPP, University of Tokyo, Tokyo, Japan
[g]Kobe University, Kobe, Japan
[h]Technion Israel Institute of Technology, Haifa, Israel
[i]Tel Aviv University, Tel Aviv, Israel
[j]Weizmann Institute of Science, Rehovot, Israel

Yasuyuki.Okumura@cern.ch

Abstract

The ATLAS Level1 endcap muon trigger selects potentially interesting events containing muons with the transverse momentum (p_T) greater than 6 GeV/c from 40 MHz proton-proton collisions. The system consists of 3,600 Thin Gap Chambers (TGCs) and the total number of readout channels is 320,000. The trigger logic is based on the coincidence between seven layers of TGCs. All processes are performed on fast electronics within 2.5 μs. To be ready for the first beam, we have succeeded in sending trigger signals of cosmic-ray muons with the synchronous operation at 40 MHz and fine signal timing adjustment. We report on the status of the commissioning and the results from the combined runs with all ATLAS detectors.

I. INTRODUCTION

The ATLAS experiment at CERN will start exploring new physics up to TeV energy scale at the beginning of spring 2009. We will start from the proton-proton collisions with a single bunch, and then the bunch-crossing rate will be increased to 40 MHz. In order to select interesting events efficiently with rejecting the large backgrounds generated with the production rate of 1 GHz (25 minimum bias events will be expected in a single collision, i.e. 25×40 MHz $= 1$ GHz), three levels of the trigger are designed at the ATLAS experiment. The first stage of the trigger (Lvl1) is based on the dedicated fast electronic circuits and makes a trigger decision to the second stage of the trigger (Lvl2) within 2.5 μs. The Lvl2 trigger and the third level of trigger, so called the event filter (EF), are performed by the simple event reconstruction codes on computers. The muon detectors and the calorimeters provide the Lvl1 trigger and reduce the event rate from 1 GHz to 75 kHz, while the Lvl2 and the EF select the events of interest more precisely using the muon detectors, the calorimeters, and the tracking systems and reduce the event rate from 75 kHz to 2 kHz, and from 2 kHz to 100 Hz, respectively.

The Lvl1 is a system of pipelined processors synchronized with the clock of 40 MHz, which is delivered from the clock of the LHC accelerator, so that all readout electronics of the subdetectors can identify the bunch-crossing numbers of interesting events, which are tagged by the Lvl1 trigger signals. Therefore, the constant latency and synchronous of the Lvl1 systems are mandatory. Since some of the trigger electronics are mounted on the detectors and the others are located in the shielded counting room, it is crucial to handle the latency and the timing of the trigger signals step by step as well as channel by channel.

In this paper, we report on the commissioning of the Lvl1 endcap muon trigger system and the results of the trigger analysis based on the data taken during the combined runs. In particular, we focus on how we handle the pipeline of the Lvl1 endcap muon system.

II. TGC TRIGGER

A. Thin Gap Chamber

The ATLAS detector has two kinds of muon trigger detectors. One is the Resistive Plate Chamber (RPC), which is located in the barrel region (pseudo-rapidity $|\eta| < 1.05$), and the other is the Thin Gap Chamber (TGC), which is located in the two endcap regions ($1.05 < |\eta| < 2.4$). The TGC is the gas chamber with multi-wires operated at the limited proportional

region (typical high voltage is 2,800 V). The small cell size with the short intervals of wires (1.8 mm) makes the time jitter less than 25 ns, which is comparable with the interval of the bunch-crossing. Thus, the TGC can distinguish a bunch-crossing of an interesting event from the others. The typical size of a TGC unit is around 1.5 m^2, and around 600 TGC units construct a wheel-shaped TGC station of 25 m in diameter, as shown in Figure 1.

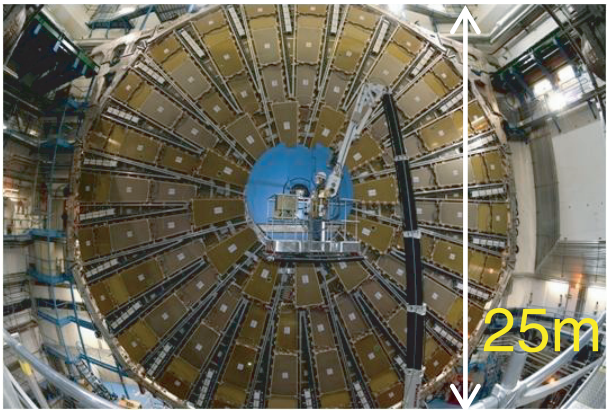

Figure 1: A picture of the TGC wheel. Almost all infrastructure including chambers, chamber services, electronics have been installed successfully in the ATLAS cavern at the beginning of 2008.

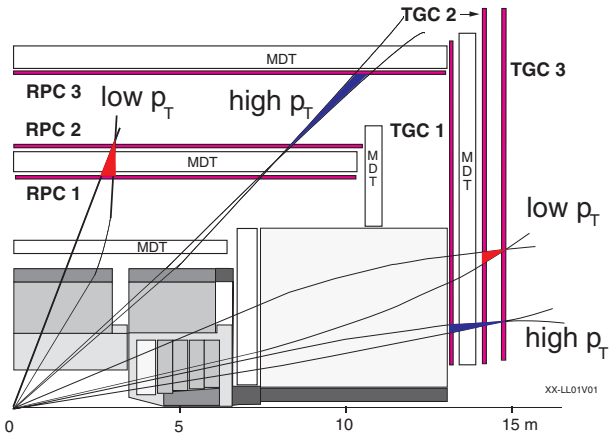

Figure 2: The cross-section diagram of the muon detectors looking at one fourth y-z plane. The scheme of the fast muon track finding is also overlaid. The TGC trigger finds muon tracks by taking coincidence between hits on three TGC wheels. Depending on the coincidence windows, low p_T or high p_T is determined. [1]

There are two kinds of TGC units. One consists of 2 gas gap layers (doublet), and the other consists of 3 gas gap layers (triplet). The inner-most TGC station (TGC1), which consists of TGC units with triplet-layer, stands vertically 13 m apart from the interaction point in z coordinate defined by direction of the beam pipe. The middle TGC station (TGC2) and the outer-most TGC station (TGC3), which consist of doublet TGC units, stand vertically 14 m and 15 m in z direction, respectively (Figure 2).

Totally there are seven wire-gap layers at each endcap and total number of channels including the anode wires and the cathode strips is about 320,000. The readouts from the wire and the strip reconstruct the hit position of the muon track in the vertical direction with respect to the beam pipe (r) and in the azimuth angle (ϕ), respectively. Using fixed z position of the wheel allow us to reconstruct the muon track trajectory three-dimensionally.

B. *Trigger Electronics*

Figure 3 shows an overview of trigger electronics.

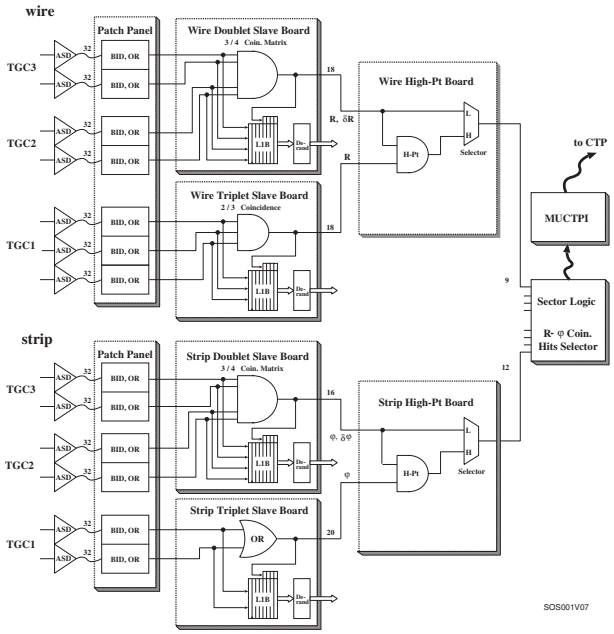

Figure 3: The TGC trigger electronics. Three steps of coincidence logic find high p_T muon track out with r-ϕ coincidence. [1]

The wire and strip signals from TGC are amplified, shaped, and discriminated on the Amplifier Shaper Discriminator circuit (ASD) on the TGC. Digitized signals are fed into Patch-Panel ASICs (PP-ASIC). Because of varieties of the time-of-flight (TOF) from the interaction point to the TGC and the cable length from the ASD to the PP-ASIC, the timing of the signals from ASD are not aligned between the channels at the PP-ASIC inputs. The difference of the timing between ASD outputs is adjusted by the PP-ASIC. The PP-ASIC also applies a proper bunch-crossing identification (BCID) for each hit, so that the coincidence logics are performed properly in the next circuit (Slave Board ASIC ; SLB-ASIC). The SLB-ASIC performs a coincidence between four layers in the The TGC2 and the TGC3 (the pivot plane) and three layers in the TGC1. While 3 out of 4 layers coincidence and 2 out of 3 layers coincidence are usually taken for the pivot plane and for the TGC1, respectively, the trigger condition can be tightened or relaxed depending on the beam condition, the noise rate of the TGC, and the response of the TGC. The outputs from SLB-ASIC are fed into High-p_T coincidence Boards (HPT). The HPT combines coincidences from the TGC1 and pivot plane to find high p_T track

candidates. Information provided by the HPT is r and δr for the wire signals, and ϕ and $\delta\phi$ for the strip signals. The (r, ϕ) and the (δr, $\delta\phi$) mean the coordinate of muon tracks on the pivot plane and the deviation of hits on the TGC1 between the track trajectory of the virtual infinite momentum and the real track trajectory which is bent by the toroidal magnet, respectively. The HPT outputs are fed into the Sector Logic Boards (SL), which determine the momentum of the muon track by making coincidence based on ($r, \delta r, \phi, \delta\phi$). The momentum of the muon track, which is quantized by six p_T thresholds, is calculated by the δr and $\delta\phi$. In case of multi-candidates of the muon tracks, two muon candidates with the highest and the second highest p_T are selected. Since the trigger logics in SL are based on the Field Programmable Gate Array (FPGA), the requirements of the p_T threshold can be implemented whenever the experimental conditions are changed. The lists of the muon candidates are sent to the Muon Central Trigger Processor Interface (MUCTPI), which combines the number of the muon candidates provided by the TGC and the RPC triggers and makes the final decision of the muon trigger.

C. Requirements on Operation

Since the individual modules and a part of the trigger systems have been tested well during the development and the assembly of the TGC system, we focus on establishing a complete pipelined trigger system synchronized with the 40 MHz clock. In particular, the TOF between the interaction point and the TGC chambers are different depending on the η, and 45 varieties of the cable length between the ASD and PP-ASIC are used as shown in Figure 4.

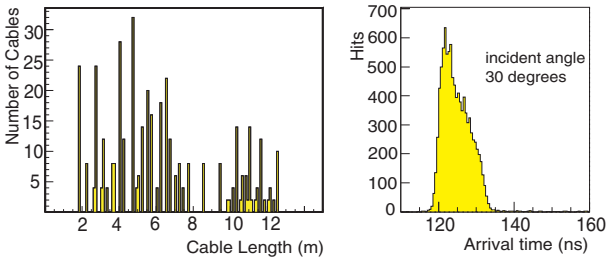

Figure 4: Left: The varieties of the cable Length. Right: TGC response for 30 degrees incident angle. [2]

We also use two varieties of the category 6 twisted pair serial links between the SLB and the HPT, and 26 varieties of the optical fiber links between the TGC detector and the counting room, so as to pass the cables with the minimum length. In order to make three kinds of coincidences described in the previous section, all signals need to be aligned properly. All ASICs and FPGAs have a functionality to delay the signals accordingly. Since the response of the TGC is varied within 25 ns due to the drift time as shown in Figure 4, the the gate width needs to be optimized and the phase of the 40 MHz clock also needs to be set at the best position for the coincidences.

Furthermore, the goodness of the synchronization is not trivial, in particular, for such a high speed data transfer. The trigger links between the HPT and the SL send more than 12,000 bits in every 25 ns without any idle cycle. A proper procedure for synchronization is mandatory.

III. Commissioning

Figure 5 summarizes variable delay functionalities. As described in the previous sections, due to the TOF and many varieties of cable length, the timing of the trigger signal needs to be adjusted in every circuits before making coincidences.

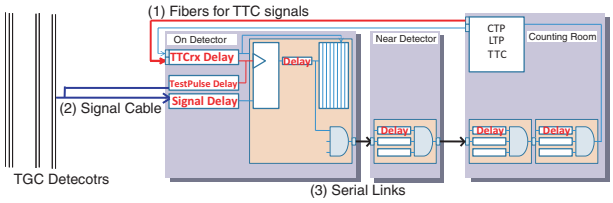

Figure 5: Variable delays to align signals timing in each component.

So as to send the Lvl1 muon trigger signals with the constant latency synchronized with the 40 MHz clock, we need to take care of

- timing alignment of the control signals,
- absorbing delays due to the varieties of TOF and cable length,
- absorbing delays due to varieties of category 6 serial links, and
- absorbing delays due to varieties of optical fiber links.

In the following subsections, we report on how to control these items in the ATLAS cavern.

A. Timing Alignment of the control signals

In the ATLAS experiment, the control signals including the 40 MHz clock, the Lvl1 trigger accept (L1A), the event counter reset (ECR), the bunch counter reset (BCR), the hardware initialization, and the test pulse trigger are distributed by the Timing, Trigger and Control (TTC) system [3]. Handling the timing of the control signals from TTC is crucial. In particular, the phase of the 40 MHz clock needs to be aligned channel by channel. Otherwise some channels may have an extra delay comparing with the other channels. For the TGC trigger system, the TTC system is located in the counting room and the all control signals are distributed from there to all hardware registers via several varieties of the optical fiber links. The propagation delay of each fiber link has been measured in the ATLAS cavern. The fastest control lines from the counting room to the electronics on detector are 251 ns, while the latest ones are 452 ns. The difference of them (i.e., $452-251 \simeq 200$ ns) needs to be absorbed at the receiver of the TTC signals on detector, so called the TTCrx chip, which can set the variable delay with the resolution of 100 ps (fine tuning) and 25 ns (coarse tuning) [4]. Configuration

procedure for the TTCrx chip delay has been established in the ATLAS Data Acquisition System framework to have LHC clock signals with the same phase in all front-end electronics.

B. *Delays due to TOF and varieties of the Cable Length*

The timing of the signals at the input of the PP-ASIC is different channel by channel due to the TOF and the varieties of the cable length. The difference needs to be aligned in the PP ASIC, before the SLB ASIC starts the first coincidence. The PP ASIC has a functionality of a variable delay which can set an additional delay for each channel. The delay can be varied from 0.9 ns to 28.5 ns with 32 quantized steps by using phase locked loop circuits.

The difference of the cable propagation delay can be emulated with the test pulse. As shown in Figure 5, the test pulse can be generated for all 320,000 channels, and the timing of the test pulse is configurable with the test pulse variable delay, which can be set with 0.9 ns steps (fine tuning) and 25 ns steps (coarse tuning). The propagation delay for each channel has been measured in the ATLAS cavern by scanning the response for the test pulses with several variable delays.

The delays due to the varieties of the TOF are simply calculated, assuming the muon tracks with the infinite momentum that come from the interaction point. Further fine tuning will be done using the beam collision data.

We estimate the propagation delay due to the sum of the cable length and the TOF from 64.7 ns to 116.0 ns. Based on these measurements, proper values of variable delays for all channels are set at the configuration process in the ATLAS data acquisition framework.

C. *Delays due to varieties of the Serial Link length*

After the SLB ASIC, the trigger signals need to be synchronized with the 40 MHz clock via high speed serial links (category 6 serial links). Before the coincidence between the pivot and TGC1 plane, the difference of the propagation delay in the serial links needs to be absorbed, because we use the different length of cables for the pivot plane and the TGC1 plane. The serial link receiver in the HPT has functionalities of the variable delays and the switches of clock edges for latching input signals to align the input signals, and to absorb the phase difference between input signals and the 40 MHz clock on the trigger processor, as shown in Figure 6. The same functionalities are implemented for the optical links between HPT and SL.

The patterns of the test pulses emulating high-p_T muon tracks are used to optimize these delays. The wrong configuration of these delays causes the missing of coincidences, the instability of the latency, and the wrong correlation between the inputs and the outputs. 2,100 test track patterns have been sent via the serial links (12,096 bits/clock) and output patterns have been checked to be perfectly same as expected. The proper configuration of the delays for all serial links has been identically set from this measurement.

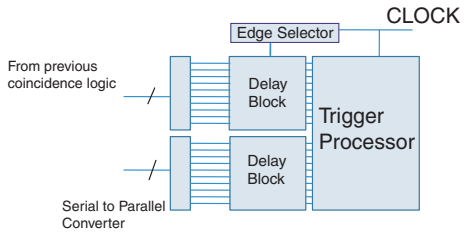

Figure 6: Block Diagram of input delay at receiver side of serial links. It consists of delay with 25 ns steps, and the clock edge selector for latching input signals.

D. *Synchronization of the signals via optical fiber links*

We use the Agilent HDMP-1032/1034 Transmitter/Receiver chip set for the communication between the HPT and the SL via the optical fiber links (G-Link) [5][6]. A 20-bits parallel word including a 4-bits coding field (c-field) and a 16-bits word field (w-field) are defined in this data transfer. 20-bits per an optical link are sent as the result of the muon track candidates at every 25 ns, which means the trigger system makes the decision of the muon trigger at every bunch-crossing. However, all “0” bits transfer, which means no muon candidates in an event, causes sometimes the problem with the synchronization between the HPT and the SL, because of two allowed data patterns of the optical fiber link. Therefore we need a special manner to solve this problem.

The G-Link protocol allows two kinds of data transfer, either 17-bits data transfer or 16-bits data transfer, depending on the setting of the 4-bits c-field. The 4-bits c-field must be “1011” in case of the 17-bits transfer mode, while c-field must be “1101” in case of the 16-bits transfer mode. Both transfer modes can be accepted for the communication of the SL with the HPT. If no muon candidates are found, HPT may send the pattern of w-field=“0000 0000 0000 0000” and c-field=“1101”, followed by the inverted pattern (w-field=“1111 1111 1111 1111” and c-field=“0010”). In this case, however, the pattern with shifting by 1 bit, w-field=“0000 0000 0000 0001” and c-field=“1011”, followed by the inverted pattern (w-field=“1111 1111 1111 1110” and c-field=“0100”) can also be acceptable. This alternative causes the wrong synchronization and results the incorrect data transfer.

So as to solve this problem, we set the unique idle word (w-field=”1111 1111 0000 0000” and c-field=”0011” followed by w-field=”1111 1100 0000 0000” and c-field=”0011”) at the beginning of the synchronization and establish the following the synchronization procedure;

1. Set the idle mode before the data taking.
2. Keep the synchronization to be locked.
3. Change the idle mode to the data transfer mode, when the data taking starts.

The procedure has been added into the ATLAS data acquisition procedure and confirmed to work well.

IV. Combined Run

A. Combined run with the Cosmic Ray

Since the cosmic ray does not come from the interaction point but top of the ATLAS cavern, the trigger condition for the cosmic ray is set as the coincidence on the only pivot plane. With this condition, the total rate of the TGC trigger for the cosmic rays is around 50 Hz.

Since the data of the cosmic rays are collected by the TGC-self trigger without the synchronization with the beam-bunch crossing, in this combined run we check a part of trigger chain. We learn from the cosmic data that the trigger latency in the pipelined system (from the SLB coincidence logic to the SLB fifo buffer memory shown in Figure 5), measured as 91 clocks (=2.275 μs), is fast enough. This assures the latency from the collision is shorter than the ATLAS requirement of 2.5 μs. Furthermore it is stably pipelined with the constant latency, which means the adjustment of the delays are well under-controlled.

B. Combined run with Proton Beam

On September 10th, 2008, we have successfully circulated the first proton beam with a single bunch in the LHC accelerator. The ATLAS has taken the data and seen the muons from the collision of the proton beams with the materials inside the beam pipe (the beam halo). We use not only the usual trigger with the 3-station coincidence but also the special trigger for the beam halo data which requires only hits on the pivot plane, in order to take the data of the beam halo effectively. Using the beam halo data allows us to measure the timing of the trigger for the tracks coming from the beam pipe. Since we can measure the timing when the proton beam passes the ATLAS detector (beam pickup trigger), comparing the timing of the TGC trigger with the beam pickup trigger tells us whether the TGC trigger timing is tuned for the beam collision. Figure 7 shows the TGC trigger timing with respect to the beam pickup trigger, in case the proton beam pass from one endcap side to the other.

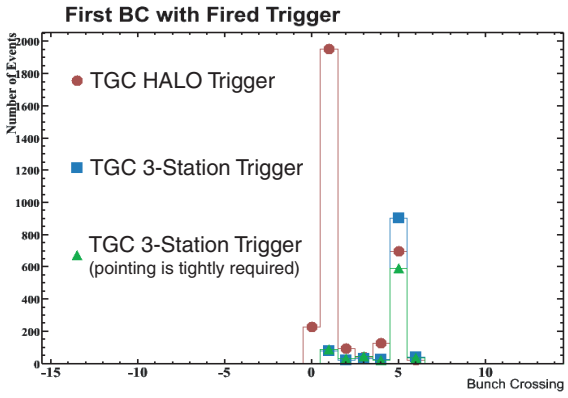

Figure 7: Trigger Timing of TGC trigger based on beam pickup signals in first beam circulation. The two peaks are corresponding to trigger signals generated in both endcaps. The difference between these two peaks is to equivalent to TOF between both sides accurately.

Two sharp peaks around 1 and 5 correspond to the timing of the both of endcaps. The difference of two peaks (= 4 bunch-crossing, i.e. 100 ns) indicates the TOF of the proton beam between endcaps ($\sim$ 30 m) with the light velocity. We find that the timing of the TGC trigger is under-controlled for the beam collisions. Only concern is the width of the peaks is not within one bunch-crossing. This is understood because the estimation of the TOF for timing alignment is not for the tracks from the beam halo but for the tracks from the beam collision. We expect that the width of peaks should be within one bunch-crossing for the only beam collision data.

V. Future Plan

Further improvements of the TGC trigger can be done only with the data of the proton-proton collisions. They include the optimization of the phase difference between the signal and the clock, the optimization of the gate width of the signal, and the optimization of the high voltage and the threshold voltage. They are all under preparation to be achieved as soon as we have first collision data.

VI. Conclusion

Since the installation of all hardware components has been successfully finished at the beginning of 2008, we have been concentrated on the timing study for the beam collision and on the establishment of the operation procedure. All we can do without the beam collision have been done systematically. Furthermore, in the commissioning we have fixed the mis-connections of the cables, and the bad modules and chips. The data taken with the cosmic rays and the first proton beam circulation indicate that the signal timing is fine-adjusted and the latency is well-understood. We are await for the first beam collision to search for the physics beyond the standard model, using muons triggered by the TGC which is well-understood.

VII. Acknowledgment

We are greatly indebted to all CERN's departments and to the LHC project for their immense efforts.

References

[1] ATLAS First Level Trigger Technical Design Report CERN/LHCC/98-14 (1998)

[2] ATLAS Muon Spectrometer Technical Design Report CERN/LHCC/97-22 (1999)

[3] Timing, Trigger and Control (TTC) Systems for the LHC, `http://ttc.web.cern.ch/TTC/intro.html`

[4] J. Christiansen *et al*, TTCrx Reference Manual(2005)

[5] Agilent Technologies, Inc. Palo Alto, CA 94306, USA `http://www.agilent.com`

[6] Agilent HDMP-1032/1034 Transmitter/Receiver Chip Set Data Sheet, Agilent Technologies, Inc. (2000)