A Monolithic Active Pixel Sensor for a "Tera-Pixel" ECAL at the ILC

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Abstract

The leading proposed technology for electromagnetic calorimeters for ILC detectors is a highly granular silicon-tungsten calorimeter. We have developed an active pixel sensor for such a calorimeter, which would have extremely fine granularity, allowing binary pixel readout. A first generation chip (TPAC1.0) has been fabricated, and this contains a 168x168 pixel array, consisting of 50x50 micron pixels. Each pixel has an integrated charge pre-amplifier and comparator. TPAC1.0 has been manufactured in a 0.18 micron CMOS "INMAPS" process which includes a deep p-well implant. We present recent results of the performance of the TPAC1.0 sensor together with comparison to device-level simulations.

I. Introduction

The ILC physics program [1],[2] requires detectors with unprecedented jet energy resolution. To achieve this goal, the detectors will need highly granular calorimeters and, for the electromagnetic calorimeter, the use of a silicon-tungsten calorimeter has been favoured. The granularity and readout requirements of such a calorimeter are closely interrelated.

Detailed simulations [3],[4] show that a pixel size of 50x50 microns results in most pixels only being hit once per event. Thus we can employ a simple binary readout using a comparator instead of an analogue measurement.

CMOS monolithic active pixel sensors (MAPS) have been previously demonstrated as suitable devices for high energy physics applications [5],[6] and so this sensor concept offers the opportunity to implement the necessary fine pixel size and integrated readout and timing electronics in a single silicon die.

The sensor specification is therefore for small pixels that are able to detect an incident minimum ionising particle (MIP); the timestamp and location of such hit events are then stored in local memories for readout in between bunch trains at the ILC. The location of hits in multiple layers of these sensors allows for reconstruction of particle showers thus implementing a digital measure of calorimetry.

The pixel requirements and intended operating mode require some in-pixel analogue signal processing, threshold discrimination and control logic, thus many transistors of both nmos and pmos types: As the charge-collecting junction is formed by an n-well and the p-doped substrate, the n-wells which form the substrate of PMOS transistors would present a significant reduction in the charge-collection efficiency of the pixel. In order to avoid these charge losses, an advanced 0.18 micron CMOS process has been developed, called *INMAPS*, which features an additional deep p-well implant to shield unrelated n-wells from collecting charge.

A first prototype, the "Tera-Pixel-Active-Calorimeter" sensor, or TPAC1.0, is shown in Figure 1: The device has been well characterised in the past months, with many results included in this document. The results of this recent testing have been used to select a preferred pixel architecture for the TPAC1.1 sensor which is currently in manufacture.

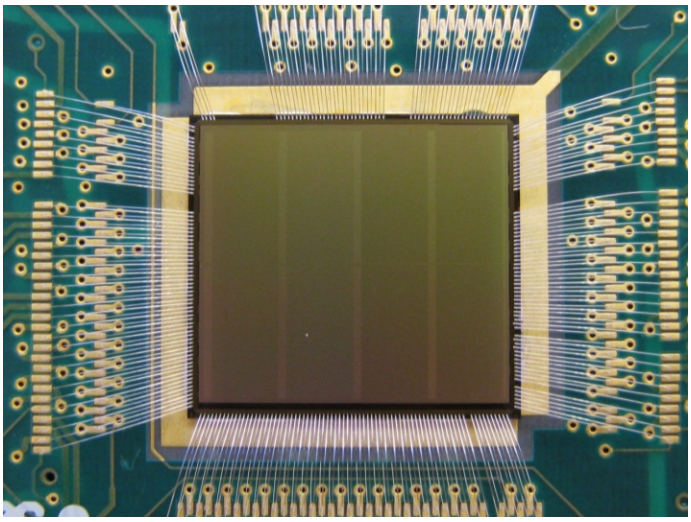

Figure 1: TPAC1.0 Sensor photograph.

II. Electronic Circuits

A. Sensor Architecture

The TPAC1.0 sensor comprises 28,224 pixels, row control logic, on-chip SRAM memory banks and I/O circuitry in a 9.7x10.5mm^2 die. The sensor collects the charge deposited by an incident particle in pixels arranged on a 50 micron pitch. This signal is compared with a global threshold and if a particle is detected, the time-code and location of the event are recorded in memories for readout at a later time. The physics of the target application is such that real incident particles are extremely rare; hence artificial hits caused by electronic noise will dominate the volume of hits that are stored and read out.

Four different pixel designs are implemented for evaluation, which fall into two distinct architectures. A common control and readout architecture serves all pixel varieties, allowing the sensor to be operated as a whole or as sub-regions. Pixels may be individually masked, allowing any permutation of single pixels to be operated and evaluated.

B. Pixel Architectures

1) The preShape pixel

The preShape pixel is based on a conventional analog front end for a charge-collecting detector. The four diodes are connected (in parallel) to a charge preamplifier, which generates a voltage step output in proportion to the collected charge. A CR-RC shaper circuit generates a pulse output in proportion to the input signal with further circuit gain to yield 94uV/e- with respect to total input charge. This signal, along with a local common-mode reference form a pseudo-differential input to the two-stage comparator. The shaper circuit returns to a stable state, depending on the signal size, and is then able to respond to another input signal.

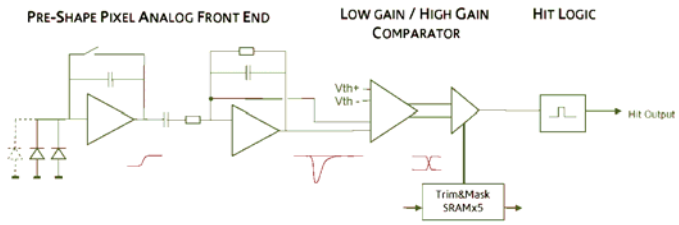

Figure 2: preShape pixel circuit diagram.

The in-pixel comparator has two parts: the first takes two differential signals, and produces a real-time differential discrimination result, with some small analog signal gain. The second comparator generates the full-swing discriminator output, and applies offset trim adjustment with 4-bit resolution. The output of the comparator is enabled with a 1-bit mask input which can be used to prevent the pixel from generating hit events.

Pixels generate a fixed length pulse using a monostable circuit, which is connected to row control logic outside the pixel. The length of the output "hit" pulse is independent of the signal size.

To achieve high circuit gain in the preamplifier, a small value of feedback capacitance was required, which was made using two larger capacitors in series to comply with manufacturing design rules. Two different simulation tools were used to evaluate the optimum orientation of the series feedback capacitors, but the two tools selected different topologies for highest gain. Two capacitor orientations are therefore implemented on the TPAC1.0 sensor as subtle variants of the preShape pixel.

2) PreSample pixel

The preSample pixel is based on a conventional MAPS sensor [7], with in-pixel analog storage of a reference level. Charge integrates on the four collecting diodes, causing a small voltage step proportional to the collected charge and the node capacitance. A charge preamplifier provides gain to generate a larger voltage step which, along with a local sample of the reset level, forms a pseudo-differential input to the two-stage comparator. The voltage step is generated in proportion to the input signal to yield 440uV/e- with respect to total input charge. The charge amplifier and reference sample must be reset after a hit event before the pixel can detect another hit, which is undertaken by the in-pixel logic.

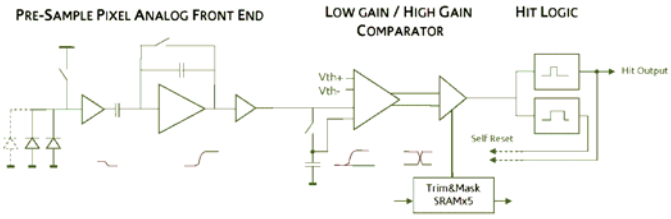

Figure 3: preSample pixel circuit diagram.

The in-pixel comparator stage is common to all pixel architectures, but the preSample pixel includes an additional monostable circuit to generate the self-reset signals that are necessary to prepare the amplifier and reference sample for another hit event.

Similar to the preShape pixel, a small capacitance in the preamplifier feedback is made with two capacitors in series. This gives rise to two subtle variants of the preSample pixel, again based on results from different simulator tools.

C. Logic Columns

The row logic is responsible for monitoring the individual hit outputs from a row of 42 pixels and writing details of any hit events to local memory. An external clock defines the timing with which hit signals are sampled. The hit signal from a pixel is asynchronous, but will have a fixed pulse-width defined by the in-pixel monostable bias setting. This pulse length is set to be O(10%) greater than the hit sampling period, which is generally matched to the bunch crossing rate of the target application. This regimen ensures that an asynchronous hit will always be sampled by the synchronous logic, with a small probability that it will be sampled twice: This is an acceptable data overhead that allows for a reasonable spread in the length of the monostable pulses, with a minimal risk that an entire hit pulse occurs between sampling and hits are therefore lost. The sampling of hits uses a "ping-pong" circuit architecture to ensure there is no dead time between samples.

The row control logic has 19 SRAM registers available for storage of hit data. A memory controller is implemented to organise the use of these registers, such that registers are not overwritten once used, and only those with valid data participate in readout.

The row control logic may be operated in "override" mode, whereby the pixel "hit" inputs are ignored and the value of the hit pattern in each bank is always stored. This operating mode fills the memories in less than 3 complete cycles of the standard control sequence, and so is only intended as a test feature.

The 19 SRAM registers occupy the full 50 micron row pitch. The hit pattern and corresponding multiplex address are stored in the first 9 bits of a register, with a further 13 bits

used to store the global timestamp code, which is incremented each time hit signals are sampled. The cross-coupled inverter structure of a SRAM cell ensures the data will be held indefinitely provided the cell is powered, so there is no requirement to refresh the data for a maximum hold time after which data is corrupted.

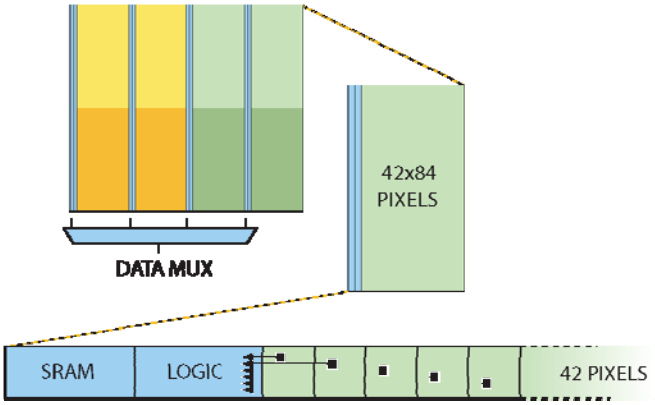

Figure 4: TPAC1.0 sensor floor plan diagram.

The full TPAC1.0 sensor comprises 4 columns of row logic, each with 168 rows, hence there are 12,768 SRAM registers of 22 bits each in total.

The row control logic and the SRAM register bank occupy a 250 micron wide region adjacent to the 42 pixels. The logic and SRAM are insensitive to incident particles; therefore this structure has an inherent 11% dead area.

III. INMAPS Process Technology

To ensure the success of this design it was essential to develop an additional processing step in a commercially available standard CMOS technology. The pixel designs implement many transistors inside the pixel that, in a standard CMOS process, would introduce a significant reduction in charge collection efficiency.

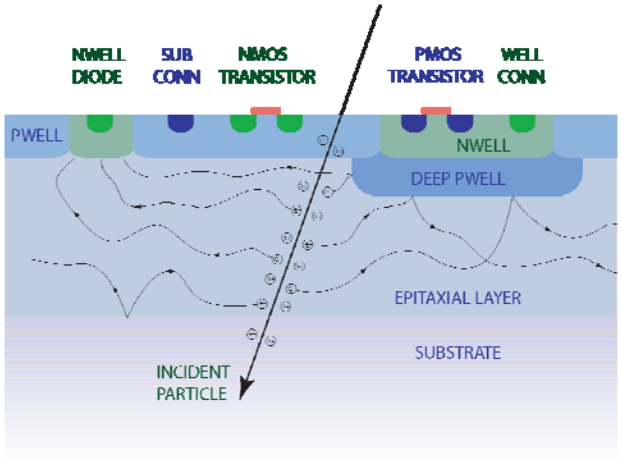

Figure 5: INMAPS process cross section diagram illustrating charge diffusion due to an incident charged particle. The deep p-well prevents diffusing charge from being collected by the n-well of in-pixel PMOS transistors.

An incident charged particle deposits electron-hole pairs along its trajectory through the epitaxial silicon layer. This charge diffuses within the region defined by the barrier formed between the epitaxial layer and the bulk silicon. The lifetime of such carriers is long, so they are most likely to reach a collecting n-well diode at a positive potential. Carriers that pass close to a diode are collected and form the signal charge input to the pixel circuits. A charge-collection efficiency reduction occurs when PMOS transistors are also present in the pixel, since these sit also in an n-well that is held at a positive potential. Carriers that pass close to these unrelated n-wells will be lost as they are absorbed by the power supply.

In order to protect the diffusing charge from n-wells of pixel circuits, a high energy "deep p-well" implant is added to the wafer processing. The diffusing charge sees this small change in doping concentrations as a potential barrier and is reflected away from the proximity of the n-well, as illustrated in Figure 5: This implant is essential to the charge-collection efficiency of the pixel, and the success of the sensor. Further information may be found in [8].

A. Pixel Layout

The layout for the two pixel architectures is shown in Figure 6: up to the first metal layer, with the key circuit blocks illustrated. The 50micron pixel boundary is marked with a dotted line, although some circuit blocks extend beyond this boundary the pixels tile correctly to form an array. The preShape and preSample pixels contain 160 and 189 transistors respectively and approximately 30 capacitors. Both pixel layouts have the four diodes in the same location, near the corners for optimum charge collection.

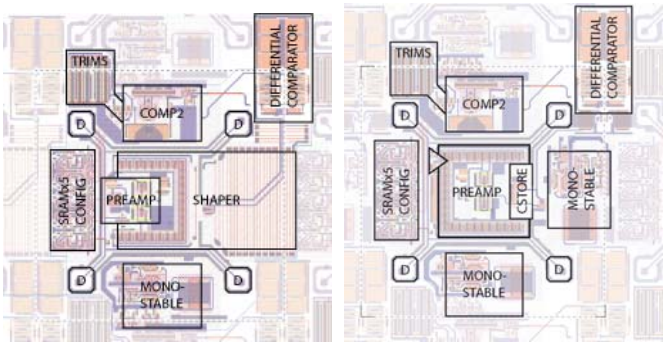

Figure 6: Annotated pixel layouts: preShape/preSample up to M1.

The deep p-well layer is added to the pixel layouts, illustrated in Figure 7: The deep p-well is placed as a symmetrical cross structure, leaving only the four collecting diodes exposed to the charge diffusing in the substrate. The deep p-well geometry is common to all pixel varieties.

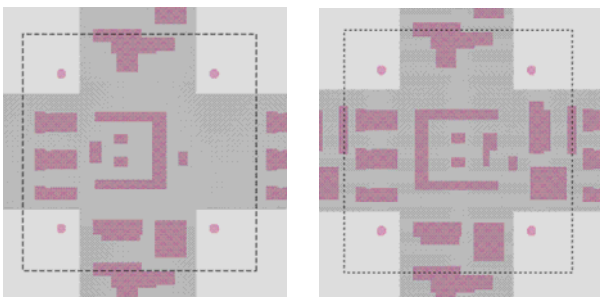

Figure 7: Pixel layouts: preShape (left) and preSample (right) showing only n-well(pink) and deep p-well (dark gray).

B. *Device Simulation*

The behaviour of diffusing charge in the substrate was modelled in ISE-TCAD tools, using the GDS data of the submitted design. Charge is "deposited" at a number of points in the pixel: The charge collected at each pixel diode, and the time-profile of this collection is simulated. Sample results from these simulations are shown in Figure 8: Two profiles through the pixel are shown, profile F passes through the very centre of the pixel, while profile B passes close to two diodes.

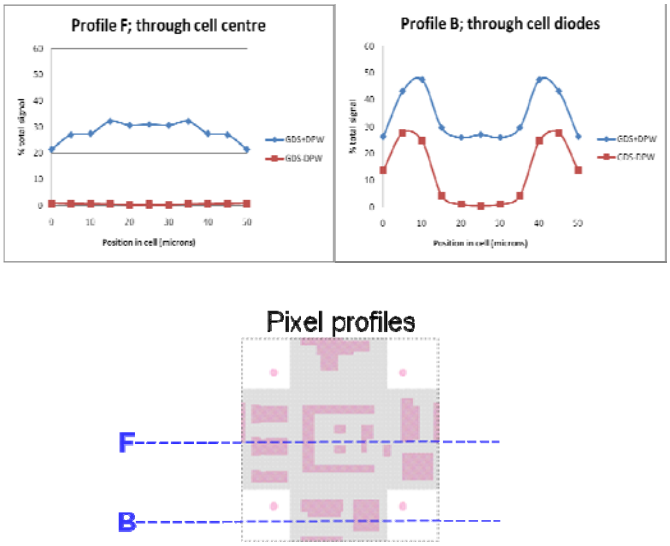

Figure 8: Simulated charge collection for particle hits in two linear profiles through a pixel (as illustrated).

The simulation results show clearly the benefits brought by the deep p-well, and the poor performance we might expect without deep p-well. Profile F that passes through the centre of the pixel collects very little charge without deep p-well, since it is mostly absorbed by the pixel electronics before it can reach a diode; the protection of the deep p-well layer is clearly demonstrated since the charge is allowed to reach the diodes. Profile B passing near a diode shows similar performance regardless of deep p-well, but again, charge deposited near pixel electronics can only reach the diode when the deep p-well is implemented.

In order to fully evaluate the performance of the new deep p-well implant the TPAC1.0 sensor was manufactured both with and without the additional processing step.

IV. Sensor Testing

Sensor test results are organised as those for the separate additional test pixels, single pixels in the main array and the performance of the pixel array as a whole. Test results for the arrays are presented for the preShape pixel variant only, since this was seen to perform more favourably than the preSample variant. The two variants of the preShape pixel are identified as quadrants 0 and 1. The test pixels implemented were only of the preSample variant; hence the details of those pixel circuits are an important part of this script.

A. *preSample Test Pixels*

Several test pixels are included at the edge of the main pixel array for detailed testing. These pixels are based on the preSample pixel architecture, and include additional analog buffers to monitor internal analog signals in the pixel circuit. The signal pulse and the reset sample are available for two adjacent pixels, and the internal differential comparator output is available from one test pixel. A third pixel allows evaluation of other in-pixel circuits.

Test pixels were evaluated with a 1064nm laser, pulsed at 25Hz in bursts of 4ns. The laser is mounted in a microscope with adjustable shutters to realise a 2x2um^2 area of illumination at the focal point. The sensor is illuminated from the rear, to avoid signal attenuation due to the many levels of metal routing in the pixel; the absorption length of silicon at this wavelength is long, so attenuation in this method is negligible. The focus of the laser was adjusted to target the epitaxial layer, accounting for the refraction of the laser light at the interface between air and the silicon. The sensor is mounted on an X-Y stage which can be remotely positioned to 1micron accuracy. Thus it is possible to deposit point-like charge at any location in the test pixel, and observe the analog response of the pixel on an oscilloscope.

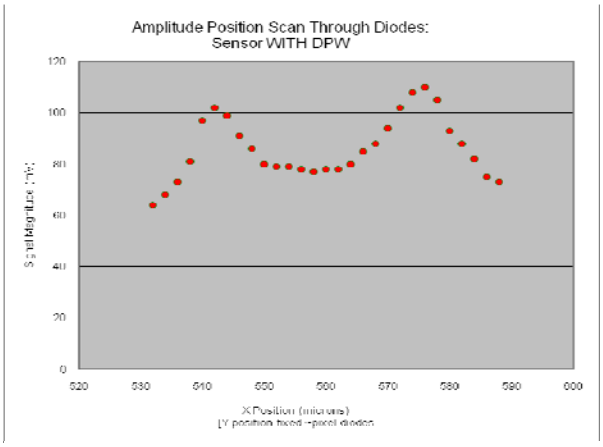

Figure 9: Amplitude response of preSample test pixel to laser stimulus: horizontal line profile intersecting two diodes.

The test pixel and the laser operate independently, with no synchronisation, but there is a laser control pulse that can be used to trigger an oscilloscope. The asynchronous pixel reset occasionally occurs during a laser event, but histogramming features on the oscilloscope eliminate susceptibility to this rare event. Signal magnitude and time-delay parameters can be recorded for each position, in an automated sequence. A typical amplitude response for a profile passing through two diodes in the test pixel is shown in Figure 9: The diodes are clearly identified in the scan, at the expected 34 micron separation.

Charge collection time is measured on the oscilloscope using the delay from the laser control pulse and a fixed 30mV threshold on the signal output from the target test pixel. This is compared with simulated results in Figure 10: where the time taken to collect 90% of the total charge is recorded. The profile between two diodes is presented on the same axis for simulation and measured results. There is a fixed-time delay from the laser control pulse to the emission of the laser pulse, but there is good correlation in the charge collection profile

between the two diodes, from which we can attain a reasonable degree of confidence in the device simulations. Automated scans of all positions in and around the test pixels are underway to further compare the device simulations with real behaviour of charge diffusing in the substrate, in sensors both with and without the deep p-well processing.

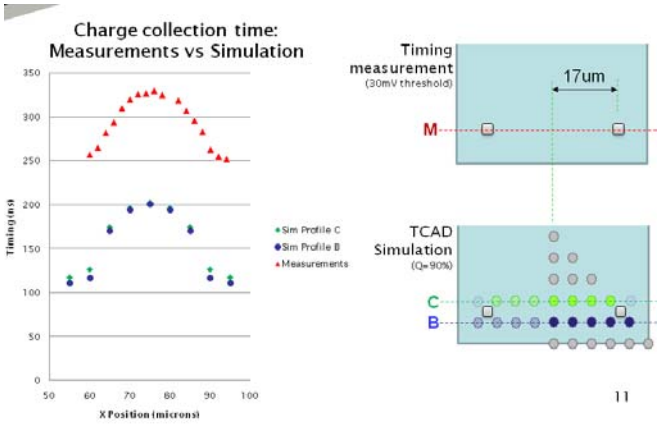

Figure 10: Comparison of measured charge collection time with device simulation results.

B. *Single preShape Pixel in Array*

Evaluation of a single pixel in the main array is achieved by setting the mask bit in every other pixel, thus leaving only a single pixel operational. Analog information is no longer available, since the pixel readout is binary, and stored in local SRAM. The method of evaluation of such pixels is therefore by threshold scan: The number of hits reported by the sensor is recorded for a wide range of thresholds. The resulting profile (see Figure 11:) can be used to determine the noise of the pixel, offset and signal response, by taking a number of bunch-trains for each threshold setting. The parameters of such runs can be adjusted for greater precision or faster scan time as required.

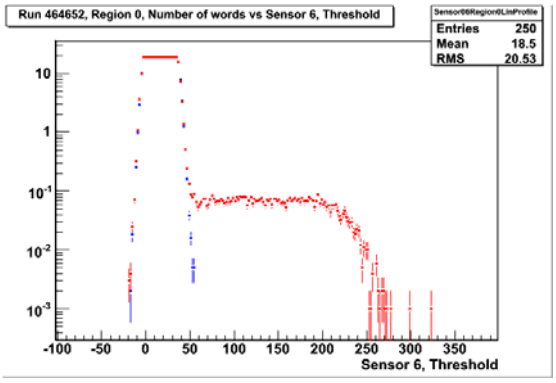

Figure 11: Two typical threshold scan results: (red) with laser source and (blue) without.

The example plot in Figure 11: shows two overlaid threshold scans; the blue response shows a single pixel with no stimulus, effectively showing the electronic circuit noise. For high thresholds, the noise is negligible, and no hits are recorded; for low thresholds the noise triggers the in-pixel comparator and hits are recorded; for very low thresholds, because the comparator is effectively edge-triggered, the comparator does not fire, hence the profile drops for small/negative thresholds. The total number of hits that may be recorded for a single pixel is 19, hence the profile of the pixel noise is capped at this level. The red response shows a typical profile with pixel stimulus, in this case a pulsed laser: The electronic noise generates a similar profile of hits, but the injected signal now generates additional hits for thresholds much higher than the electronic noise, up to the magnitude of the signal, beyond which there are again no further hits recorded. The signal magnitude may thus be estimated from the "roll-off" of this threshold scan. The accuracy of this technique is limited by the statistics of the threshold scan (which can take some considerable time) and the quality of the curve-fitting algorithm applied to the signal "roll-off" response.

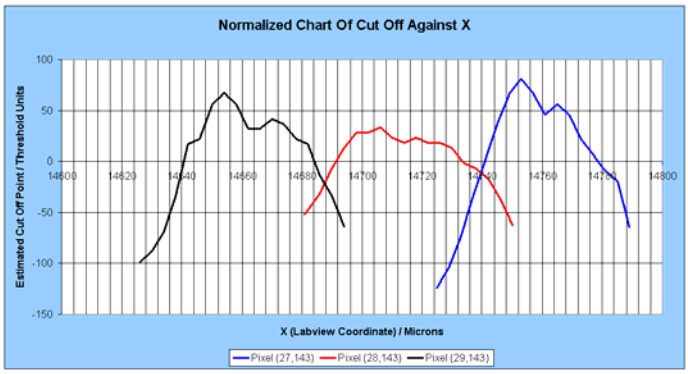

Figure 12: Normalised signal magnitude plots for three adjacent pixels, as used to identify exact location and orientation of sensor when illuminated from the rear surface.

An estimation of absolute position is possible using the threshold-scan technique: Rear illumination of the sensor offers no clues as to position, which may not be square to the x/y stage, but laser scans in the test pixels indicate that local maximum should be found scanning through the centre of pixels, or twin-peaks should be seen in scans. Such a scan of pixel centre axes is shown in Figure 12: which shows the response of three adjacent pixels in normalised units. The 50 micron pixel boundary can be easily deduced from these results. This technique is used near the corners of the sensor to establish the alignment of the sensor in the laser system, so that a correction factor can be calculated and applied to any X or Y movement request where comparisons are to be made.

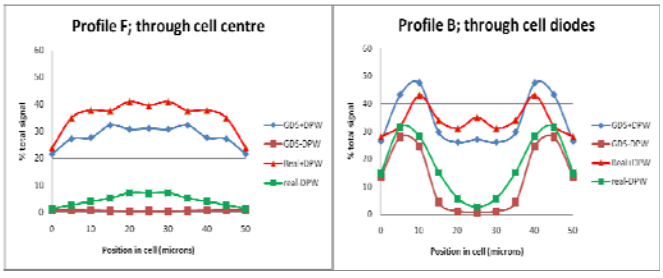

Figure 13: Comparison of simulation results ("GDS") with measured ("real") response of single preShape pixel in array for two linear profiles through the pixel.

A further comparison with simulation results can now be made, by testing the pixel response to charge deposited in all areas of the pixel. Figure 13: shows the same simulation data from Figure 8:, but now with added results from laser induced signals, normalised to the maximum signal size. The

qualitative similarity between simulation and measurements is clear, indicating the predicted benefits of the deep p-well implant are true in the manufactured devices. Similarly, the results from the non- deep p-well sensor clearly show the poor performance we would have achieved if the deep p-well module had not been developed.

The pixel array was also exposed to a strong ^{55}Fe source for a number of days, during which time several pixels were unmasked and threshold scans performed. ^{55}Fe is a key calibration technique, since the emitted 5.9keV X-rays will result in a well defined charge deposit of 1600e- at a point, which will sometimes occur in the diode well where no charge can diffuse. Typical results are shown in Figure 14: The signal roll-off will occur at the peak signal, which is more easily found by taking a derivative, where the small peak (shown) corresponds to the peak ^{55}Fe signal. This technique is used to calibrate the pixel electronics and the "threshold units" relative scale that is generally used.

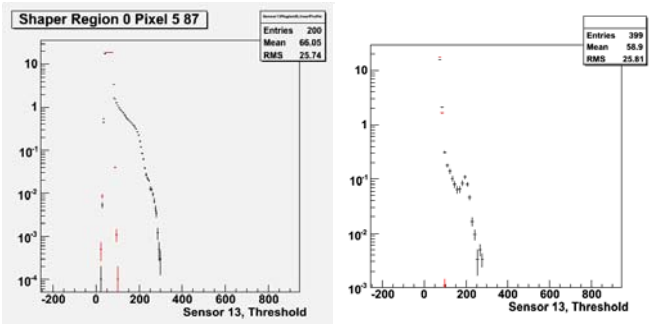

Figure 14: Single pixel ^{55}Fe result: Standard threshold scan (with/without source) shown on the left; Derivative is shown on the right, demonstrating ^{55}Fe peak.

C. *preShape Pixel Array Performance*

Evaluation of the full array of preShape pixels begins by evaluating each individually for noise. Only a single pixel is unmasked in any row and a threshold scan performed. By systematically changing the mask for subsequent runs, a scan over all pixels of the sensor can be built up. The pedestal, or x axis offset from one pixel to the next is large and variable, which is illustrated in the histogram of Figure 15:(left), where the mean value of the noise histogram from all 14,112 preShape pixels is plotted for both pixel variants. This per-pixel data is used to calculate the per-pixel trim adjustment. The trim adjustment is loaded into the in-pixel configuration registers and the per-pixel scan repeated. The correct operation of the trim adjustment can be seen in the histogram in Figure 15:(right).

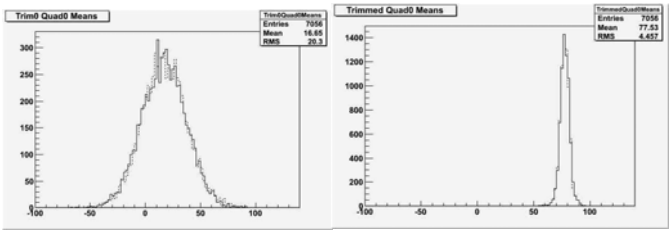

Figure 15: Histogram of per-pixel threshold scan mean values for quad 0 (solid) and quad 1 (dashed) preShape array pixels. Left shows before trimming, right shows after trimming.

An evaluation of pixel gain uniformity is possible using the laser source, now that absolute position and pixel pedestals are known. Approximately 250 pixels are hit with the laser in an equivalent position, and their signal magnitude evaluated by the threshold-scan/fit technique. The pedestal-adjusted gain uniformity is shown in Figure 16: for both variants of the preShape pixel. The pixel gain is uniform to 12%, and quadrant 1 shows preferable mean gain and signal-to-noise performance over quadrant 0.

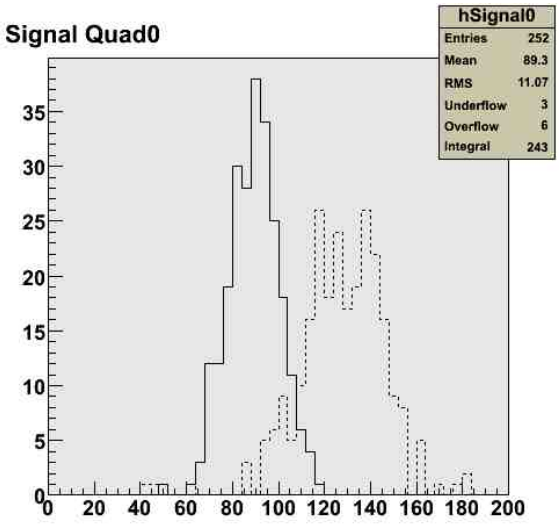

Figure 16: preShape pixel gain uniformity: histograms shown for quad 0 (solid) and quad 1 (dashed).

V. Future Outlook

Full characterisation of the TPAC1.0 sensor will conclude in the coming months, involving automated laser scans over test pixel regions, and characterisation of many pixels in the main arrays. A stack of 4 sensors will also be used to look for cosmic rays over a long period.

A new sensor, TPAC1.1 has been designed and is due back from manufacture at the end of September 2008. The new sensor selects a single pixel variant, (preShape quadrant 1) and is thus a homogenous pixel array. The in-pixel trim adjustment was upgraded from 4 bits to 6 bits to ensure pixels can be "aligned" to greater accuracy than the pixel noise. Test pixels of the preShape variant are included in TPAC1.1 in order to further learn more about the internal workings of these pixels. Beyond these and some minor changes, the sensor is very similar to TPAC1.0, and as such is I/O, PCB and DAQ compatible. This will enable immediate verification of the revised sensor with a known working test system. The full portfolio of characterisation summarised in this script will be repeated for the new sensors. The homogenous pixel array make this sensor ideal for beam tests, which are anticipated in early 2009: Four sensors will be mounted in a stack, with a number of tungsten plates and scintillators to prove the sensors in a demonstration ECAL environment with particle showers.

VI. Conclusions

We have successfully designed, built and demonstrated operation of a highly complex pixellated sensor for an ECAL at the ILC. The pixels have been shown to respond to input stimulus from ^{55}Fe and infrared laser, which studies have shown to correspond to device simulations.

We have successfully developed, implemented and verified a deep p-well implant on a standard 0.18micron CMOS process, to improve the charge collection efficiency of a MAPS detector with in-pixel electronics. The inclusion of such a layer is seen to be essential to the success of the design.

A revised sensor is imminently due back from fabrication, where a single pixel architecture was selected from the characterisation work presented herein. Testing of this new sensor will begin immediately on its return, thanks to complete compatibility with existing test systems. The new sensor has a homogenous array of pixels, and so it well suited to the intended beam test in early 2009, where it is hoped to demonstrate ECAL operation in a real particle beam, using tungsten to generate showers in the 4 layers.

In the long term this collaboration hopes to build larger scale sensors from these pixels and their associated circuits to demonstrate digital calorimetry with a stack of multiple sensor/tungsten layers in a particle beam environment.

VII. References

[1] LDC Detector Outline Document, http://www.ilcldc.org/documents/dod/outline.pdf

[2] SiD Detector Outline Document, http://hep.uchicago.edu/~oreglia/siddod.pdf

[3] J.A. Ballin et al., "A MAPS-based digital electromagnetic calorimeter for the ILC", proceedings for LCWS07 (2007) arXiv:0709.1346 [physics.ins-det]

[4] M.Stanitzki et al, “A Tera-Pixel Calorimeter for the ILC” in Proceedings for IEEE NSS 2007

[5] R. Turchetta, "CMOS Sensors for the detection of Minimum Ionising Particles", in Proceedings of the 2001 IEEE Workshop on Charge-Coupled Devices and Image Sensors, Lake Tahoe, Nevada, USA, 7-9 June 2001, 180-183

[6] P. Allport et al, “CMOS Sensors for High Energy Physics”, Extended programme of the 2005 IEEE Workshop on CCD and Advanced Image Sensors, Nagano, Japan

[7] E.R. Fossum, “CMOS image sensors: Electronic Camera-On-A-Chip”, IEEE Trans. Electron Devices, vol 44, no.10 pp. 1689-1698, Oct 1997

[8] R.Turchetta et al, “Monolithic Active Pixel Sensors (MAPS) in a quadruple well technology for nearly 100% fill factor and full CMOS pixels”, Sensors Journal Special Issue: Integrated High-performance Imagers.