Design of an integrated particle detector-cell based on latchup effect

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Abstract

The paper describes an innovative idea for a silicon pixel detector. The principle is based on latchup effect that is common in to-date CMOS technologies working in a radiation environment. A prototype was constructed in the past with commercial components and here is described in detail an integrated version of the design. In principle the detector has low triggering and dead time, can operate at room temperature, does not require a high voltage power supply and is intrinsically tolerant to radiation. As a latchup-based detector can be constructed using state-of-the-art CMOS technologies, here it is presented a design of a prototype that will be implemented on a commercial 0.35 μm Bi-CMOS technology and tested at Electronics Department of Torino Politecnico.

I. INTRODUCTION

Single Event Effects (SEEs) are caused by the charge deposited by a particle with over-threshold energy within microelectronics devices. Due to a potential permanent hazard in CMOS devices, one of the main SEEs is the well-known Single Event Latchup, SEL [1]. The latchup effect is based upon injected charges within microelectronics devices, whatever their origin. The only general requirement for a striking particle to ignite SEL in a given device is the minimum value of the deposited charge along its path. Following latchup ignition, the sensitive cell retains the position of the crossing particle by means of a self-locking thyristor. This provides a noiseless, digital, robust and stable signal until the whole system has been powered off. In CMOS devices the stimulated ignition of latchup effects caused by external radiation has so far proven to be a hidden hazard; however here it is proposed as a powerful means of achieving the precise detection and positioning of a broad range of particles.

II. THE LATCHUP EFFECT

Latchup is the ignition of a pn-pn or np-np parasitic structure created in conventional CMOS technologies. Fig. 1 shows a pn-pn structure on a p-type substrate silicon formed by two parasitic pnp (Q_1) and npn (Q_2) bipolar transistors. The transistors are locked together in a thyristor-like positive feedback loop. R_S and R_W stand for the substrate and well distributed resistors respectively. A series resistor R_L is also located between the OUT contact and VDD in order to limit the current produced by latchup ignition. R_L induces a reasonable output voltage drop at the OUT pin, which can be easily read. Otherwise voltage is at VDD level when the thyristor is off.

The latchup effect [2] involves several steps [3], [4]. First, the small transient well (substrate) current must be sufficiently high to forward bias the Q_1 (Q_2) base-emitter junction. This requires a sufficient drop in voltage in the well (substrate) distributed resistor R_W (R_S). Second, the amplified current from Q_1 (Q_2) must be high enough to turn on Q_2 (Q_1) by forward biasing its base-emitter junction via the substrate (well) current. This current may lead to a significant voltage drop in the substrate (well) distributed resistor R_S (R_W). Then the Q_2 (Q_1) transistor can turn on to allow the current flowing in the well (substrate) to keep forward-bias conditions on the Q_1 (Q_2) transistor until the whole thyristor reaches a standing latched state. Q_1 may then lead Q_2 to saturate or, similarly, vice-versa, as long as the product of the current gains of the two transistors is greater than 1. The latchup condition must not only be sustained but also controlled within the substrate
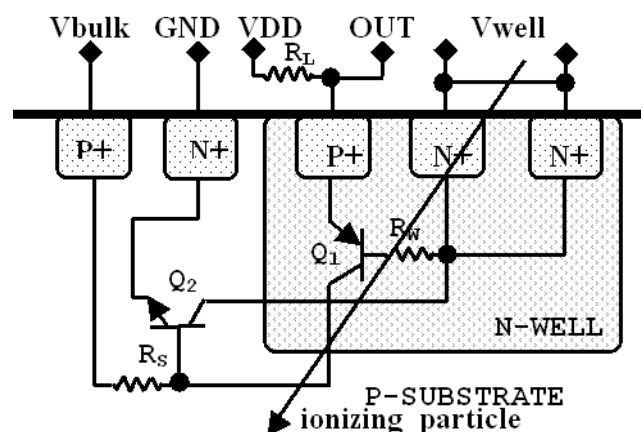

Figure 1: cross-section layout of a p-substrate cell

and well regions for a minimum amount of time to allow the detector readout process to take place [5], [6]. The cell proposed as the sensitive element in a latchup-based detector should be sized small enough to have a reasonable spatial resolution as a detector element for use in physics experiments [7].

III. PROTOTYPE

Previous investigations indicate that the recognizable charge might be comparable to that collected into to-date detectors. In fact, a prototype made up of discrete components was designed, constructed and exploited and the tests with daylight, electrons, via a current pulse generator and with a laser beam showed a charge sensitivity of the order of 1 pC [8-9]. It is expected to scale the charge sensitivity with an integrated version of the prototype. This is the reason why a new prototype is under design via a commercial AMS 0.35μm BiCMOS technology. Moreover, here a mixed-mode Bipolar-MOS circuit is designed and it is going to be submitted. The circuit is basically composed of a p-channel bipolar and a n-channel MOS transistors, plus some biasing resistors. In addition, the resistors are made via resistive polysilicon provided by the technology. The choice of the transistors are based upon the technology features and models. The two circuits shown in Fig. 1 and 2 differ because the Q_1 transistor is a planar PMOS in Fig. 1 while it is a vertical bipolar PNP in Fig. 2. The principle remains the same as the two transistors are locked in the same positive feedbacak loop. The charge here is collected in the base-emitter region of the bipolar and in the gate area of the NMOS transistor. For this reason, in principle, a thick detector is not required. As the bipolar transistor will be fabricated vertically while the NMOS is planar, it is expected that the two transistors retain also a different sensitivity due to the different technology
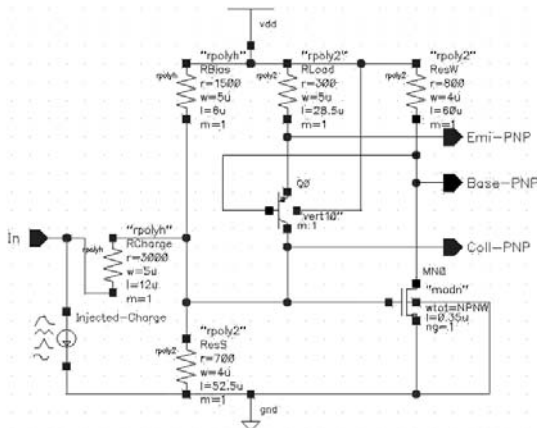

Figure 2 mixed-mode Bipolar-MOS circuit

implementations. The BJT might be mainly sensitive to deep charge despite the planar NMOS that might be ignited via surface injected charge. The combination of the two transistor could provide a balanced sensitivity of the entire cell.

IV. SIMULATIONS

The circuit shown in Fig. 2 has been Monte Carlo simulated, and other investigations are ongoing, to choose the best parameters in term of cell pre-bias and polysilicon layers used for resistors. These choices will manly affect the final layout.

Table 1 - Design parameters of Fig. 2		
Parameter	Sweep	Geometry
Resistor Rs	700 Ω	4×52 μm layer 2-poly
Resistor RL	250÷350 Ω	5×28 μm layer 2-poly
Resistor RW	800 Ω	4×60 μm layer 2-poly
Resistor RBias	1.4÷1.6 kΩ	5×6 μm layer h-poly
VDD	3.3 V	
Resistor RCharge	3.0 kΩ	5×12 μm layer h-poly
Input Charge	150÷350 fC	

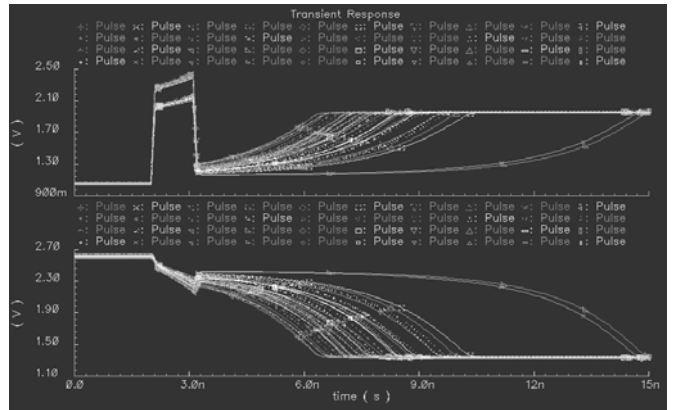Table 1 summarizes the parameters used to simulate the cell

Figure 3 Monte Carlo simulation

and Fig. 3 shows one of the main representative Monte Carlo simulations. The above curve in the figure is the injected stimulus and the below plot is the output port Base-PNP that saturates towards ground when the cell ignites. The circuit has been stimulated via a charge pulse of the order of a fraction of pC, i.e., a current of some μA that flows for some ns on a given resistor. Thus, the injected charge, by passing through the biasing resistors, provides the cell with the required extra biasing voltage drop to start ignition. The output spread accounts for the technology mismatches of the fabrication process. In ay case, the circuit works even though with different ignition speeds, from 3 to 12 ns after the stimulus. The simulations have not been stressed till he highest sensitivity of the cell as they have been carried out to get a quite-balanced circuit to test with different stimuli to get inspirations for new prototypes.

V. CONCLUSION

In principle an integrated version of a latchup-based detector could be interesting in terms of spatial resolution, triggering and dead time. Plus, it requires neither a high voltage power nor a biasing current. In addition, cell power consumption is negligible when the thyristor is off and the cell also works at room temperature. Moreover, it might be intrinsically radiation tolerant since the prototype can be fabricated with

state-of-the art, low resistivity technologies. Out signal does not require charge/current amplifiers and analog-to-digital converters normally embedded in front-end modules; the latchup-based detector's out signal is self-noiseless, digital, robust and stable.

According to the features described above the application fields may range from beam monitors to heavy ion selectors. Of course, the latchup susceptibility of the proposed cell needs to be in depth confirmed, investigated and finely tuned.

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