A CMOS 130nm Evaluation Digitizer Chip for Silicon Strips Readout

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Abstract

A CMOS 130nm evaluation chip intended to read Silicon strip detectors at the ILC has been designed and successfully tested. Optimized for a detector capacitance of 10 pF, it includes four channels of charge integration, pulse shaping, a 16-deep analogue sampler triggered on input analogue sums, and parallel analogue to digital conversion. Tests results of the full chain are reported, demonstrating the behaviour and performance of the full sampling process and analogue to digital conversion. Each channel dissipates less than one milli-Watt static power.

I. INTRODUCTION

The constraints in terms of room, power, transparency to radiation at the International Linear Collider (ILC) or even more at the Large Hadron Collider upgrades (LHC, CERN Geneva) dictate the use of Deep Sub-Micron CMOS technologies, in order to implement efficiently Front-end electronics able to process and digitize millions of channels, as it will be the case for Silicon strips detectors [1]. Deep-Submicron CMOS technologies down to 90nm are available through worldwide Multiproject Wafer Centers (MPW), such as Europractice at IMEC, Leuven, Belgium.

A. Detector and readout parameters

The Silicon strip detectors envisaged at the ILC are 1-60cm long, 100-300 micrometer thick, and have a 50 micrometer pitch. Therefore, a total channel capacitance between 1 and 100 pF has to be foreseen for the readout electronics. This capacitance dictates the noise performance, for a given shaping time. The ILC machine will produce trains of 3000 or 6000 bunches time spaced by 150 or 300 ns, and stay idle for 199 ms. Occupancy will be of a few per cents in the barrel region, up to 10 per cent in the forward regions. The cycle is therefore 5 Hz, with a data taking stage of 1 ms. During trains, data will be recorded in analogue pipe-lines, digitized and processed during the idle stage. Power cycling will switch DC supplies on at every train, off after digitization, for most of the idle stage.

B. Detector data

In order to achieve a few micrometers space resolution, analogue information has to be recorded channel by channel, in order to calculate centroids on-detector after digitization. A 10-bit precision is foreseen.

Each charge cluster has to be time-tagged in order to be able to identify the originating beam crossing without any ambiguity.

C. On-detector processing

During data taking, activity exceeding a given threshold on the analog sum of adjacent channels will be sampled at 10-20 MHz and stored in a 8-deep analogue pipe-line including pedestal, and digitized after the train in parallel for all channels with a 10-bit Wilkinson Analogue to Digital Converter. In case a strip is hit several times during a train, an event buffer can record 8 sets of samples, according to the detector occupancy. The analogue pipe-line has therefore two dimensions, one along time and the other for events.

As mentioned, digital signal processing in the front-end can perform some low level tasks such as centroids, least squares amplitude and time fits, lossless data compression, error correcting codes.

II. FRONT-END CHIP ARCHITECTURE

The final goal is therefore to integrate of the order of 1000 channels in 90nm CMOS including amplifiers with a 30mV/MIP voltage gain over 20-40 MIPs, pulse shaping between 500ns and 3µs, zero suppression, pulse sampling, event buffering, AD conversion, digital pre-processing, calibration and power switching.

Two 130nm chips have been designed, the first one being a full digitizing 4-channel version, the second one implementing some blocks required in the final chip, such as calibration, an improved version of the analogue pipe-line, a 10-bit digital to analog converter for the generation of internal reference, and some test active and passive components. The architecture of the 4-channel chip is depicted on Figure 1.

The motivations for going to 130nm CMOS technology were to achieve a lower material readout, faster at less power, and better radiation hardness performance (though this is not required at the ILC, but certainly for LHC). Moreover, this technology is presently dominant in the industry. Drawbacks are a reduced dynamic range due to smaller voltage supply range, gate/subthreshold leaks, a longer design time due to

more constraining design rules, and more complex models, sometimes not up to date, regarding the noise, in particular.

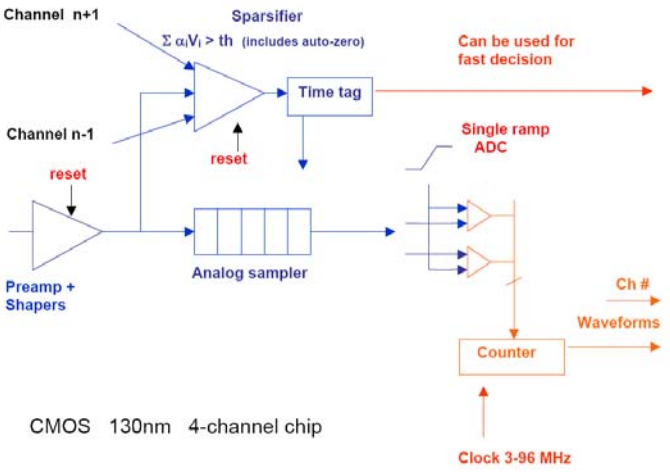

Figure 1: Foreseen front-end chip architecture

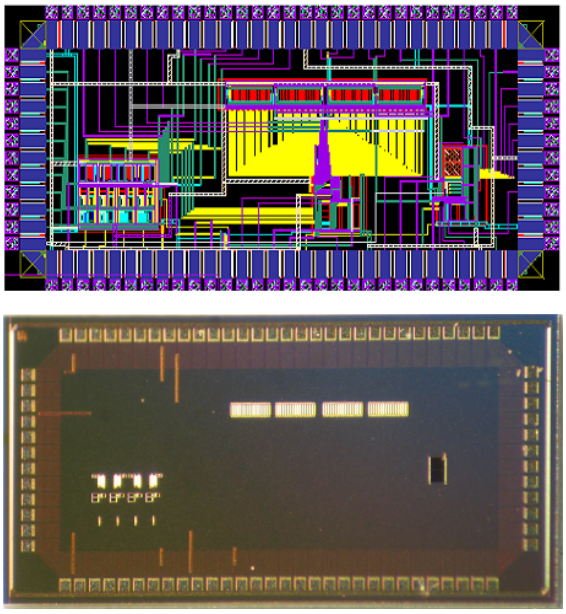

Figure 2: 4-channel 130nm CMOS chip

III. TARGETED NUMBERS

A charge gain of 30 mV/Minimum Ionizing Particle (MIP) was foreseen, noise performance of a previously designed chip in 180nm CMOS technology was measured at 375 + 10.5 e-/pF for a 3 µs shaping, at 210µW power, for the preamplifier and shaper. Process features in 180 and 130 nm are sketched in Table 1.

Table 1: 180 and 130 nm CMOS technologies from United Microelectronics Corporation (Taiwan, China)

Feature size/ Feature	180nm	130nm
3.3V transistors	Yes	Yes
Logic supply voltage	1.8V	1.2V
Metal layers	6 Al	8 Cu
MIM capacitors	1 fF/µm^2	1.5 fF/µm^2
Transistors	3 Vt options	3 Vt options + low leakage

IV. 4-CHANNEL FRONT-END CHIP DESIGN

A full chain including preamplifier, pulse shaper, sparsifier, analog-pipe-line and ADC was implemented in order to validate the technology under realistic conditions, using a radio-active source and under beam-tests. The layout and photo are shown Figure 2. An full analogue channel from preamplifier to sparsifier channel occupied 90 x 350µm^2, a 16-sample analogue pipe-line 250 x 100µm^2, the ADC 250 x 100 µm^2.

V. RESULTS

A. *Preamplifier and Shaper*

A gain of 29 was measured for the preamplifier fro 20 MIPs at 1% linearity, 30 MIP's at 5%. The shaper's peaking available time range was 0.8-2,5 µs (against 0.7-3µs anticipated), for a total power of 245 µW (preamp + shaper). The output of the preamplifier is shown Figure 3.

The linearities shown Figure 4 were obtained for the preamplifier and shaper.

The noise was measured at 625 + 9 electron/pF at 2 µs shaping time, and 850 + 14 electron/pF at 0.8 µs shaping time. These numbers are not far from the 180nm chip performance. A comparison is sketched Figure 5.

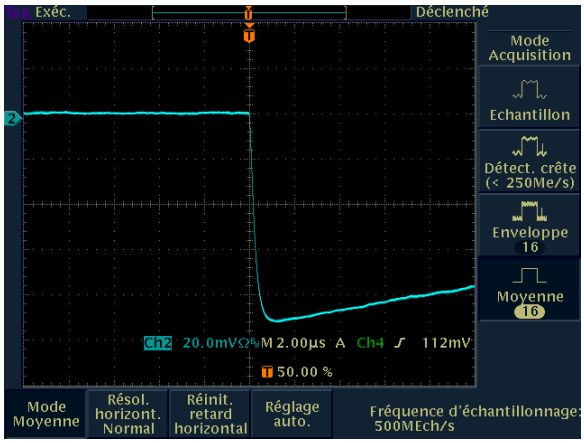

Figure 3: Preamplifier output

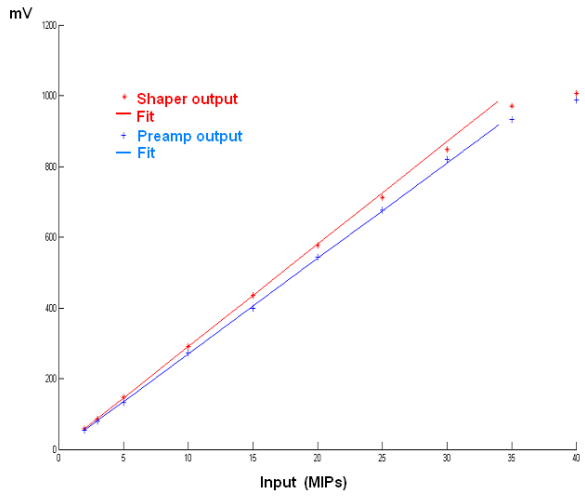

Figure 4: Preamplifier and shaper linearities

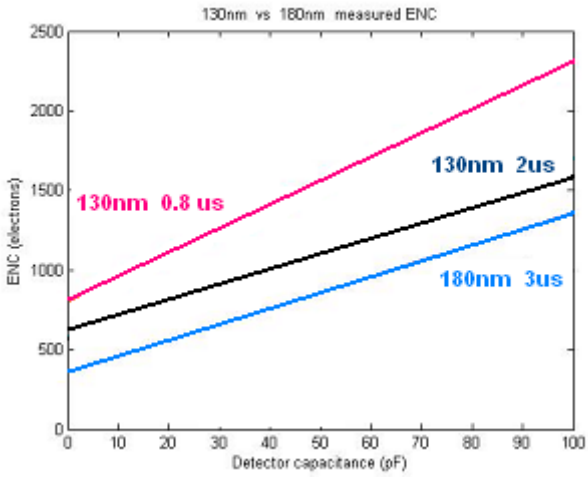

Figure 5: Noise in 180 and 130 nm CMOS technologies

B. *Analogue pipe-line*

The analogue pipe-line samples the output of the shaper. In the 4-channel chip, the pipe-line was implemented with 1 pF capacitances, multiplexed using analogue switches toward the ADC. Two channels were also connected to an output pad for diagnostics, the capacitance of this pad adding as a parasitic to the pipe-line introduced distortions on the observed channels, before and after analogue to digital conversion.

Analogue pipe-lines were designed at LAPP Annecy. On the second 130nm chip, an analogue buffer was inserted between the pipe-line and the ADC to allow using the analogue output. The digitized waveforms using either a pulse generator as a source, or a laser diode when the chip was connected to an actual Silicon detector, shown Figure 6, are quite similar, although their decay is slightly corrupted by the artifact mentionned previously. The chips were corrected using Focused Ion Beam technology, cutting the traces feeding the bonding pads, and the correct waveform was obtained.

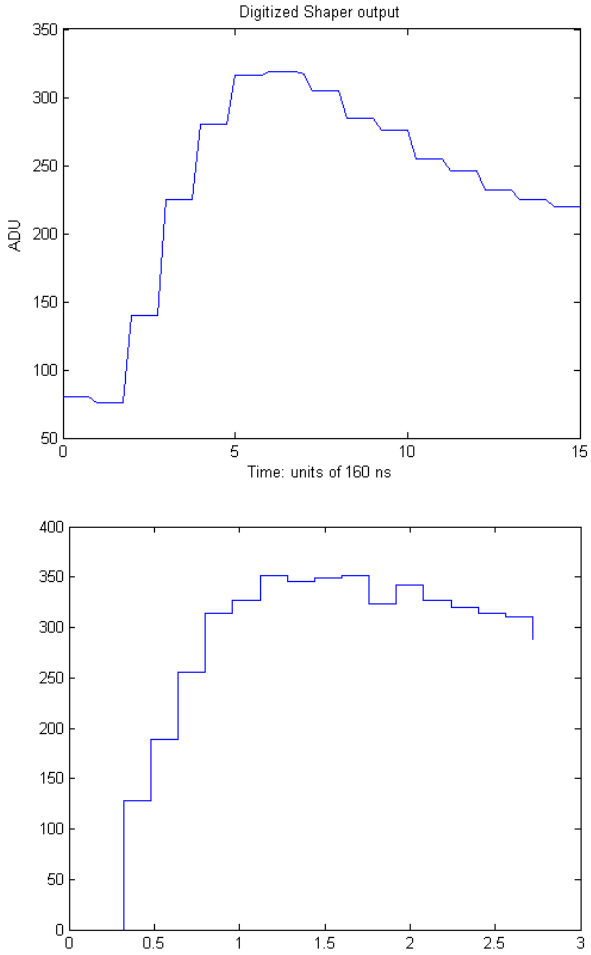

Figure 6 a and b : Digitized shaper waveform
6a: Electrical test (pulse generator)
6b: Laser diode + Silicon detector
Horizontal: units of 160ns, Vertical: 1 ADU = 500 µV

C. *Analogue to digital converter*

The most efficient ADC structure for the case of Silicon strip readout where the number of channels per chip is very large (above 256), is clearly the Wilkinson ADC (single ramp) since the only block that scales with the number of channels is the comparator. Therefore, power and Silicon area are minimized compared to other architectures.

The ADC is fully functional and presently under tests, preliminary results are presented Figure 7a and b. Noise shown on Figure 7b is interpreted as originated in the differential pair of the comparator. Noise RMS value calculated from these samples is found to be 1mV rms, to be compared to the LSB value of 250 µV. Power is 30mW per channel, for the chosen biasing point.

Some unexpected features such as gain differences between channel, that may be due either to channel to channel differences in the input calibration capacitance values (traces

on PCB), or damages to the chip due to the FIB process remain to be understood.

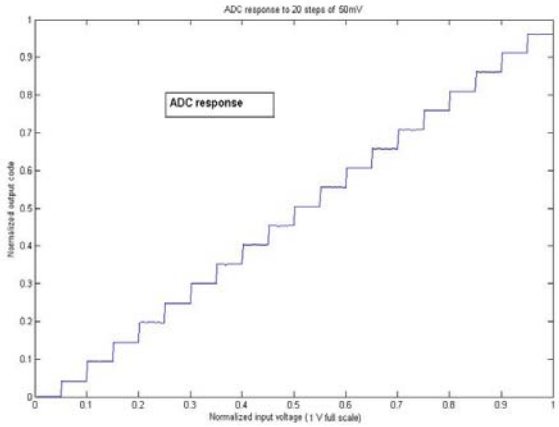

Figure 7a: ADC scan: 20 steps of 50 mV

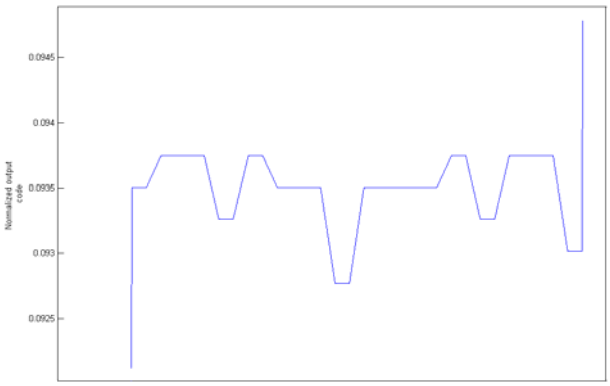

Figure 7b: Zoom on a step from Figure 7a: 16 samples from the same DC value.

D. Power cycling

Power cycling is of prime importance at the ILC since the duty cycle allows basically saving 99.5% of the DC power. A previous version of the chip in 180nm CMOS was pulsed, using the available current sources analog controls. The recovery from power-on delay was found of the order of one millisecond, due to external decoupling components and should be greatly reduced in the next chip since power cycling will be taken into account at the design time. The fraction of power used in sleep mode is under evaluation.

E. Overall performance

Figure 8 shows digitized calibration pulses peak values for a given channel. Linearity is within +3/-2 % on a 22 MIP input range.

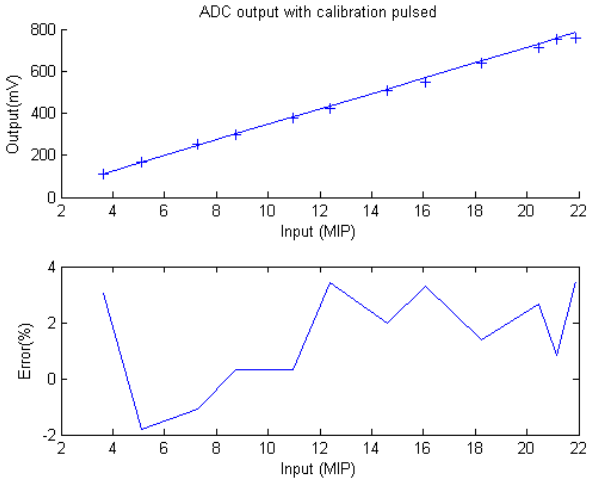

Figure 8: Digitized calibration pulses responses for a 1-22 MIP input range

VI. NEXT CHIP

After the two present chips will be fully understood and debugged after radio-active source and beam tests, all blocks will be merged to build a 128 channel version in 130nm CMOS including calibration and power cycling. Digital will be implemented using logic synthesis and merged with the analog blocks.

VII. CONCLUSION

Although some issues had to be faced with the 130nm technology, such as unaccurate noise modeling, transistors leakage stray currents, more constraining designn rules, it was possible to implement the two test chips in a reasonnable amount of time, thanks to the help of Erwin Deumens and Paul Malisse at Europractice-IMEC providing a very efficient interface to UMC. Measured performance mainly agree with the simulations, and most of the analog blocks have been validated for the next design.

These two 130nm CMOS designs and first test results demonstrate the feasibility of a highly integrated front-end for Silicon strips (or even large pixels) readout with DC power under 500 uW and Silicon area under 100x500 µ2 per channel

VIII. REFERENCE

[1] Same authors

Front-end Electronics for Silicon Trackers readout in Deep Sub-Micron Technology. The case of Silicon strips at the ILC

12th Workshop on Electronics for LHC and Future Experiments, Sept. 25-29th, 2006 Valencia, Spain.