The ALICE Silicon Pixel Detector System (SPD)

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Abstract

The ALICE silicon pixel detector (SPD) comprises the two innermost layers of the ALICE inner tracker system. The SPD includes 120 detector modules (half-staves) each consisting of 10 ALICE pixel chips bump bonded to two silicon sensors and one multi-chip read-out module. Each pixel chip contains 8192 active cells, so that the total number of pixel cells in the SPD is $\approx 10^7$. The on-detector read-out is based on a multi-chip-module containing 4 ASICs and an optical transceiver module. The constraints on material budget and detector module dimensions are very demanding.
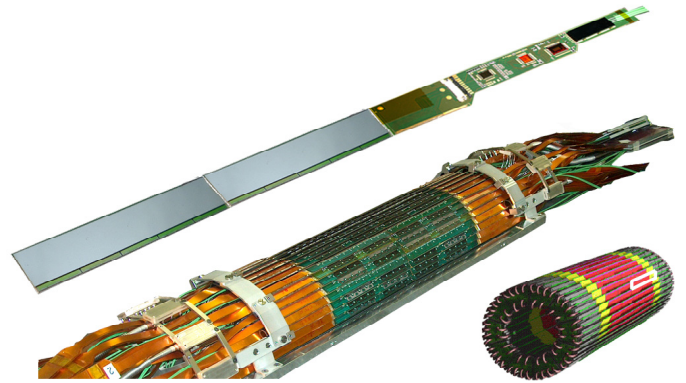
Figure 1: (from right to left) SPD artistic view, half barrel, half stave

I.   SPD LAYOUT AND PARAMETERS

The ALICE silicon pixel detector (SPD) consists of two barrel layers at radii of 3.9 cm and 7.6 cm, respectively and has an active length of 28.3 cm. The basic detector module is the half-stave, in which the sensitive elements are two silicon sensors bump-bonded to 5 read-out ASICs each, see fig. 1. A multi-layer aluminum flexible flat cable provides power to the pixel chips and connects signal lines to a multi-chip read-out module (MCM). Each pixel chip contains a matrix of 8192 cells. The SPD contains 9.83×10^6 pixel cells. A half-stave has the physical dimensions of 240 mm x 15 mm x 2 mm. Each layer of the SPD has a material budget of 1 % of radiation length X_0. The

distance of the half-staves in the inner layer to the ALICE beam pipe is 4 mm only.

The half-staves are mounted on 10 light-weight carbon fiber sectors, each sector supporting 4 half-staves on the inner layer and 8 half-staves on the outer layer, for a total of 120 half-staves and 1200 pixel read-out chips, see fig.1. The pseudorapidity coverage of the inner layer is $|\eta| < 1.95$. Table 1 summarizes the SPD system parameters.

The read-out is organized in 2 trigger levels, the ALICE L1 trigger signal after 6 μs upon which the hits are stored in multi-event buffers and the ALICE L2 trigger signal after 100 μs upon which data are read-out from the pixel chips and trans-

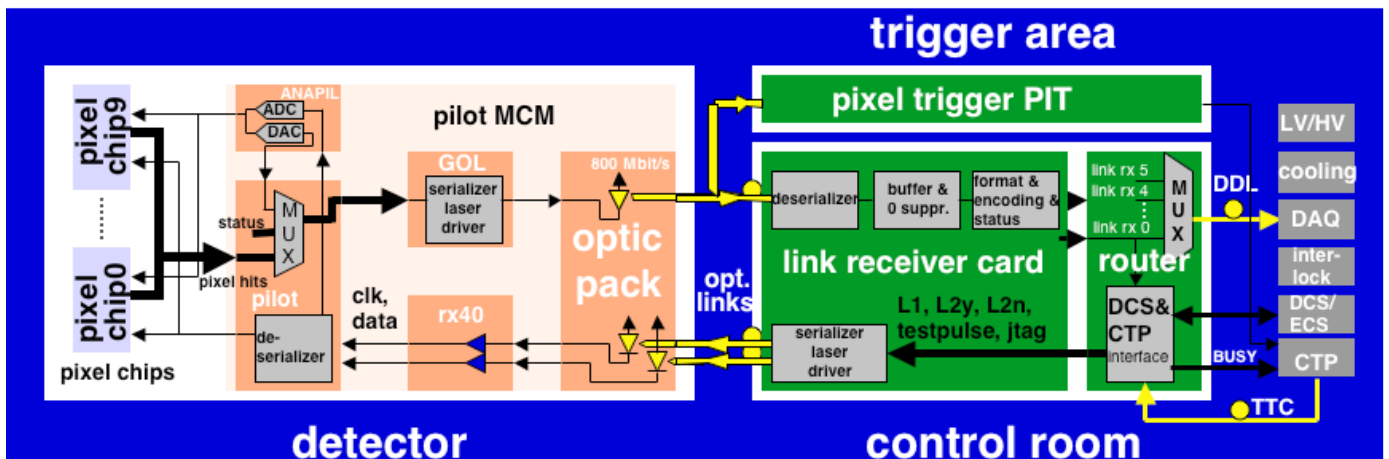Figure 2: SPD system block diagram

Table 1: System Parameters

Number of channels	$9.83 * 10^6$
Number of detector modules	120
Number of sectors	10
Number of trigger levels for read-out, ALICE L1 (6 μs), L2 (100 μs)	2
Read-out time	260 μs
Total dose in inner layer over 10 yrs	250 krad
Neutron flux in inner layer over 10 yrs	$3 \times 10^{12} cm^{-2}$
Material budget	1% X_0 per layer
Power dissipation	1.3 kW
Operating temperature	24 °C

ferred to the control room within 260 μs. The ALICE L0 signal is not used for the read-out. The total dose and the neutron flux as shown in the table are lower by 2 orders of magnitude compared to the CMS or ATLAS pixel detector values, but they are still too high for the application of industrial electronics. Thus, all ASICs have been developed in a 0.25 μm CMOS process radiation hardened and tolerant against single event upset by design techniques. Due to the low total dose levels the detector can be operated at room temperature [1].

II. SYSTEM ARCHITECTURE

Fig. 2 shows a block diagram of the SPD system. The VME and FPGA-based off-detector read-out electronics establishes the interface to the ALICE trigger, DAQ, DCS (detector control system) and ECS (experimental control system) [2]. It consists of 20 9U VME boards with three plug-in daughter cards each (router and link receivers [3]). The off-detector electronic transmits the trigger and configuration data on two optical fibers, one carrying the clock, the other serial data, to an on-detector multi-chip-module which forwards the information to the pixel chips and initiates the read-out sequence. It transmits read-out data via an 800 Mbit/s G-link compatible optical link to the off-detector electronics. There the data are zero-suppressed and re-formated before they are sent via the ALICE detector data link DDL [4] to the DAQ.
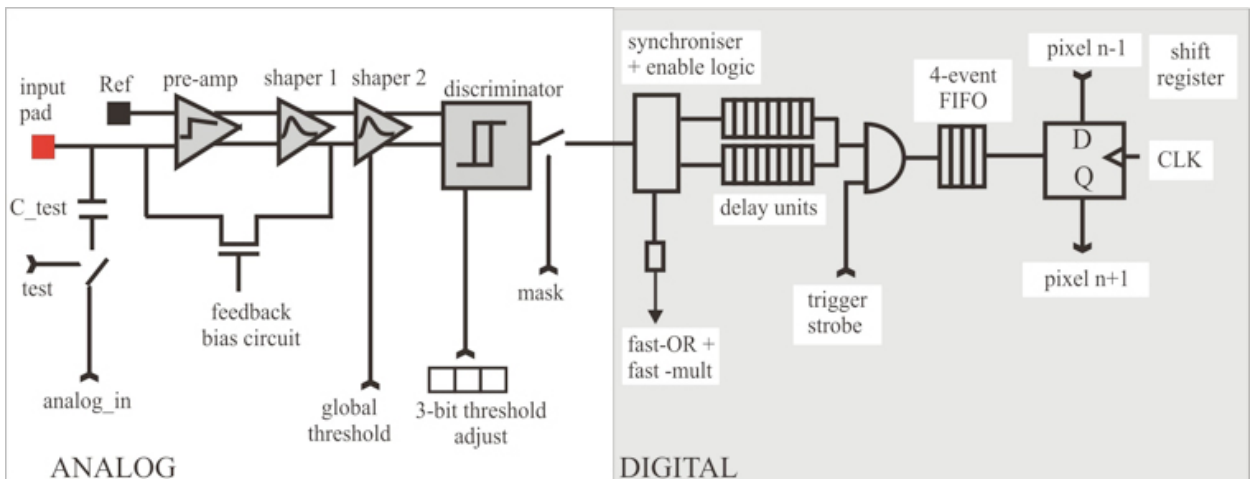
III. ON-DETECTOR ELECTRONICS

A. Pixel read-out chips and sensors

The pixel chip matrix consists of 8192 pixels organized in 256 rows times 32 columns. Each pixel has a size of 425 μm x 50 μm. The detector signal or a test pulse which can be enabled for each pixel individually is sent to a differential amplifier, shaper and discriminator. A global threshold is set for all pixels. A 3-bit register allows fine tuning of each discriminator threshold. In practical use of the SPD this fine tuning was found not to be required. Each pixel can be masked and removed from the read-out. All pixels are connected to a so called fastOr circuitry whose output is active if at least a programmable number of pixels have been hit. If this threshold is set to one pixel the output is active if at least one out of the 8192 pixels in one chip is active. The binary discriminator hit information, is stored in a programmable delay line during the L1 trigger latency. In case of a positive L1 decision the hit is stored in one out of four multi event buffers where the data wait for the L2 trigger decision to be read out via a 32-bit parallel data bus or are discarded. Fig. 3 shows a block diagram of the pixel chip.

One sensor assembly, the ladder, contains each 5 read-out chips with the dimensions of 13.68 mm x 15.58 mm connected by bump bonding to one p-in-n sensor element (72.72 mm x 13.92 mm). In total 40960 Pb-Sn bump bond connections with a 25 μm diameter and ~12 μm stand off are used for one ladder. In order to keep the material budget within 1% X_0 (each layer), the read-out chip and the sensors are 200 μm thick and the pixel chips are thinned down to 150 μm [5].

B. Multi-chip read-out module (MCM) and ASICs

In each half-stave one multi-chip module initiates the read-out and performs the configuration process of the pixel chips. The connection to the control room is established via three optical fibers. All on-detector ASICs have been implemented using a commercial 0.25 μm CMOS process; radiation hardness is obtained by appropriate gate design rules and by redundancy in the critical nodes. The 5 layer-MCM with the dimension 110 mm
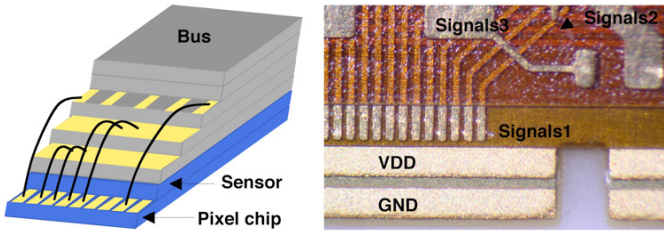

Figure 3: Pixel chip block diagram

Figure 4: Pixel bus

x 15 mm x 2 mm is made in a sequential build up (SBU) technology using polyimide (Kapton) as base material. The MCM contains four ASICs and a custom developed 800 Mbit/s optical link for the data transfer between the detector and the control room. The RX40 [6] converts the signal from the receiver PIN diodes to LVDS signals. The digital PILOT2003 [7] chip deserializes the incoming data and provides the configuration data in JTAG protocol to the pixel chips, controls the read-out procedure and forwards the data to the 800 Mbit/s G-link compatible serializer GOL [8]. The ANAPIL [7] chip provides analog bias voltages to the pixel read-out chips and measures detector temperature and supply voltages.

IV. ON-DETECTOR ELECTRONICS INTEGRATION

The compactness of the design sets severe constraints on the material budget and dimensions of the detector elements and the interconnects.

The very small clearance between the SPD inner layer and the wall of the beam pipe requires that the overall radial thickness of the half-staves is less than 3 mm. The width of the half-staves is determined by the pixel chip dimensions; the clearance between the edges of adjacent half-staves is down to ≈ 0.2 mm and the width of the MCM substrate is limited to 11 mm in order to avoid interference with the other structural elements.

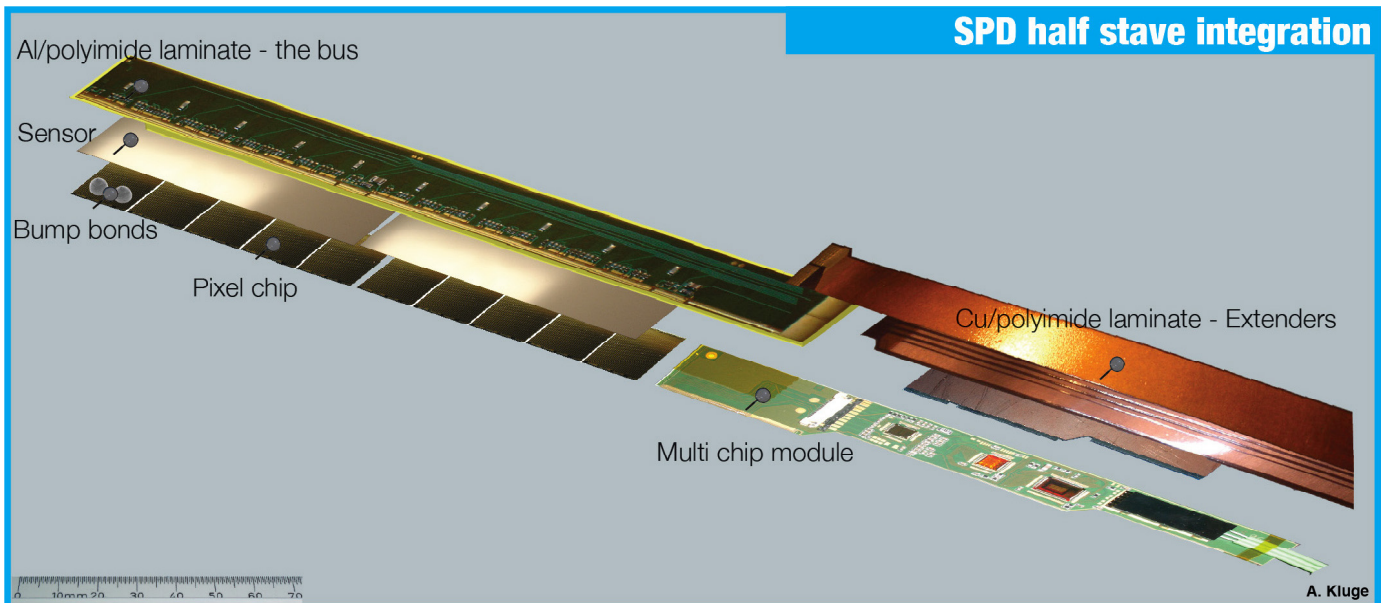Fig. 5 shows the components of a half-stave. The two lad-

ders with the 10 pixel chips bump bonded to two sensor elements and the MCM are placed onto a kapton grounding foil to isolate the half-stave from the carbon fiber support. The MCM is covered with a mechanical protection lid. The interconnections between the pixel chips and the read-out MCM is established via a multi-layer flexible flat cable (pixel bus) glued on top of the ladders and the MCM in which aluminium layers are used as conductor to even further reduce the material budget. Wire bonds from the pixel chip pads are connected to the bond pads of the bus. From there the signals are routed on the bus to the MCM. Then wire bonds connect the bus lines to the MCM. The pixel bus also provides supply voltages to the pixel chips. As the implementation of vias in aluminum is difficult vias are used for signal traces only. To access the ground and power planes for the wire bond connections each subsequent layer of the bus is made less wide by 0.5 mm. Fig. 4 illustrates this principle. The bus is 200 mm x 13 mm x 0.35 mm in dimension. It has two power planes and three signal planes with a thickness of 10 μm to 50 μm and a bond wire pitch of 150 μm.

V. OFF-DETECTOR ELECTRONICS

A. SPD read-out electronics

The SPD read-out electronics is located in the control room CR4 of ALICE. Twenty 9U VME based electronics cards, the routers, contain each 3 plug-in type daughter cards, the link receiver cards [3]. The link receiver cards are connected via optical fibers to two half-staves. The link receivers zero-suppress and re-format the hit data to an ALICE off-line analysis compatible format. The routers multiplex data from the six half-staves into one ALICE DDL and attach trigger and status information. Fig. 6 shows a photograph of the router board with three link receiver cards.

Each of the 20 router cards provides the interface to the trigger, DAQ and DCS/ECS for 6 half-staves. The trigger informa-
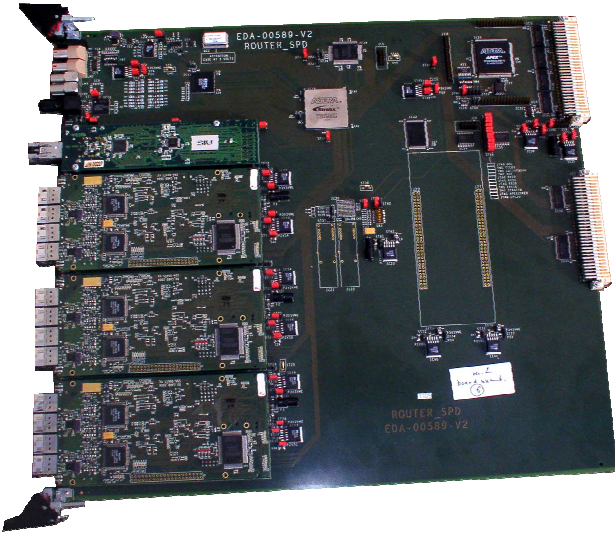

Figure 5: Half stave components

Figure 6: Router and plugged link receiver cards

tion arrives on fibers from the trigger, timing and control (TTC) system [9]. The interface from the routers to the DAQ is made via optical ALICE detector data links, DDLs, for each router one DDL. 4 PC-based local data concentrators, LDCs [2], receive the 20 DDLs. The data access from the DCS/ECS to the routers is established via the router VME ports. The same port also allows monitoring and copying the data flow during data taking.

B. L0 pixel trigger electronics

The SPD contributes to the generation of the ALICE first level trigger signal L0. Each of the 1200 pixel chips has a fastOr output indicating the presence of at least one hit in the matrix. These signals are sent from each half-stave to the trigger room in the ALICE cavern. There the pixel trigger processor (PIT) extracts the fastOr bits and forwards the output of the trigger algorithm to the L0 input of the ALICE central trigger processor CTP [10]. A 9U sized processor board, the BRAIN board, has been constructed to perform the trigger algorithm and to hold 5 plug-in type daughter cards on each side of the board. The 10 daughter cards receive 12 optical links each, extract the fastOr signals and forward them to the BRAIN processor. The system is capable to process 96 Gbit/s data from 120 800 Mbit/s links. For the generation, transmission, extraction and processing of the fastOr signal a latency of 850 ns is targeted. Fig. 7 shows the two cards [11].

VI. ELECTRONICS SIMULATION AND PRODUCTION TESTS

The full SPD system from the frontend-chips and the MCMs to the off-detector electronics has been simulated using a board level VERILOG simulation environment. This system simulation allowed the different hardware designers to elaborate the various components in the system directly during development. The simulation model also was used during the production tests of the electronics components. The MCMs, the pixel bus and the link receivers were connected to FPGA-based pattern gen-

erators loaded with the simulation models of the components which they are connected to in the SPD. For these tests the MCMs and the pixel bus were temporarily wire bonded to a test card. The link receiver cards were directly connected to the pattern generator. Router cards together with 6 link receiver cards were tested via JTAG-based boundary scan. The pixel chips individually and also after they were bump bonded to the sensor ladders were connected to a test station emulating the read-out system on a waver prober machine.

VII. MECHANICS AND SERVICES

A. Carbon fiber support and cooling

The SPD is divided in 10 sectors. 10 carbon fiber support carry four inner layer half-staves and eight outer layer half-staves. The half-staves are mounted in a turbo-like geometry to establish full geometrical coverage. In the sensitive area the wall thickness of the support is 200 μm.

Each of the half-staves consumes ~11 W i.e. 1300 W for the whole SPD. The cooling system is based on a fluor-carbon evaporative system using C_4F_{10} which allows the evaporation to take place at the foreseen operation temperature of 24 °C
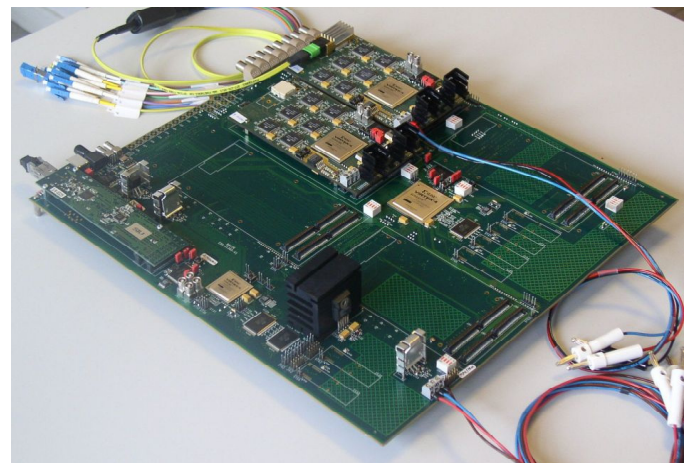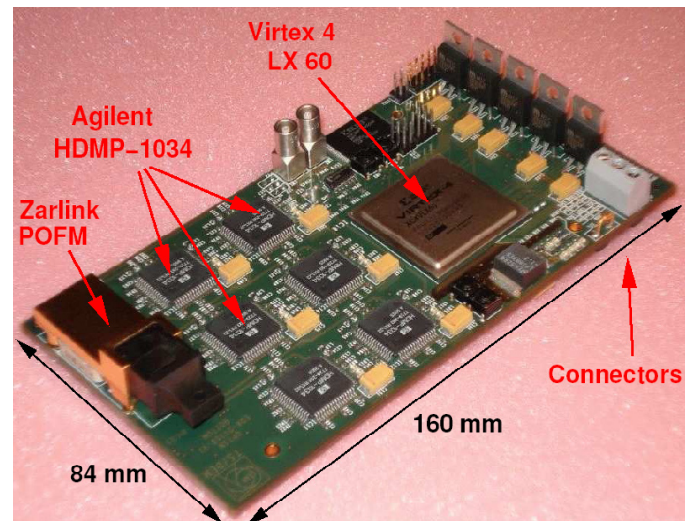

Figure 7: OPTIN (top) and BRAIN (bottom) cards

still leaving sufficient residual pressure for the recovery of the fluid along the 50 m return line from the detector to the cooling plant. The main design requirements are to minimize the material budget for both the fluid and the cooling duct, provide long term stability against corrosion, chemical compatibility (in case of fluid leakage) with both the carbon fiber support and the beryllium beam pipe, to minimize the temperature gradient along the half-stave, and to reduce the effects of the material temperature extension mismatch. Each half-stave is thermally connected to a cooling duct made of Phynox (alloy of Co, Cr, Ni, Mo) mounted in a groove on the carbon fiber support. The tube has a wall thickness of 40 μm and an initial diameter of 2.6 mm, squeezed down to an external thickness of 600 μm.

C. *Power supplies*

The pixel chips of one half-stave work with a voltage and current consumption of 1.8V/5.5A. The MCMs are powered with 2.6V/0.5A. The power supply system is based on the CAEN EASY 3000 series. The half-staves are connected to the differential sensing power supplies directly without local regulators via 40 m long cables. All power supply channels are electrically floating with respect to each other. The MCM ground and the pixel chip ground are connected to each other on the half-stave. The return paths of all half-staves are connected to a so called reference ground via a 10 kOhm resistor inside the power supply module. The reference ground is connected to a metallic structure in the ALICE experimental setup (front absorber).

D. *Detector safety temperature interlock*

Due to the light mass of the detector modules and its resulting and destructive temperature increase during a failure of the cooling system the power supplies must be switched off immediately. Two independent PT1000-based temperature sensor chains are placed on the pixel bus and the MCM. One is read out via the optical link. The off-detector electronics evaluates the temperature constantly and switches the power supply off either via software or via a hardware based interlock system in the routers. The other chain is connected by wire to a PLC-based system in the power supply racks which reads the hard-wired temperature sensors and directly acts on the power supply module.

VIII. FULL SYSTEM PRE-COMMISSION AND INSTALLATION

As access to the detector after installation in ALICE is not foreseen, full system laboratory tests of the entire detector system including the sensors, pixel read-out chips, the multi-chip module, the optical links, the off-detector electronics, the ALICE trigger system, the ALICE data acquisition system, the ALICE detector and experimental control system, full length low volage and high voltage cables and final power supplies have been performed. The SPD and the full read-out system has been installed in ALICE.

IX. SUMMARY

The tight material budget and the limitation in physical dimensions required by the detector design introduce new challenges for the integration of the on-detector electronics. The full system has been pre-commissioned in a clean room and installed in ALICE.

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