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LHCb Preshower Front-End Electronics Board. Qualification of the final prototype.

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Abstract

This note describes the tests performed on the final prototypes of the SPD/Preshower Front-End electronics boards.

1 Test Bench Description

The general setup of the test bench is presented in figure 1, where the main components are the backplane with the CROC and the *FEB*s under test, the analog (AWG) or digital (memory boards) stimuli and the master PC. We dispose of two backplanes, the standard LHCb backplane which allows to test in principle 16 different *FEB*s at the same time and a homemade backplane that can receive only a CROC and a *FEB*, but allows easier debugging by easy captures of the signal transiting the backplane and full *TRIG_PGA* tests by injection of all the trigger IOs.

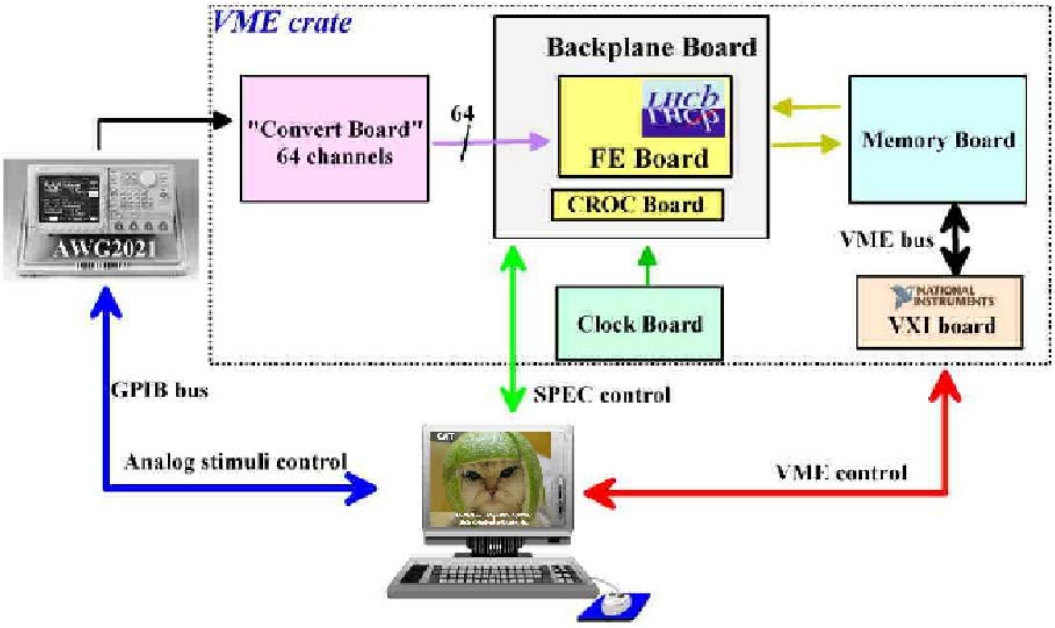

Figure 1: Experimental setup

2 Software Description

The software for the PS *FEB* control was developped in the CAT [1] frame. From the *GUI* point of view, there is first a graphical interface dedicated to the *FEB*, presented in figure 2, which allows a fast view, load and check of the main board parameters. Specially dedicated panels are available for each of the PGAs of the board which allow the tuning by hand of all the PGAs parameters, write/read accesses, monitoring of the different flags, fast access to the RAMs,

etc. The *FE_PGA* and the *TRIG_PGA* panels are presented in figures 3 and respectively 4.

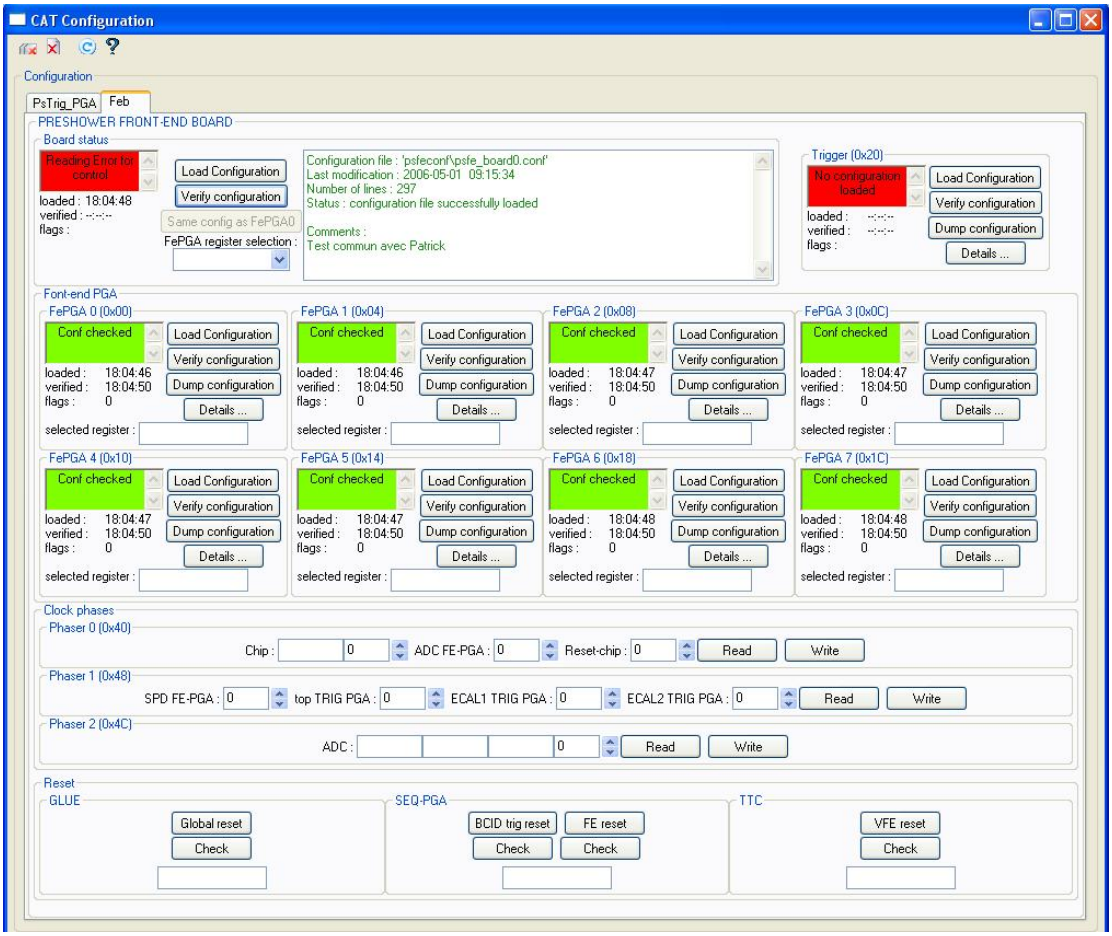

Figure 2: CAT Panel for the global configuration of the *FEB*.

For testing automatically the board and for time-consumming tests, CAT processes are defined, which can be run repeatedly either on individual components or on the full board.

3 Board stability with the ground clock frequency

By using an external clock generator, the *FEB* ground clock was varied. The functioning was normal up to 46 MHz for the full board and the *FE_PGA* was still working properly at 50 MHz.

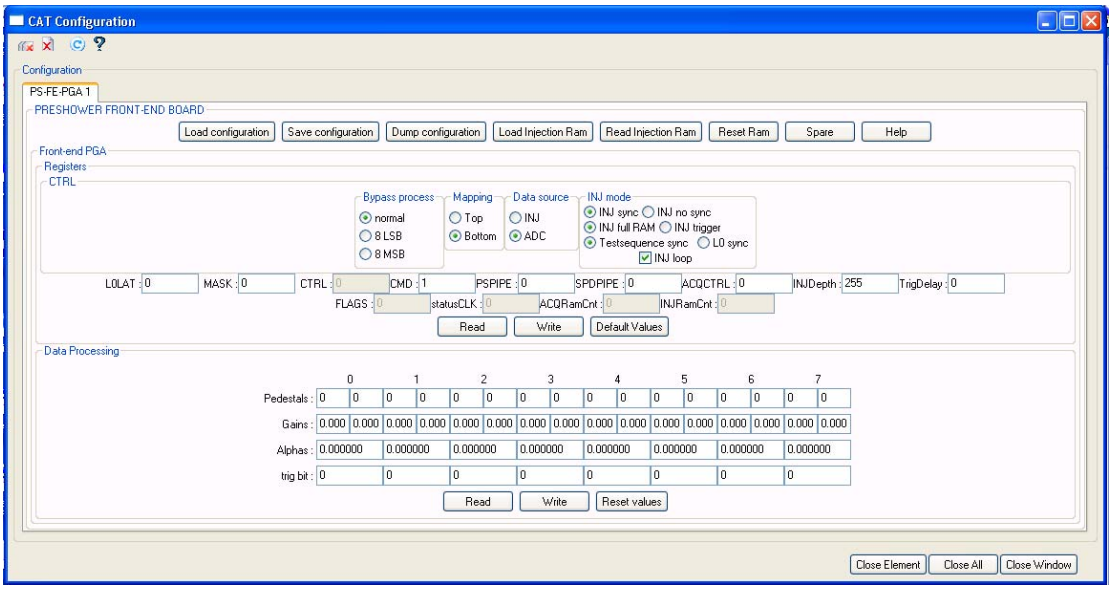

Figure 3: *FE_PGA* panel.

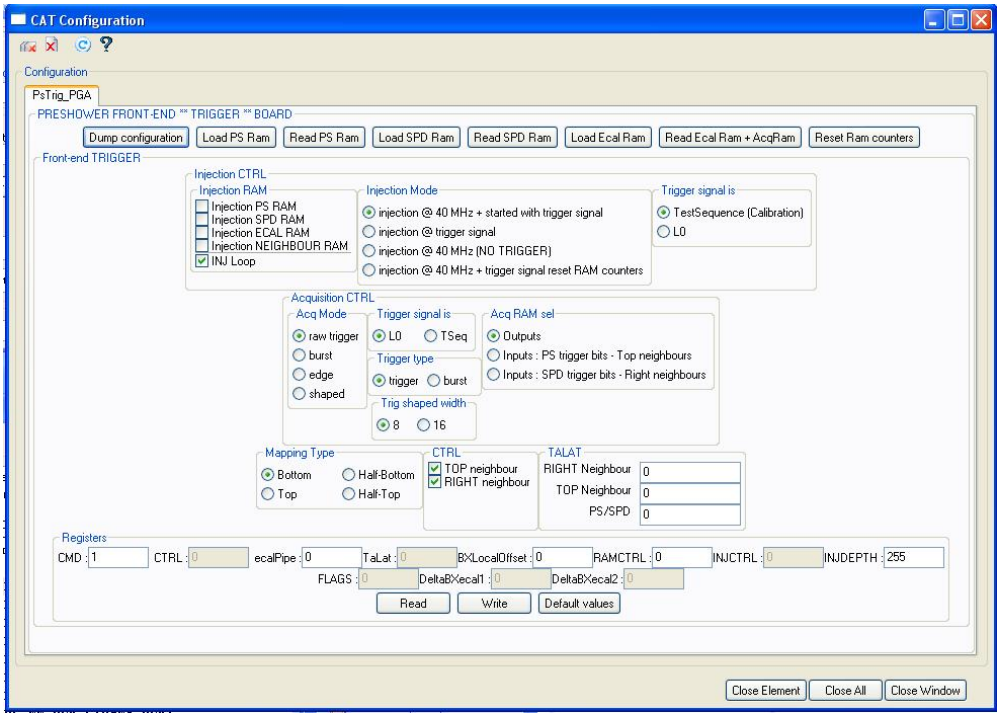

Figure 4: *TRIG_PGA* panel.

4 L0SEQ / ground clock phase range

The relative phase between the *L0SEQ* and *SEQ_PGA* clocks was varied to check that we are not near the borders of the allowed phase. It was found that the default phase lays in the middle of the allowed $(-5, +5)$ range.

5 I2C communications tests

One or several processes were created for each pertinent board component in order to check the I2C communications. The general test structure is the following:

- random numbers are shot for all the bytes to be transmitted to the element, within the required ranges
- the registers are written and re-read from the board
- in case of errors detected, a second read access is performed on the board. If the second read values fit the ones meant to be loaded, the event is considered a read error, whereas if not, the error is labeled either a write error if the two reads agree or a SPECS error otherwise. In case of SPECS error, the SPECS Master is reset before continuing.
- the errors are saved into a file, together with the occurrence time.

A single process is available for the Delay Chips (only four phases, ie 4 I2C bytes to be write/read) and for the *SEQ_PGA*, whereas two were created for the *FE_PGA*s and for the *TRIG_PGA*, corresponding to the registers attainable through short and respectively long I2C frames.

With this procedure, the table 1 gives the error rates for the eight *FE_PGA*s of the board. The global error rate if of 8/500000 frame transfers for the delay chips. For the *TRIG_PGA*, the obtained error rate is consistent with the global error rate measured for the *FE_PGA* short frames. Similar result was obtained for the injection RAMs.

The frequency of the write errors was checked by varying the I2C frames length between 4 and 13 in Write mode and no dependency on the frame length was found.

6 *FE_PGA* tests

6.1 CTRL register checks

Except the INJRAM and ACQRAM operation in synchronised/non synchronised mode and of the masking of the PS and SPD trigger channels, the good functioning of the others CTRL options was checked manually and not in an automatic

	FEPGA	0	1	2	3	4	5	6	7
short frames	read	2	2	1	3	2	3	4	3
	write	3(7)	1	1	2	4	1	3	1
	specs	0	0	0	0	0	0	0	0
long frames	read	10	16	13	3	11	15	12	7
	write	6	5	9	6	8	6	24	10
	specs	192	29	21	90	22	53	110	42

Table 1: Number of I2C communication errors on *FE*s for 500000 write accesses, for both short SPECS frames (9 I2C bytes in write mode, 12 I2C bytes in read access) and long SPECS frames (33 I2C bytes in both read/write access).

way, but all were found to work properly . We did not perform yet a common test with SPD in order to check the good functioning of the two pipelines allowing the PS and SPD data synchronisation.

6.2 Processing tests

Four processes are run to test each step of the data processing (ie the offset subtraction, the α and the gain corrections, the trigger bit computation) in the *FE_PGA* individually. The test structure is the following:

- random numbers are shot for all the parameters, within the required ranges;
- the injection RAM is loaded with a randomly shot constant pattern;
- the registers and the INJRAM are loaded and checked;
- the ACQRAM is put in the non-synchronised mode;
- the ACQRAM is read two times and if the results of the two reads are consistent, the result is compared with the expected values, after processing.
- the errors are saved into a file, together with the occurrence time.

For all the four processes, no errors were found over 22000 events.

6.3 DAQ through the *SEQ_PGA*

The data acquisition path was checked using both pedestal runs and the injection RAM. No dysfunctioning was found other than a *SEQ_PGA* instability when the system starts: once in a while and completely randomly but always at powering on, the *SEQ_PGA* does not generate the *read commands* requested by the *FE_PGA*s in order to transmit the data, after a $L0$ signal. According to the conceptors, the instability should be solved in the next *SEQ_PGA* version.

6.4 Pedestals stability and noise

Pedestal data were taken over extended periods of time and the noise levels and stability were checked. Figure 5, left shows the pedestal for one of the 64 board channels (after the offset subtraction), whereas figure 5, right shows the noise distribution for all the 64 channels. The noise level is less than 0.55 ADC count for all the channels and well within the specifications. The noise and the pedestals were also found to be stable over a run of 4 hours (see figure 6).

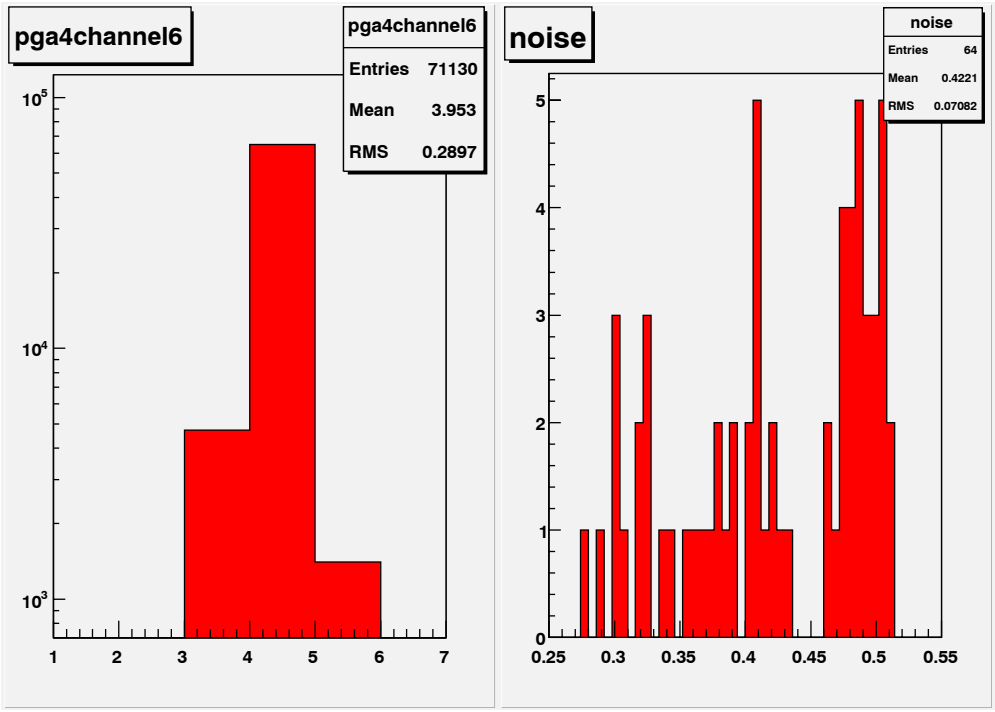

Figure 5: *Left:* Pedestal distribution (in ADC counts) after offset subtraction for channel 6 of the *FE_PGA* 4. *Right:* Noise distribution (in ADC counts) for all the 64 channels of the board.

6.5 Analog signals injection - uniformity and crosstalk

By injecting analog signals on four of the 64 channels of the board with the AWG device, it was checked that the data recorded by the DAQ was consistent with the injected values. The output channels were uniform and no digital crosstalk was observed.

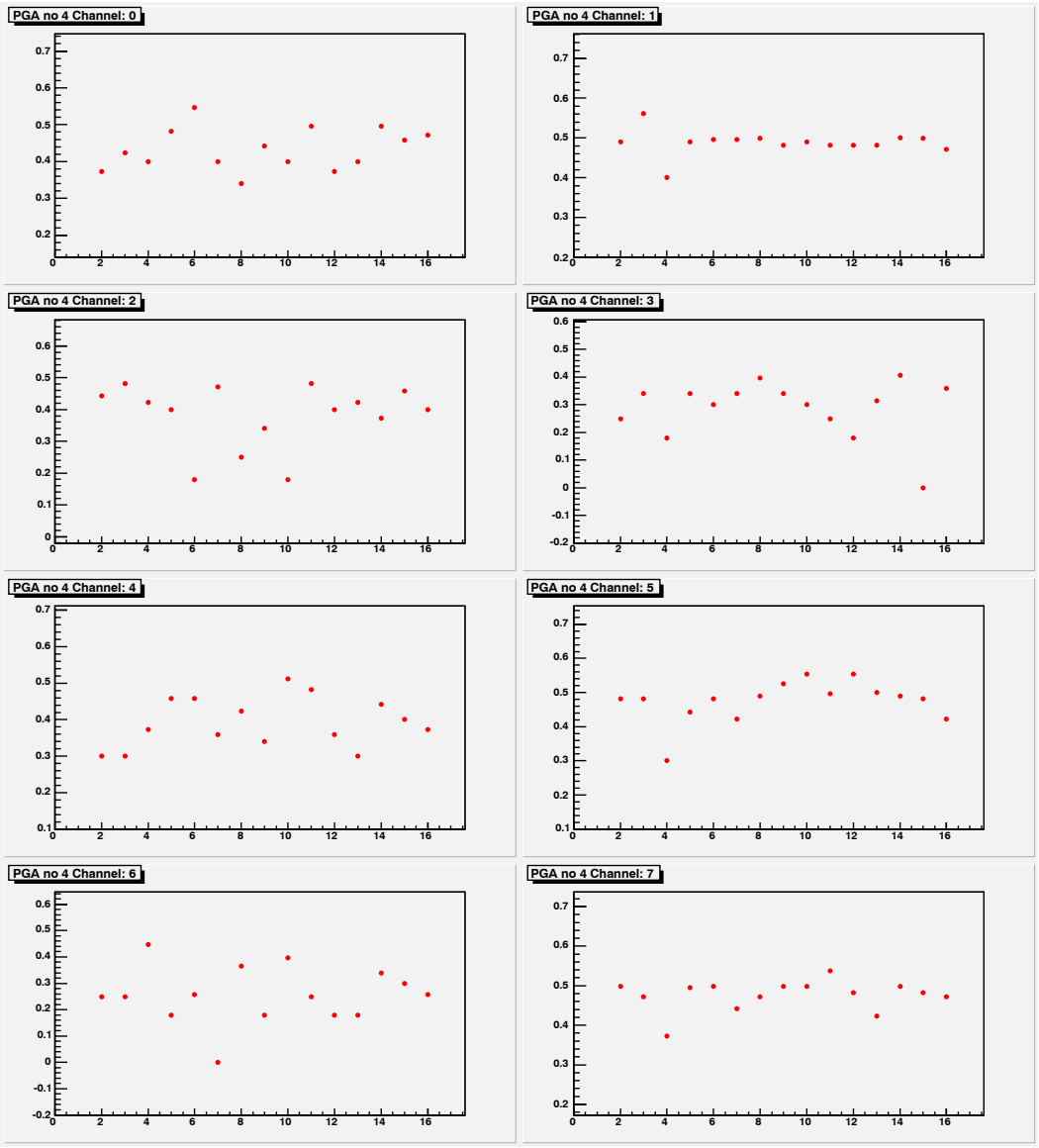

Figure 6: Noise stability over a run of $\sim$ 4h (there are 15 min between each data point) for all the board channels. The noise is given in ADC counts.

6.6 Common test with the PSVFE board

It was checked that the clock and reset signals sent to the *VFE* board were clean and had the right electrical levels.

7 The test bench for the trigger part

A PS FE board and a CROC can be plugged in a dedicated and homemade VME crate (figure 1). The clock is given by a specific board and all the devices which have to communicate with the PS FE board are emulated by memory cards. These memory cards can either inject or acquire the data which are received or sent by the PS FE board. They are steered by a computer through a VXI bus.

According to figure 7, five memory cards of 2^{16} bit depth are needed for testing the PS FE board external communications : three for the inputs, two for the outputs. Their respective roles are described in tables 2 and 3. As far as the inputs are concerned, the memory cards can be looped for a continuous injection. On top of that, the difference of phases between PS clock and input clocks (Top neighbours, ECAL1, ECAL2, SPD VFE) can be adjusted by FE board phasers.

Board name	Emulated devices	Data injected
Mem card 3	Top neighbours	PS (8b), SPD (8b)
	Right neighbours	PS (9b), SPD (9b)
	Others	TTC (8b), LO (1b)
Mem card 4	SPD VFE	SPD trigger bits (64b)
Mem card 5	ECAL1 VFE	ECAL1 BCID (7b), address1 (5b)
	ECAL2 VFE	ECAL2 BCID (7b), address2 (5b)

Table 2: *Input memory cards*

Board name	Emulated devices	Data acquired
Mem card 1	Bottom neighbours	PS (8b), SPD (8b)
	Validation board	PS BCID (7b), address1 (5b), neighbourhood1 (8b), address2 (5b), neighbourhood2 (8b)
Mem card 2	Left neighbours	PS (9b), SPD (9b)
	SPD control board	PS BCID (7b), SPD multiplicity (7b)
	Others	SEQ to CROC data (21b)

Table 3: *Output memory cards*

8 *TRIG_PGA* tests

All the tests which are reported in this document are carried out by software automated processes for which the relevant number of events can be chosen. They are aimed at checking the connexions and functionnalities of the APA component; they shall be also useful for testing the boards in the installation and commissioning phase of the electronics.

Seven versions of the TrigPGA were implemented during the prototype validation sequence. For each of them, several bugs or incorrections were identified. The results presented in this document only stands for the present version denoted *proto1*. Among the different problems encountered, the most critical one was the number of nets which were often at the limit of what the device could accept, though only half of the resources were used. It has been solved by removing the PS and SPD trigger bits injection Rams within the TrigPGa. None of the necessary internal tests is affected since those trigger bits can be injected from the FePGAs.

8.1 Algorithm tests

8.1.1 SPD multiplicity

The SPD multiplicity computation has been checked by using the FePGA injection RAMs and the TrigPGA acquisition RAM. A first (succesfull) test consisted in injecting a specific SPD pattern (cf table 4) in order to scroll the SPD multiplicity values from 0 to 64. A more comprehensive test was performed by injecting random patterns and by comparing the result of the computation to the expected value. A null error rate was achieved on several runs on 1,000 events.

8.1.2 Mapping and neighbour searching algorithm

The neighbours searching algorithm has been tested in several steps :

SPD trigger bits									SPD multiplicity
63	...	6	5	4	3	2	1	0	
0	...	0	0	0	0	0	0	0	0
0	...	0	0	0	0	0	0	1	1
0	...	0	0	0	0	0	1	1	2
0	...	0	0	0	0	1	1	1	3
0	...	0	0	0	1	1	1	1	4
0	...	0	0	1	1	1	1	1	5
0	...	0	1	1	1	1	1	1	6

Table 4: *The first seven lines of the pattern used for testing SPD multiplicity*

- First, the FePGAs-TrigPGA link connectivity and the mapping type is tested by injecting PS and SPD data from FePGAs and by displaying them in TrigPGA acquitision RAM (bypass mode activated). Mapping has been fully checked within the *TRIG_PGA* but it has still to be checked whether the mapping for half-boards is properly handled by the *TRIG_PGA*.
- Then, a simple test of the algorithm is performed. Only one couple of SPD and PS cells is randomly enabled and neighbours are set to zero. This pattern is fixed while ECAL addresses are scrolled from 0 to 31 in order to study each cell of the two 4x8 blocks. For the two mapping modes and for 32/64 blocks, this process has been run successfully over 1,000 events. An example is given in figure 8.
- A more complete test is realised by activating randomly several SPD and PS cells and by injecting Top and Right neighbours. Again, perfect behaviour of the algorithm is observed.

8.2 Injection and acquisition modes

The test procedure is akin to what was performed for the FePGAs tests. All the options were found to work correctly.

8.3 Checking external communication

As previously explained, the test bench is designed to check all the inputs and outputs lines in a board. Every connexion has been checked. It is worth to mention that most of them were checked elsewhere when common tests of the calorimeter electronics occured : two common tests in Clermont implying SPD VFE Board and the Validation Board, respectively; one was organised at CERN and all the

electronics board of the calorimeter system were available. The connectivity test of the PS FE board prototype by means of the Clermont test bench shall therefore also be seen as a preparation for the serial production qualification procedure, as far as the trigger part is concerned.

8.4 Synchronization and integration

8.4.1 PS + PS

One major point of the tests before launching the production of the boards is to check whether the communication between two PS FE boards (neighbour transmission : sending and receiving) is correct. Though the second prototype has only one FePGA instrumented, a complete communication test can be performed thanks to the internal injection and acquisition system of the TrigPGA. The two boards are plugged in the crate according to sketch of the figure 9. In this configuration, the PS FE board 2 receives the Left neighbours of the PS FE board 1 by the backplane and the Bottom neighbours of the PS FE board 1 by a cable.

First, fixed PS and SPD patterns are injected in the first PS FE board. The test consists in checking the good reception of neighbours by the second PS FE board (use of acquisition RAM in bypass mode). It has already been checked that the neighbours are properly taken into account in the neighbour searching algorithm.

8.4.2 ECAL + Trigger validation board

As already mentionned, a common test took place at CERN in which all the electronics boards of the calorimeter system were available. The outcome of the test is not directly related to the validation of the PS FE Board prototype prior to the serial production. Yet, ECAL and PS FE Boards were operated synchronously with success and a systematic scrutiny of the result of the search for neighbour was performed at the Validation Board level. The test lasted five hours and no error out of 600 000 events was observed, giving confidence in the device on one hand, in the ability of integrating succesfully several different FE Boards on another hand.

References

[1] *Presentation of the Software for the Monitoring and Control*, F. Machefert, Calorimeter Meeting, LHCb week, 8 March 2005.

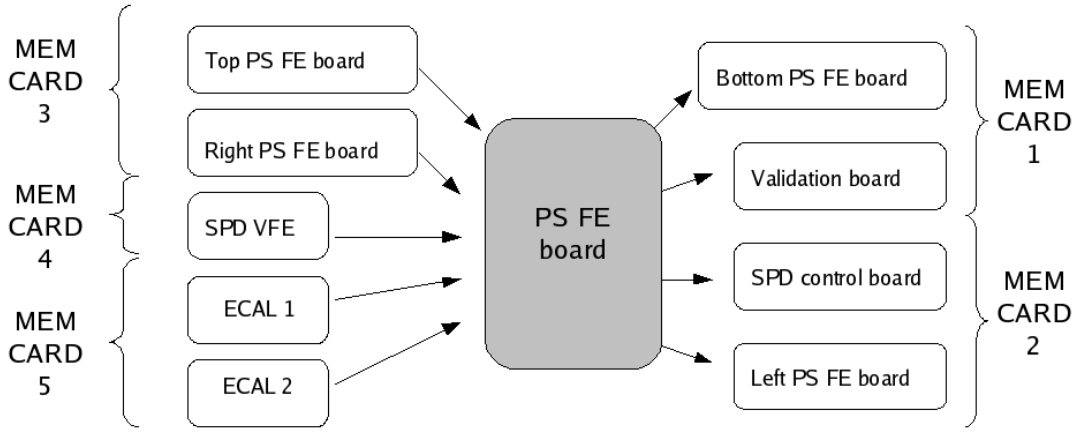

Figure 7: *Devices emulated by memory cards*

0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0
0	0	0	0	0	0	0	0

PS(left) and SPD(right) matrices before mapping

0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	0	0	0	0	0	0

PS(left) and SPD(right) matrices after Bottom mapping

@val1	val1	@val2	val2
0	0	0	0
1	0	1	0
2	0	2	0
3	64	3	0
4	32	4	0
5	0	5	8
6	0	6	1
7	0	7	0
8	0	8	0
9	0	9	0
10	0	10	0
11	128	11	0
12	16	12	0
13	0	13	0
14	0	14	0
15	0	15	0
16	0	16	0
17	0	17	0
18	0	18	0
19	0	19	0
20	0	20	0
21	0	21	0
22	0	22	0
23	0	23	0
24	0	24	0
25	0	25	0
26	0	26	0
27	0	27	0
28	0	28	0
29	4	29	0
30	2	30	0
31	0	31	0

Figure 8: *Example of simple test results (Bottom mapping, whole card), same conventions as in the relevant figure of the companion note.*

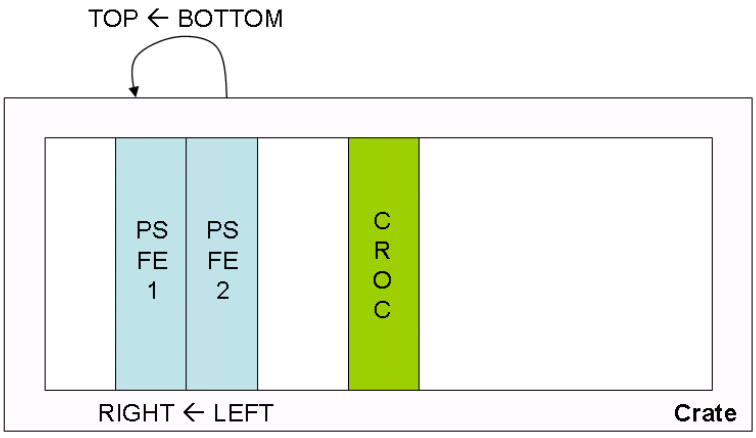

Figure 9: *Experimental setup for testing the two PS FE board synchronization*