OT FE-Box Test Procedures

April 2, 2008

Abstract

Abstract: The OT FE readout requirements is the precise (∼0.5 ns) and efficient drift time measurement at an occupancy of ∼4% to ensure single hit resolution. The acquired achievement of such performance on an assembled FE−Box is verify through a final test performed using a special FE−Tester. In this note the test procedures are described.

LHCb Technical Note

Issue	Preliminary
Revision	4
Reference	LHCb-2007-122
Created	Semptember 14, 2007
Last Modified	April 2, 2008

Prepared by A. Pellegrino, E. Simioni, T. Sluijk, A. Zwart, J.D.Schipper
P. Timmer, F. Jansen, N. Tuning, H. Terrier, T. Du Pree
Ad Berkien, † A. Weber, P. Caputa
NIKHEF, Amsterdam, The Netherlands

† *On leave from Physikalische Institut, Heidelberg, Germany*

Contents

List of Tables

1 Overview of the Readout System

The FE−Box readout has a modular structure consisting of four different type of boards: HV board (decoupling the analog signal from the high voltage), ASDBLR aboard (amplification), OTIS board (drift time measurement) and GOL auxiliary board (supply voltage and the optical link for data transmission). The boards are installed in an aluminum frame built to fit on the straw module providing the mechanical protection and electrical shielding to the electronics inside.

1.1 Amplifier

Charge signals from the straw detector are decoupled from the high voltage and amplified, shaped and discriminated by the ATLAS ASDBLR chips. The main characteristics of the ASDBLR chip are:

1. Eight input channels and two test pulses (low and high).

2. A fast peaking time of ∼6ns due to a shaping network and the baseline restoration which separate the leading edge of the input signal and cut the ions induced current tail.

3. Radiation hardness withstanding 3.5 10^{14} n/cm^2 [1].

4. Low cross talk of 0.2% and low noise of <1fC equivalent charge thanks to the DMILL bipolar process adopted for the chip production.

5. Optimized for grounding and heat dissipation through a 100 μm copper layer endowed in the PCB and several vias between the board layers.

The block diagrams of the chip functionality is shown in Fig.1. Two ASDBLR chip are assembled on one ASDBLR board.

1.2 Time to Digital Converter (TDC)

Digitized signal from two ASDBLR boards are then collected by the OTIS board [3] (Outer tracker Time Information System) which contains a 32 channel TDC. The chip is developed using a standard 0.25 μ CMOS process. The drift time data of each channel is stored in a pipeline of 4 μs waiting for the trigger veto. The block diagram of the OTIS chis is reported in Fig. 2.

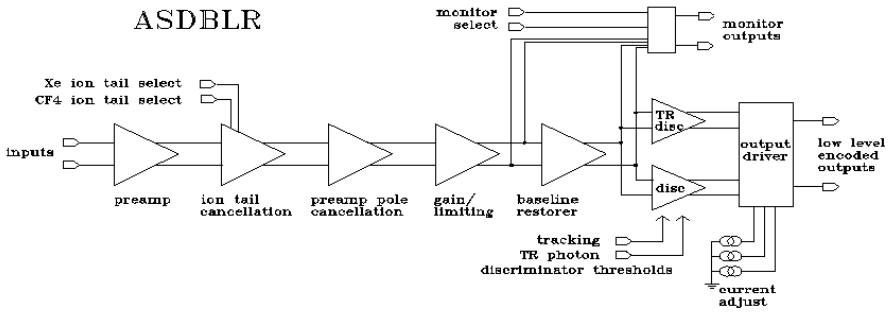

Figure 1: Block diagram of the ASDBLR Chip.

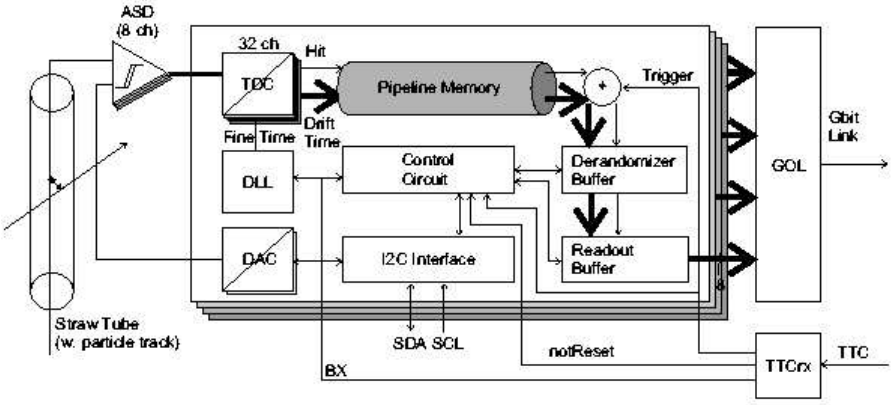

Figure 2: Block diagram of the OTIS Chip

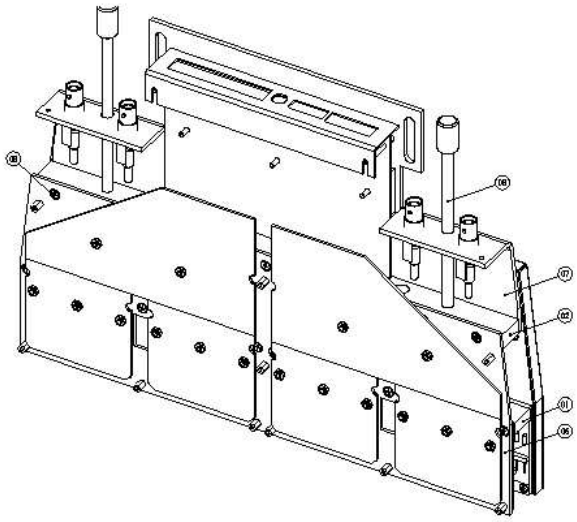

Figure 3: Outline of the FE−Box chassis with boards.

1.3 Gigabit Optical Link (GOL)

At L0 accept the output of the TDC is collected by one Gigabit Optical Link chip (GOL) assembled in the GOL auxiliary board. The GOL board collects the signals coming from four OTIS boards and low voltage supply (+2.5 V and ± 3 V), TFC signals (Time and Fast Control) and I^2C slow control bus. Optical fibers carry the data ∼90 meters far from the detector at the L0 output rate of 1.1 MHz to the TELL1 board [2] in order to be filtered and finally stored for off-line processing.

1.4 FE−Box

The FE−Box consists of an aluminum chassis designed to fit one end of the detector module on which are installed 4 HV boards, 8 ASDBLR boards, 4 OTIS boards and 1 GOL auxiliary board. The FE−Chassis provides the cooling system, four inputs for the HV, the shielding cover and two connectors to fix the FE−Box on the straw module. In Fig.3 the drawing of as open FE−Box is shown.

2 FE−Test Setup Description

The electronics readout requirements are a precise (∼0.5 ns) and efficient drift time measurement at an occupancy of 4% to ensure single hit resolution (200

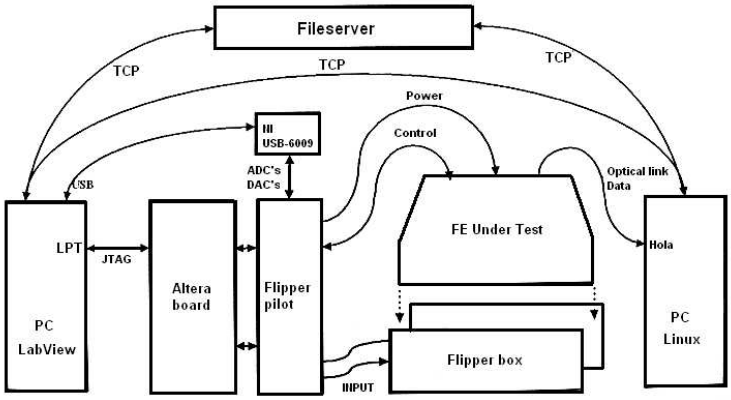

Figure 4: Block diagram of the FE Test Setup.

micron) and efficient charged particle reconstruction. To achieve the desired performance, several steps of quality assurance during the production have been applied, using dedicated test setups for each type of board [7].

The performance on an assembled FE−Box is verified through a final test performed using a special FE−Tester. The block diagram of the setup is shown in Fig.4. The FE−Tester is based on the test setup build for the Alice Alcapone tester. The heart of the setup is a PCB with an Altera programmable logic chip. Most of the electronics needed for the tests is built on the controller board. To interface the FE−Box a specific connection board is developed (Flipper Box) with the additional required electronics to provide the input signal on the 128 channels of the FE−Box. The logic in the Altera chip is controlled by a LabView program on a PC. The connection between them is a JTAG interface through the parallel port. For the communication with the FE−Box the I2C bus is used. The out-coming data stream from the GOL board is collected by the HOLA acquisition board [4]. The data exchange between the two machine and a file-server is guarantee by standard TCP.

In summary the FE−Tester consists of a programmable pulser capable to provide all the functionality of the readout (slow and fast controls) mimicking the input signals as real module detector. the FE−Test functionality are here summarized:

1. Generation of input signals straw-like. Those signals are tunable in intensity and in time with a resolution of $\sim$0.5 fC and 150 ps respectively.

2. Generation TFT (Time and Fast Control).

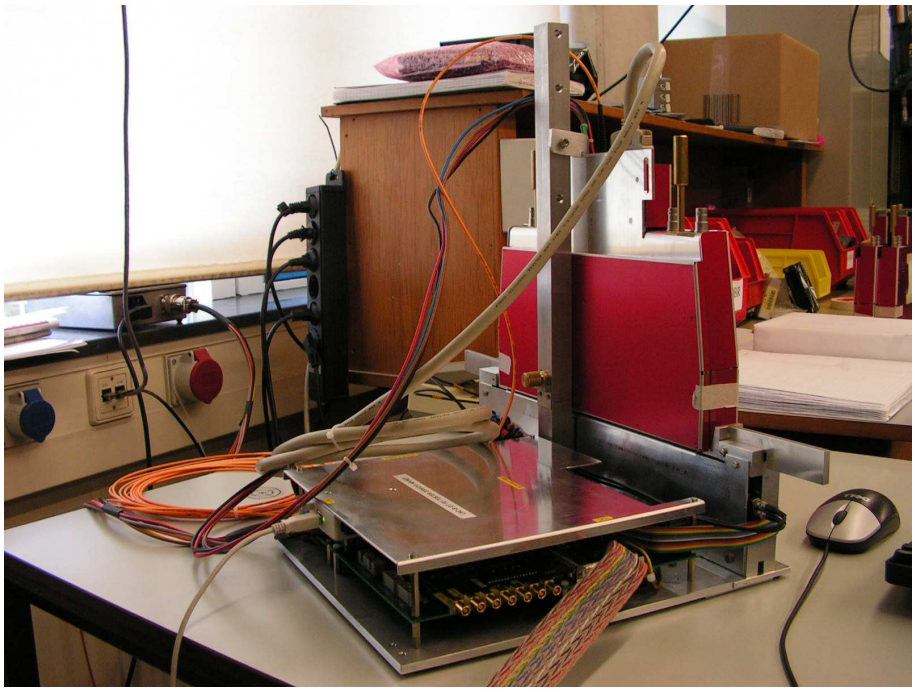

Figure 5: Picture of the FE−Setup at NIKHEF.

3. Generation of I2C (Slow Control).

4. Power supply and data acquisition.

All those operations are automatized and controlled through LabView. In Fig. 5 a picture of the FE−Setup is shown.

3 Test of the FE−Box

The following tests have been performed on assembled FE−Boxes:

1. Threshold Characteristics. A threshold scan is done and the measurement of the half-efficiency-point is carried out for a fixed input charge. The relative variation of the half-efficiency-point is expected to be less than 60 mV (rougly corresponding to half fC) out of the 128 channels as required in the ASDBLR chip selection [6]. A threshold scan is also performed using the test pulse signals (low and high) generated in the ASDBLR chip. The last test on the preamplifier is done through an amplitude scan with fixed threshold to carry out the half-efficiency-point and the ENC (equivalent noise charge).

2. Timing. Measurement of the time conversion linearity and the channel-by-channel resolution of the OTIS board.

3. Noise. Dark noise is studied as function of the threshold.

4. Synchronization. Four 8 bit TDC chips are inside a single FE−Box. The time difference between test pulse and the L0 is checked with a latency scan and therefore the synchronization between channels is verified.

3.1 Threshold Characteristics

One general requirement of the preamplifier, is the channel-by-channel uniformity response for the same input charge Q_i. The efficiency, noise and occupancy are strongly sensitive to the threshold which influence the detector performance. The threshold must be chosen such that the uniformity between channels is guaranteed in a wide range of input charge.
Given the function $g(Q_i)$ representing the signal amplitude after pre-amplification of the input charge Q_i, to measure channel-by-channel uniformity we need to "compare" those amplitudes between channels defining an appropriate

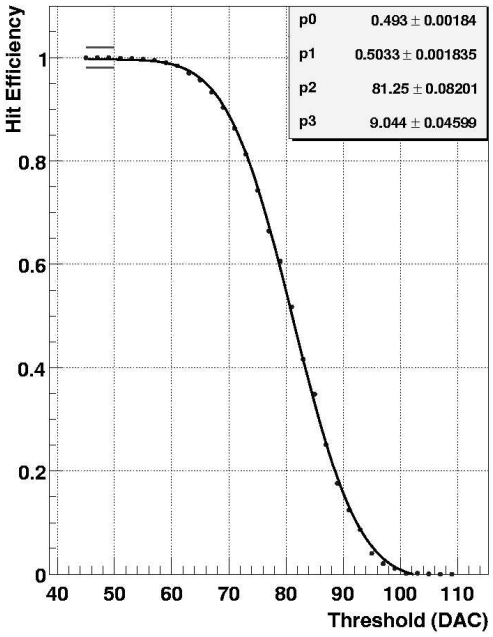

Figure 6: Hit-efficiency as function of threshold for a fixed input charge.

amplitude estimator. The easiest number to measure is the hit-efficiency. Varying the threshold from low to high, the hit-efficiency goes from 1 to 0. In the ideal condition of absence of noise the hit-efficiency profile against threshold would be modeled as a step function. Assuming Gaussian noise the expression for the hit-probability for a fixed threshold and input charge is [5]:

$$Pr(V_{thr}, Q_i) = N \int_{V_{thr}}^{+\infty} e^{-\frac{1}{2}\left(\frac{V-g(Q_i)}{\sqrt{2}\ \sigma_{noise}}\right)^2} dV \tag{1}$$

Where N is a normalization factor, V is the threshold and σ_{noise} is the Gaussian noise amplitude. The Eq. 1 can be rewritten using the standard erf function:

$$Pr(V_{thr}, Q_i) = \frac{1}{2} \ - \ \frac{1}{2} Erf\Big(\frac{V_{thr} - g(Q_i)}{\sqrt{2}\ \sigma_{noise}}\Big) \tag{2}$$

The hit-efficiency is 50%. for $V_{thr} = g(Q_i)$. The threshold in which the condition above is realized is called half-efficiency threshold and from now on we refer to it as $V_{thr}^{50\%}$, which is the estimator for $g(Q_i)$. By measuring the hit-efficiency profile against threshold and fitting the Erf function model, we can determine channel-by-channel the $V_{thr}^{50\%}$ and the σ_{noise} as shown in Fig 6. The hypotesis of gaussian error fits the data points.

Parameter	Charge	Cut
ΔV_{thr}^{max}	5 fC	$\pm$ 30 mV
ΔV_{thr}^{max}	30 fC	$\pm$ 60 mV
ΔV_{thr}^{Gmax}	5 fC	$\pm$ 30 mV

Table 1: Selection cuts on $V_{thr}^{50\%}$ uniformity for ASDBLR chip.

3.1.1 Requirements in the $V_{thr}^{50\%}$ uniformity

Each ASDBLR chip has been individually tested at UPENN university before assembly. By the test results, chips have been first pre-selected in order to separate chips with working problems and then further selected applying constraints on the $V_{thr}^{50\%}$ uniformity. The two main parameter defined for a single ASDBLR chip are:

1. ΔV_{thr}^{max} : The absolute maximum deviation by the average in the half-efficiency-point measured on the single ASDBLR (8 channels).

2. $\Delta V_{thr}^{G\ max}$: The absolute maximum deviation by the global average in the half-efficiency-point (measured on the total amount of preselected chips).

Five different values of injected charge have been used in the chip test, (0, 3, 5, 30 and 50 fC) and the cuts applied after pre-selection are summarized in Table 1.

3.1.2 Threshold Scan with the FE−Setup

The channel-by-channel $V_{thr}^{50\%}$ is determined in three ways: using the FE−Box input and the two test-pulses in the ASDBLR chip.

1. From the input: injection of the signals through the flipper-box (straw-like signals).

2. From Test-pulse: signals generated by the slow-control and routed through the GOL board and the four OTIS until the the 16 ASDBLR ICs. In the ASDBLR there are two test-pulse inputs: high test-pulse and low test-pulse. The amplitudes of those test-pulses are not tunable.

The functioning and the performance of the ASDBLR once assembled on the PCB is guaranteed by three different channel-by-channel determinations of the $V_{thr}^{50\%}$.
About 2% of assembled ASDBLR chips show a channel broken or having a

large deviations. Usually this is due to problems in the chip soldering, missing components or damaged ASDBLR board input/output connector pins. The uniformity in the $V_{thr}^{50\%}$ is in good agreement with the requirements adopted in the chip selection.

3.1.3 Systematics in the input Threshold Scan

The $V_{thr}^{[50\%]}$ is determined with good accuracy of $\sim$1% and systematic deviations due to the setup (in particular the flipper box) are detectable. As shown in Fig. 4, the flipper box receives from the control pilot two signals, one for each side of the FE−Box. Each signal is then split through 64 channels but the amount of charge available slowly decreases going from the first to the last channel. Since the half-efficiency-point is a function of the injected charge the first channel has higher value of $V_{thr}^{[50\%]}$.
This systematic can be estimated and an offset to each channel is added. An offset up to the $\sim 4\%$ has been measured, based on a Gaussian fit to the 128 distributions of $V_{thr}^{[50\%]}\,(\mathrm{FE}, \mathrm{ch})$ measured in testing the FE−Boxes. In Fig. 7 the profile of the offsets measured for each channel are shown.
The values of the means $\{\mu\,(\mathrm{ch}) : \mathrm{ch} = 1, ..., 128\}$ from the Gaussian fits are then used to calculate the offsets:

$$\epsilon(\mathrm{ch}) \equiv \frac{1}{128}\sum_{k=1}^{128}\mu(k) - \mu(\mathrm{ch}), \tag{3}$$

which are used to correct the values of $V_{thr}^{[50\%]}$ measured:

$$V_{thr}^{[50\%]}\,(\mathrm{FE}, \mathrm{ch}) \rightarrow V_{thr}^{[50\%]}\,(\mathrm{FE}, \mathrm{ch}) + \epsilon(\mathrm{ch}). \tag{4}$$

3.1.4 Half-efficiency-point in the input charge amplitude scan

As shown in Fig. 8, increasing the input charge for a fixed threshold the hit efficiency goes from 0 to 1. As in the threshold scan, the ideal profile would be a step function but assuming Gaussian noise the following model can be used to fit the data points:

$$Pr(Q_i, V_{thr}) = \frac{1}{2} \;+\; \frac{1}{2}Erf\Big(\frac{g(Q_i) - V_{thr}}{\sqrt{2}\;\sigma_{noise}}\Big) \tag{5}$$

Now assuming that amplifier response is linear [5] we can write:

$$Pr(Q_i, V_{thr}) = \frac{1}{2} \;+\; \frac{1}{2}Erf\Big(\frac{g(Q_i) - Q_{thr}}{\sqrt{2}\;ENC}\Big) \tag{6}$$

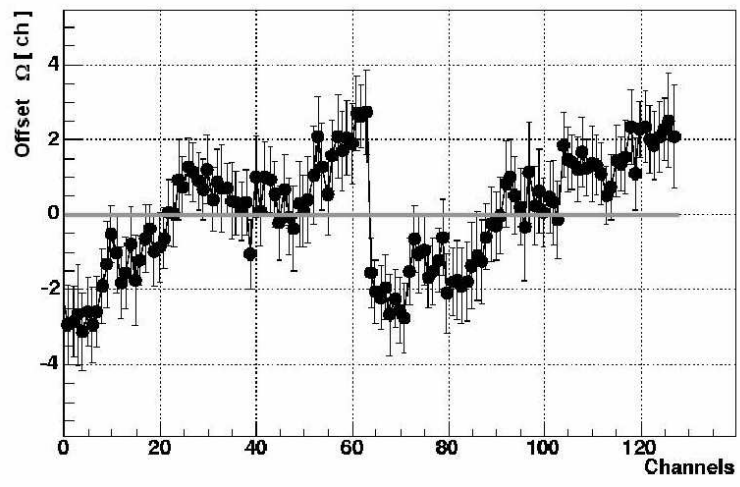

Figure 7: Offset Corrections ϵ(ch) as function of channels.

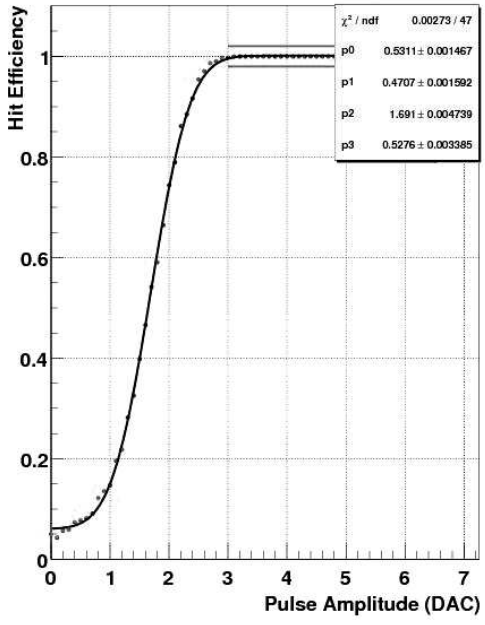

Figure 8: Hit-efficiency as function of amplitude charge for a fixed threshold.

Obtaining a direct measurement of the ENC (equivalent noise charge). This measurement is strongly anti-correlated and complementary to the one performed in the threshold scan.

3.1.5 Test Settings

The threshold range and other default parameters of the test are summarize in table 2 and 3.

Signal	Charge	Starting Thr	Step Size	#Steps
Input	3	46	2	32
Test-pulse low	fixed (1.5 DAC)	80	2	32
Test-pulse high	fixed (3.5 DAC)	46	2	32

Table 2: Parameters used in the threshold scans. All the number are given in DAC.

Signal	Threshold	Starting Charge	Step Size	#Steps
Input	80	0	0.1	50

Table 3: Parameters used in the charge amplitude scan. All the number are given in DAC.

3.2 Timing

The aim of the timing test is to measure the channel by channel linearity and resolution.

3.2.1 Linearity of OTIS

The FE−Setup provides a straw-like signal with high time accuracy (0.15 ns). Tuning the delay between the L0 and the input signal (for fixed threshold and input charge) a delay scan is performed. Considering the overall steps and matching the mean measured drift time (see Fig. 9) with the time delay set, the linear correlation shown in Fig. 10 is obtained for each channel. The straight line runs over the readout window of 192 TDC (75 ns) as shown in Fig. 10.
One out of 20 FE−Boxes shows bad linearity or large offset deviant from other channels.

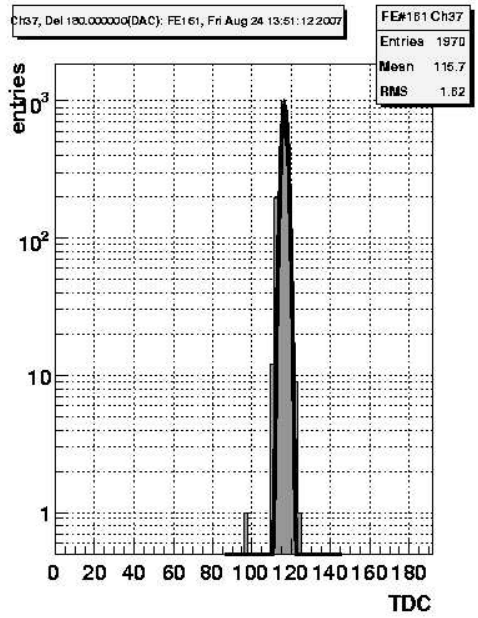

Figure 9: Example of drift time distribution with a Gaussian fit.

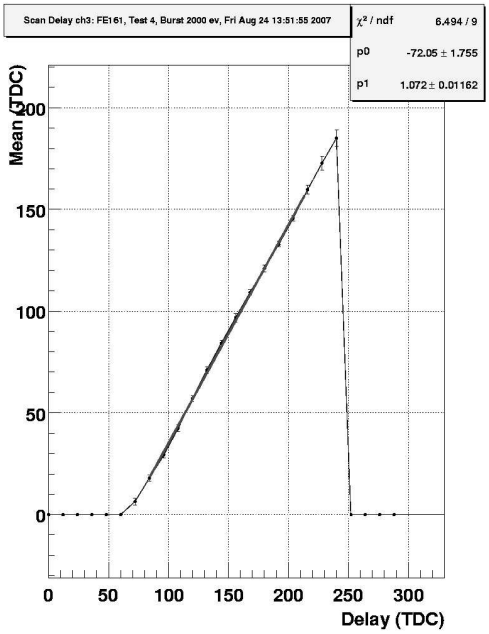

Figure 10: Linearity of the OTIS board.

3.2.2 Systematics in the input Delay Scan

Due to the high time accuracy, systematics due to the setup are detectable. The flipper pilot generates two input signals which goes through the flipper box as explained in the previous section. The time offset between the two main signals is easily detectable with the oscilloscope and can be corrected tuning the cable length or introducing a delay unit. A second source of systematics is due to the fact that each main signal is split between 64 channels. As conseguence the signal has to go through the flipper box yielding a channel-by-channel delay of about $\sim$0.2 ns. This time offset does not affect the linearity studies but only shift the straight line on Fig. 10.

3.2.3 Test Settings

To estimate the linearity of the four TDC of a FE board several acquisition of 2000 events has been take varing the set delay like shown in the table 5.

Signal	Charge	Starting Delay	Step Size	#Steps
Input	4	0	30	25

Table 4: Parameters used in the delay scan. All the number are given in DAC.

3.2.4 Resolution

By the sigma of the Gaussian fit applied on the drift time spectra, the single-channel time resolution is estimated. Noisy channels or channels with double-peak in the drift spectra are detected by with a large value of sigma. Combining all the drift time spectra collected in the first part of the production we can infer the average time resolution of the OTIS: 1.3 $\pm$ 0.2 TDC which correspond to 0.50 $\pm$ 0.06 ns as shown in Fig. 11.

3.3 Noise

A threshold scan is performed without input. For very low threshold (20 DAC, corresponding to $\sim$200 mV) the hit efficiency is 1 but increasing the threshold it decreases exponentially to zero as shown in Fig. 12. This dependence is studied for each channel aiming to find noisy channels or problems due to bad shielding cover. For a threshold less than 20 DAC (200 mV) due to signal reflection the noise fraction is less than one. In Fig. 13 the noise

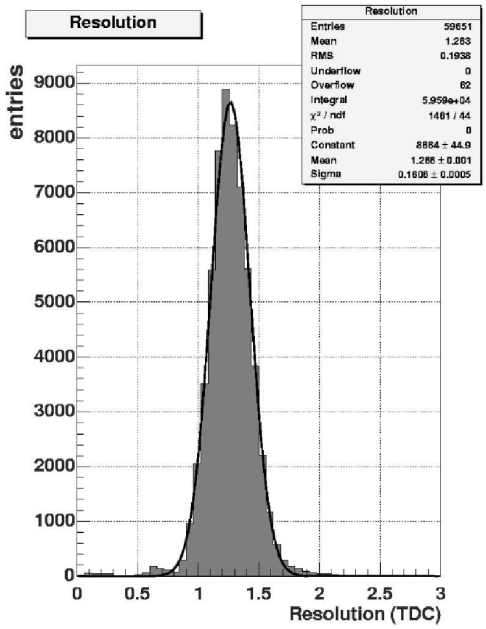

Figure 11: Distribution of the time resolution as carry out by the datas of the FE mass production tests.

entries (out of a burst lenght of 2000 events) map is shown. About one out of 30 FE−Box are repaired due to this.

3.3.1 Test Settings

Signal	Charge	Starting Thr	Step Size	#Steps
Input	0	14	2	32

Table 5: Parameters used in the noise threshold scans. All the number are given in DAC.

3.4 Synchronization

Drift time information per event is stored in a 4 μs pipeline buffer in the OTIS chip waiting for the LO trigger decision. Since four OTIS chips are embedded in a FE−Box it is crucial to verify whether the latency is equal for all the channels. Varying the delay between the high Test-Pulse and the L0,

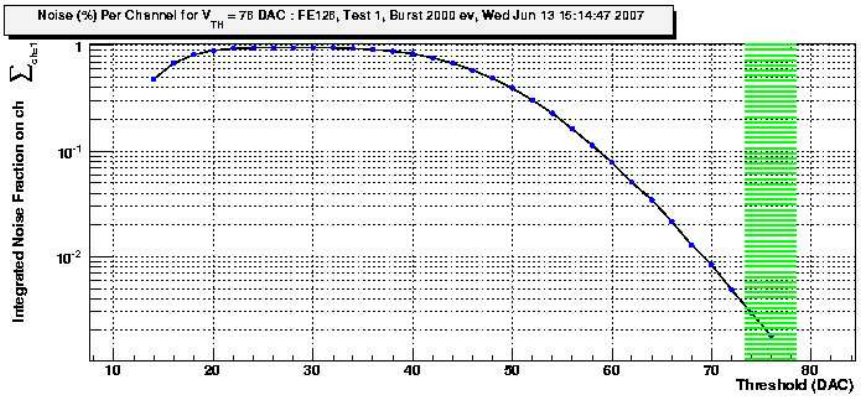

Figure 12: Average noise fraction as function of threshold.

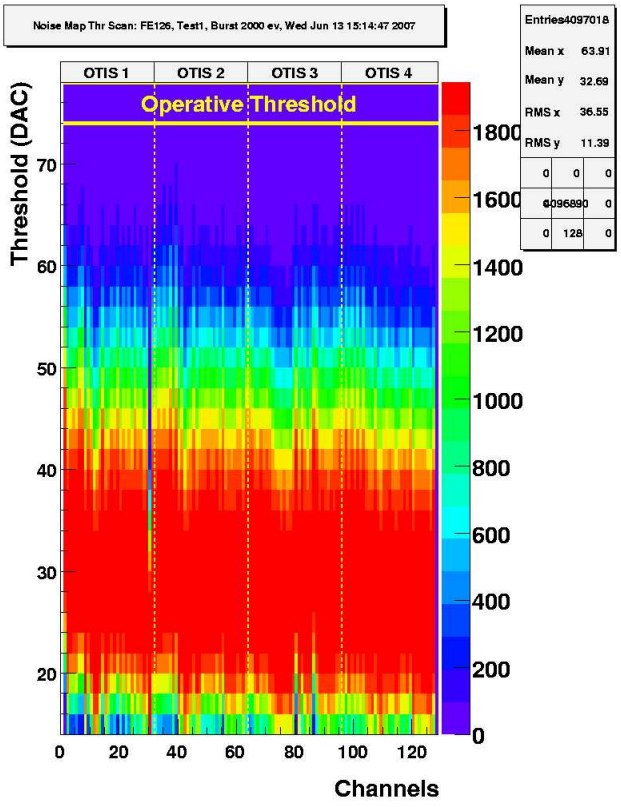

Figure 13: Noise entries as function of threshold.

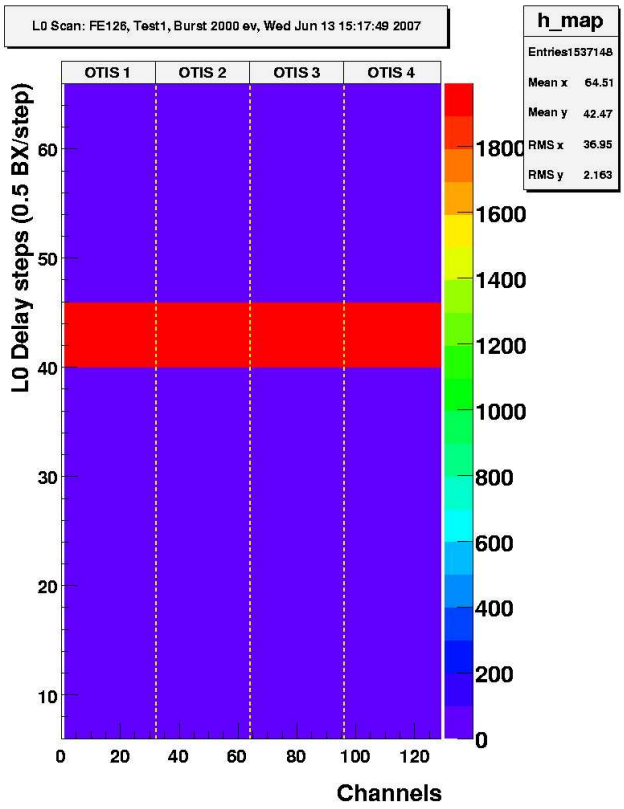

Figure 14: Summary plot of Latency scan.

a latency scan in steps of 12.5 ns is performed to verify the overall synchronization across the read-out windows of 75 ns. When the synchronization is reached the hit efficiency is one while is zero otherwise. In Fig. 14 the number of entries are reported as function of the L0 delay.

3.4.1 Test Settings

Signal	Charge	Starting L0	Step Size	#Steps
Test-pulse high	fixed	0	0.5 bx	60

Table 6: Parameters used in the latency scans. All the number are given in DAC exept for the Step Size.

4 Summary

The FE−Setup has been used during the R&D phase of the Outer Tracker electronics. Its usefulness was proven by finding problems at an early stage and finally it was crucial to improve the overall performance. Secondly, the FE−Tester was used during mass production of the FE−Boxes, and commissioned each FE−Box before delivery to CERN for the installation on the Outer Tracker.

References

[1] Mitch Newcomer et al. [Nuclear Science Symposium Conference Record, 2002 IEEE Publication Date: 10-16 Nov. 2002, Volume: 1, On page(s): 151- 155 vol.1] *Radiation Hardness: Design Approach and Measurements of the ASDBLR ASIC for the ATLAS TRT*

[2] Legger, F; Bay, A; Haefeli, G; Locatelli, L [Nucl. Instrum. Methods Phys. Res., A 535 (2004) 497-499] *TELL1 : development of a common readout board for LHCb*

[3] [EDMS Note, 859585 (2007)] *The OTIS 1.1 Reference Manual,*

[4] E. B. van der.[CERN, Geneva, Switzerland. [Online]. Available: http://hsi.web.cern.ch/HSI/s-link/devices/hola] *HOLA High-Speed Optical Link for ATLAS*

[5] A. Pellegrino et al. [LHCb Collaboration, CERN-LHCb-2004-117.- Geneva : CERN, 14 Dec 2004 . - mult. p], *Noise Studies with the LHCb Outer Tracker ASDBLR Board.*

[6] E.Simioni, T. Sluijk, A. Pellegrino. [LHCb Collaboration, CERN-LHCb-2005-088.- Geneva : CERN, 07 Nov 2005 . - 25 p], *Selection of ADSLBR chip for LHCb Outer Tracker FE.*

[7] E.Simioni, T. Sluijk, N. Tuning et al. [LHCb Collaboration, CERN-LHCb-2007-122.- Geneva : CERN, 07 Sept 2007 . - 25 p], *OT FE boards Test and Production*