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THE UA1 DATA-ACQUISITION SYSTEM

The UA1 Collaboration

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Abstract

The data-acquisition system of the UA1 experiment running at the CERN $p\bar{p}$ collider is described. The front-end electronics generates 1.6 Mbytes of raw data for each event. Parallel data-stream processors reduce the typical event data to 60,000 bytes in a time of less than 10 ms. Data are read out by Remus CAMAC branches, formated data streams being read in parallel by buffer units with multi-event storage capability. For test and monitoring, the data flow can be accessed by local processors associated with each detector subsystem. Alternatively, the over-all system can be partitioned off in a set of independent subsystems running their own data acquisition with or without a synchronous trigger. On-line functions are assured by a number of multi-task and dedicated-task 16-bit and 32-bit computers. A variety of microprocessor-based systems with autonomous capabilities control the experimental apparatus.

Introduction

The UA1 experiment is a general-purpose detector system designed to provide a full solid-angle coverage of the LSS5 intersection region at the CERN $p\bar{p}$ collider. The apparatus is composed of a variety of complementary detectors surrounding the collision region to provide particle tracking, electromagnetic and hadron calorimetry, muon identification, and magnetic analysis. The over-all detector structure has been described elsewhere[1], and the image chamber central detector is the subject of a separate contribution to this conference.

The data-acquisition system presented in this report is a Remus CAMAC readout system with distributed intelligence and function separation facilities. Its development started at CERN in 1979, and data taking commenced in July 1981 during the collider machine development period. This report describes the general components of the system and the way in which its major functions are at present implemented.

1. Trigger Rate

When six proton-antiproton bunches are circulating in the collider, a beam crossing occurs every 3.8 μs. At the ultimate luminosity of 10^{30} cm^{-2} s^{-1} the expected collision rate is about 50 kHz.

The total number of channels in the detector (ADC, TDC, wires) is about 20,000, and the digital information, accumulated by the front-end electronics after a trigger, consists of 1.6 Mbytes. The majority of these data come from the central detector, where wire pulses are sampled every 32 ns over a time of 4 μs. The typical event data are reduced to 60,000 bytes by a set of parallel processors at a rate of 100 Hz. The maximum data-taking rate is limited to 10 Hz by the tape writing speed.

The data-acquisition system is structured in three distinct stages: data reduction and formating, data collection and filtering, and computer data-taking. Each stage of the data acquisition runs with its own dead-time, so corresponding levels of trigger decision are combined in order to reduce the rate between stages.

To reduce the trigger rate from 50 kHz to 100 kHz, two levels of trigger decision take place before the data reduction phase is initialized. The first-level decision is made between beam crossings; events are selected on the basis of energy deposition in the calorimeter and a muon particle identification. The second-level trigger is only activated if a muon candidate is identified in the first level. By means of microprocessors, the muon drift chamber information is analysed to determine, with more accuracy, if the muon candidate comes from the interaction region.

A third-level trigger makes decisions based on the analysis of the event data; it uses processors programmable in high-level language (168E) and it is part of the data-collection stage of the system. Levels two and three are at present still in a state of development and they will not be described here.

2. Data Reduction and Formating

The data reduction phase takes place at the occurrence of a first-level trigger (and second level if enabled). It consists of the suppression of null information channels and data re-formating with or without arithmetic computations.

The information coming from the calorimeters, the muon chamber (without second-level trigger), and the very forward chamber (VFC) is either already packed by the digitizer electronics or directly treated by hard-wired devices with a fixed and simple algorithm such as the LRS 2280 ADC processor. The amount of data generated by this part of the apparatus is of the order of 20,000 bytes and the reduction time is more or less constant at 3 ms.

The handling of the information coming from the central detector is more complex.

The basic principle of each sense-wire readout electronics[2] is represented in Fig. 1.

By means of two six-bit fast analog-to-digital converters (FADCs), the digitizing electronics samples the two wire-edge pulses every 32 ns, measuring a non-linear function of the energy loss dE/dx and, directly, the track position along the wire by charge division method. The drift time within the window of 32 ns is measured by a three-bit time-to-digital (TDC) interpolator with an accuracy of 4 ns, and an additional bit, the time tag, flags the sample at which a start of pulse (hit) has been detected.

The digital outputs of the two FADCs, the TDC, and the time tag are then stored in a circular buffer memory, 128 words deep, of 16 bits, providing a continuous record of the last 4 μs wire information (the maximum drift time in the chamber is about 3.6 μs).

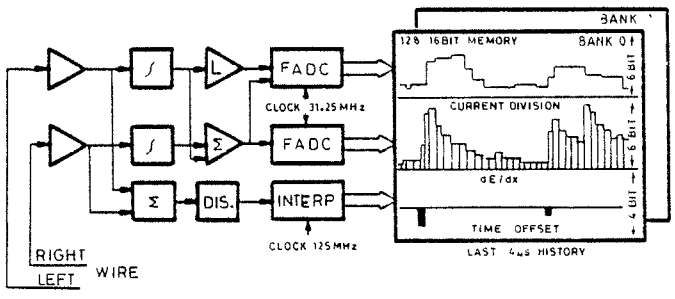

Fig. 1. Central detector wire readout block diagram.

To allow all the electronic channels to operate with identical performances and to obtain the maximum of accuracy in charge division measurement, two gains and four off-sets in each signal processing channel are adjustable over a small range by means of six-bit digital-to-analog converters (DACs).

A four-unit CAMAC module, the charge and time digitizer (CTD), supplies the digitizing and control electronics for 12 wire channels.

The elementary system for the central detector data reduction is a CAMAC crate containing one time-stop interpolator, five charge and time digitizers, and one readout processor (ROP)[3]. Each crate can handle up to 60 wires, and the complete set-up consists of 110 crates.

Given the functions of the digitizing electronics, at the occurrence of a trigger 15,360 bytes are accumulated in the CTD memories of each crate and 1.6 Mbytes in all the system. This primary information must be reduced as quickly as possible in the form of single-hit coordinates, such as the drift time, the wire number, the track position along the wire, the energy loss, and the pulse duration. This is one of the tasks of the ROP unit.

2.1 The central detector readout processor

The ROP is a dual processor system that combines the fast handling of the CTD data with more sophisticated functions for monitoring and calibration of the central detector electronics.

The ROP is a four-unit CAMAC module containing a data formater processor and a control processor (fig. 2).

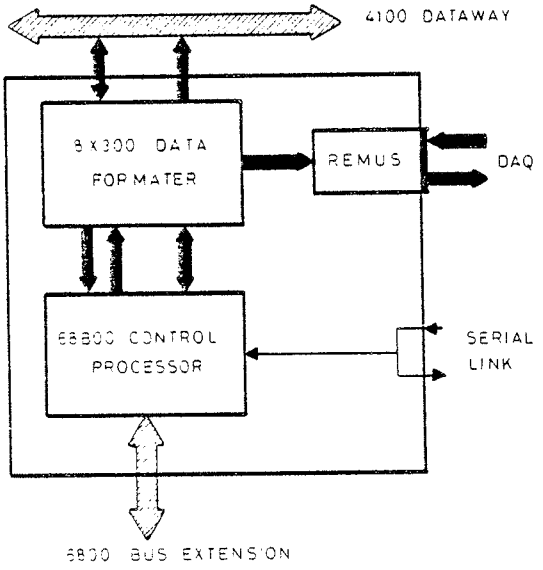

Fig. 2 ROP block diagram

The data formater (DF) is based on the 8-bit Signetics 8X300 microprocessor (250 ns cycle) with instruction word extended to 24 bits to define bus-source and bus-destination addresses and a few direct actions. Its hardware comprises 256 24-bit control store memory locations, two 16-bit summing registers, a 4K 12-bit look-up table, a 1K 16-bit Remus port output FIFO, and a variety of registers for control, status, and data communication. The control processor (CP) is based on the 68B00 microprocessor with 8K RAM, 24K EPROM, 4 DMA channels, an advanced data-link controller (ADLC) port[4], and parallel input/ouput to communicate with the DF and the module front-panel.

The two processors play complementary roles in the ROP crate system. The DF acts as the input/output processor for data acquisition, while the CP supervises the crate operations testing all the internal module functions, bootstrapping and controlling the DF programs, and monitoring the performance of the electronics. The CP has also its own data-handling tasks in order to evaluate the characteristic parameters of each electronics channel and adjust the associated gains and off-sets via on-line calibration procedures.

2.2 Central detector data re-formating

During data acquisition each ROP crate accepts Trigger, Clear, and Read signals from the experimental logic. At the occurrence of a first-level trigger, the CTD digitizers are stopped by the beam-crossing signal delayed by 4 μs; then, if the event is accepted by the second level of decision, a Read signal starts the CTD scanning and the data formating process. All these operations are executed in parallel on all the ROP crates under the control of the DF processors.

The more important data-reduction algorithms at present implemented in the DF software are the 'unpacked data format' and the 'packed data format'.

CTD unpacked format

The DF initializes the CTD 0-skipping procedure. A fast search for a non-zero time tag is done by the CTD at a rate of 4 μs per wire. For each pulse found, a two-byte hit header word is created, packing the drift time and wire address followed by a variable length data block containing the CTD module number and the current division and dE/dx samples associated with the pulse, the end-of-pulse being detected by a comparison of the dE/dx sample with a given threshold.

All processed data are output into the Remus 1K data FIFO and are optionally sent, together with wire statistics information and error flags, to the CP for monitoring and local data sampling.

The number of bytes generated by each hit depends on the pulse length and the chosen end-of-pulse threshold. The average hit length is of the order of 20 bytes. Typical events produce up to 100 hits per crate, corresponding to about 2000 bytes. The dead-time of this kind of data reduction is 200 μs per hit.

CTD packed format

This format is currently used during data taking. The hit search and header word construction proceed in the same way as for the unpacked format, but the pulse information is reduced by the calculation of the total charges deposited at the two edges of the wire and the pulse duration. By means of the DF look-up table, preloaded with suitable conversion parameters, the dE/dx sample, corrected for its base line shift, is transformed by a quantity proportional to the wire total charge contribution of the sample. In the same manner the current division measurement, weighted with the corresponding dE/dx sample, gives the evaluation of the charge deposited at one edge of the wire, as given by the following formulae:

$$Q(\text{total}) = \sum \{B(1-A)(F_i-BL)/[(63-BL)(63-AF_i)]\}$$

$$Q(\text{left}) = \sum \{Z_i B(1-A)(F_i-BL)/[(63-BL)(63-AF_i)]\}$$

(sum over the pulse samples),

where Z_i and F_i are the current division and dE/dx samples, A and B are fixed parameters defining the non-linear response of the dE/dx FADC channel, and BL is the adjustable base line of the dE/dx channel. The charge integrals

are accumulated over the pulse samples until an end-of-pulse is found or when a given number of samples have been added (usually eight, corresponding to 256 ns).

The total hit information produced with this format consists of a minimum of six bytes containing the drift time, the wire and CTD module number, the Q(total) and Q(left) charges, and the pulse length expressed in number of samples. For long pulses the charge evaluations are repeated every eight samples, and an additional four bytes are output. The time needed to process a single hit is of the order of 30 to 100 μs, depending on the length of the signal. For events with up to 100 hits per crate the reduction dead-time varies from 3 to 10 ms.

3. Data Readout

The complete UA1 readout system consists of about 200 crates housed in a mobile electronics control room near the experimental apparatus. All front-end data digitizer electronics are allocated in CAMAC crates; however, only the calorimeters and trigger information readout (ADC, TDC, scalers) use standard CAMAC, whilst the central detector CTD crates run the ESONE COMPEX protocol.

The data collection is performed using the CERN Romulus/Remus method of reading CAMAC[5]. This system is based on two types of CAMAC modules: the branch driver (CERN type 243) and the crate controller (CERN type 244 and the ROP processor). These units connect crates together in branches (vertical bus) organized in a tree-like network, always terminating with a single branch driver sitting in a standard CAMAC crate. The V-bus essentially carries the data stream from the front-end to the branch driver. Crates are read autonomously; markers and word counts are generated to format the data, in this way minimizing the software and hardware overheads during a computer DMA transfer.

To increase the flexibility of the system and improve the performance of the readout, the V-bus data handling was extended with the addition of two auxiliary Remus modules: the Remus Router Unit (RRU) and the Remus Data Buffer (RDB).

3.1 Data Flow and System Partitioning

By means of a RRU the data flow can be switched between two separate V-bus highways, so that the complete system can be partitioned off in a set of independent data-acquisition subsystems which are synchronously or asynchronously triggered.

Alternatively, one V-bus can spy the data whilst they are being read out by the second one performing as master. Local processors can thus access the data in parasitic mode for monitoring purposes, without affecting data acquisition.

This data-routing strategy is applied at two levels. Near the front-end electronics, CAVIAR microcomputers[6] are used as local processors for each individual branch of the detector. During the assembly and development of the apparatus, the CAVIARs are used to perform test and debugging functions, whilst during data acquisition they run monitoring and display programs without altering the front-end data in any way.

The data-routing technique is applied at a second level to the collection of the complete event data in the main control room. This allows the various computer systems to sample data from a full event record simultaneously.

3.2 Parallel Readout

The V-bus is read in an autonomous mode, by means of a buffer unit, and event data are temporarily stored in a dual port memory operating as a FIFO, 4K or 16K deep. The buffer stores all the V-bus data and control bits at the speed of 1 μs per word, so many event data blocks can be pipelined without losing their original data structure, whilst the data readout continues at the output port driven by the subsequent elements of the V-bus tree. The input triggers are counted in each memory, and the results from all memories are compared during output to verify that all data blocks are synchronized on the same event. Through input control signals, the buffer can operate in single event, multievent, or transparent mode, and further triggers are inhibited by a Busy output signal during the upstream data reading.

The block diagram of the UA1 V-bus structure is represented in Fig. 3. All the digitizer crates are grouped in 30 sub-branches, each driven by a buffer unit. The partition of the crates and the size of the memories were chosen in such a way as to have a total storage capacity of up to four events with an average distribution of data per branch of 2000 bytes for typical events of 60,000 bytes.

At this level the data acquisition runs in parallel, taking a total time of the order of 1 ms. The data reduction time being 3 to 10 ms according to the trigger, the full experiment electronics dead-time is 4 to 10 ms, allowing maximum peak rates of 200 and 100 events per second.

The computer readout procedure and the event data structure are not affected by the parallel readout. The latter can be switched off by setting all buffer units in transparent mode. The data taking can continue as before but with the experiment dead-time limited by the full event computer reading.

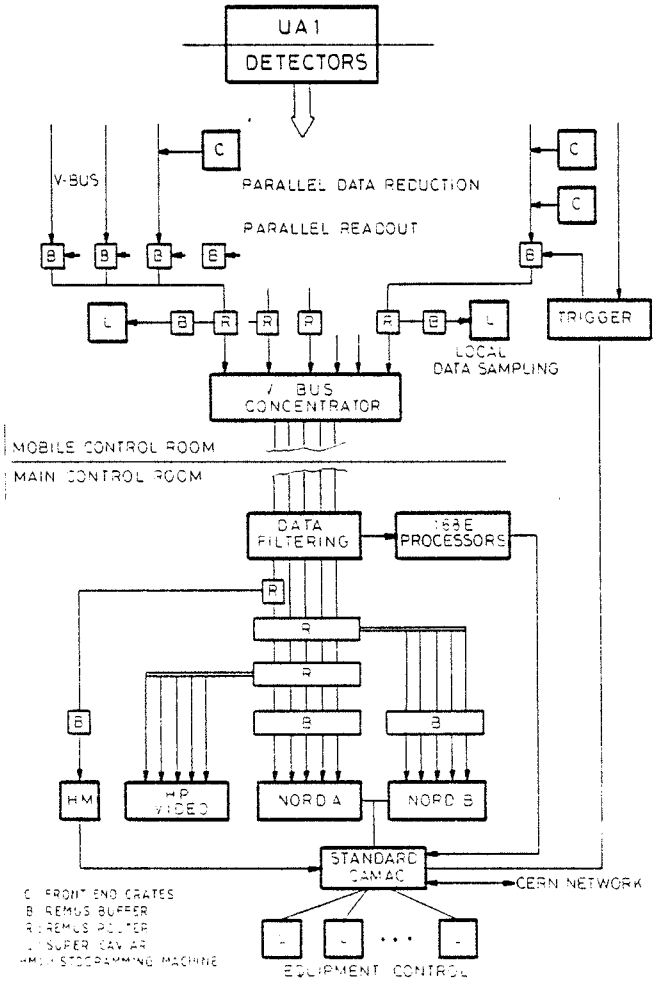

Fig. 3 UA1 data-acquisition block diagram.

3.3 Data Collection

After the first stage of parallel readout, data are collected and merged into five branches and transmitted to the Main Control Room, one hundred metres away. The long-distance transmission causes a slowing down of the data rate to 0.75 Mbyte/s per single branch (3.7 Mbyte/s when the five branches are read in parallel). Before terminating in the data-acquisition computer, the main data stream goes through different levels of routers, each one driven by a large memory buffer of 64 kbytes operating this time in single event mode and allowing a maximum trigger rate of 50 events per second. This last stage of parallel readout allows the same event information to be read by different computers (one acting as master and the others as spy); or, by appropriate dynamical change of the router position, selected event data can be dispatched to different data-acquisition systems in order to increase the over-all experiment maximum data rate to more than 10 events per second and eventually to associate the acquisition of different trigger types with separate computers. It is planned to install the third-level trigger at the top of this structure. This trigger is based on 168E processors[7] that have parallel access to the five main branches via a CAMAC-168E bus interface being developed at CERN.

4. On-line Computers

4.1 The Machines

The UA1 general computing support is based on the Norsk Data ND 100/500 16-bit and 32-bit machines. In addition, three HP21MXE minicomputers are assigned to dedicated functions, such as video-tape mass storage, mass histogramming, and luminosity chamber data acquisition. A set of CAVIAR and SUPER CAVIAR microcomputers are responsible for the control and monitoring of all the equipment. The CERN standard link (CERNET) provides the communication with the CERN central computer facilities and with a remote Megatek interactive graphic system driven by a VAX11-780.

4.1.1 The NORD computers. The NORD 100/500-type machine is a new Norsk Data product. As its hardware and software development fell slightly behind the evolution of the experiment, temporary configurations were installed during the first phase of the UA1 run. At present we are converging toward the final configuration, consisting of two identical NORD 100/500 systems with 2 Mbyte memory, STC 6250 bpi 125 ips magnetic tape units, and 75 Mbyte disks. They are referenced as NORD A and NORD B systems and are the main on-line computer support of the experiment.

The NORD 100 runs the multi-user, multi-task virtual memory operating system SINTRAN III, allowing standard real-time programming and the implementation of direct tasks associated with hardware interrupts. The NORD 500 is a powerful 32-bit processor equivalent to a 0.3 IBM/370 168. It runs in multi-user mode and has the NORD 100 as front-end.

A CERN-developed package (DAS) performs all the basic operations of data taking, namely the system initialization, the CAMAC readout, the magnetic tape recording and replay, the communication with the data sampling programs, the error handling, and the production of run summaries for the bookkeeping. The over-all system is fast and efficient, and its speed is essentially limited by the hardware.

A data base is installed on the two machines for the purpose of having a common mechanism for storing and retrieving the information concerning the apparatus parameters and the experiment running conditions.

Several multi-video terminals (MVIT)[8] provide the machine/operator interface during the experiment. The MVIT is a 6800 microprocessor terminal developed in UA1; it consists of a keyboard, four alphanumeric video signal outputs, and a touch panel. The status information is presented as histograms on four CRTs, scrolling text in selected frames of the screen or as horizontal circular messages, whilst inputs are chosen from a menu list by programmable touches.

4.1.2 NORD system general tasks. The identical configuration of the two NORD systems and the common access to CAMAC allow any task and program running in one machine to be, in principle, transportable to the other, thus providing a continuous functional back-up. However, the two systems play different roles according to the running condition of the experiment. The function of each machine is defined by its task configuration. The definition and the function assignation of each computer system are still in an evolutive state, and more experience with the data handling and the on-line use of the 168E processors is needed for a definitive consolidation of the over-all system. Listed below are the more general hardware and software configurations foreseen for the NORD computers.

Data-taking and experiment monitor[9]

The NORD 100 of system A runs DAS as master; it reads CAMAC and writes tape. Only very efficient and consolidated tasks are activated; they provide a check of the readout system, a monitor of the trigger and collide performances, and a first data analysis based on the energy deposition in the calorimeters. Full event analysis with accumulation of physical result statistics is done at the same time on the NORD 500 A. The NORD 100 of system B runs DAS in spy mode, servicing a variety of user-developed data-sampling programs for display, monitoring, alarm, and supervision of the distributed intelligence controlling the detectors' equipment. The remote VAX11-780 graphic station is serviced as well. During this phase, the NORD B is the real host-computer system. If one of the computers hangs up because of an unrecoverable failure, then all its tasks or a subset are moved to a single machine that will carry on the data acquisition but with limited efficiency.

High-luminosity, dual trigger data taking

When running at high luminosity it seems convenient to separate the trigger into two classes: the 'few' trigger and the 'many' trigger, these being the two trigger selections made either at the first level of hardware logic decision or at the level of 168E filter processors. To increase data-taking efficiency to the maximum, the NORD B system is devoted to the prior collection of the 'few'-type events. A trigger supervisor processor controls the data routing between the two computers according to the incoming trigger type and monitors the 'many' trigger dead-time in order to keep its rate lower than the data-recording saturation of the NORD A, thus always allowing free space in the parallel readout FIFOs for the acquisition of 'few'-type event data.

Calibration and maintenance

By setting the Remus Router Units, the readout can be split into a large set of independent subsystems for hardware maintenance. Calibrationwise, the UA1 detector can be divided into two parts: the calorimeter and the image chamber. At the level of computer data collection, the over-all system is partitioned off into two independent ones by setting the calorimeter branch router, NORD A being used to calibrate hadron and electromagnetic calorimeters and NORD B to calibrate the central detector via the SUPER-CAVIAR ROP controller.

Off-line preprocessing

It is foreseen that the off-line DST tape production will run on NORD A, using the NORD 500 machine and

the 168E processors; the NORD B system is devoted to program development and apparatus maintenance.

4.2 Dedicated Tasks

These functions are taken away from the main computers in order to off-load their charge. They are still activated and controlled by the NORD B computer, but their execution is performed by separate processors.

4.2.1 Luminosity chamber data acquisition. The UA1 luminosity monitor runs as an experiment apart. The data acquisition is performed by a CERN standard HP21MXE system using its own CAMAC readout and magnetic tape storage. A CAMAC-to-CAMAC link provides communication between the luminosity monitor and the host computer.

4.2.2 Histogramming machine (HM). The histogramming and the average and sigma calculations are the simplest tools for evaluating the performance of a data channel such as an ADC. Histogramming is a time- and memory-consuming task that can become very heavy for a multi-user computer system such as the NORD when the number of channels and events to be treated in a short time is high. The UA1 calorimeter detectors consist of 7500 ADC channels, and their calibration procedures need the accumulation of several hundred events taken with different external conditions (simulation pulses, laser flashes, etc.).

At the beginning of the experiment it was thought necessary to provide additional histogramming facilities in the main computers. In the case of the central detector readout, these were included in the design of the system, and for the ADC channels a HP21MX minicomputer (HM) with 384 kbyte memory was completely dedicated to the task of mass histogramming.

The HM runs a software optimized for fast histogramming and statistics parameter evaluation, allowing the filling of one thousand histograms at the rate of 10 events per second, or the first and second moments calculation of 7500 channels taking one second per event[8]. The HM has only access to the calorimeter data via a RRU, and it can operate in spy mode during data acquisition or in master mode during the calibration. The NORD B system communicates with the HM via a serial link. The NORD initializes, books, and reads back accumulated histograms for display and updating of tables of constants. The HM is treated as a peripheral of the NORD computer with a limited and well-defined set of functions. During data taking, the HM role is complementary to that of the main computer, where histogramming tasks are devoted essentially to monitoring the physical information contained in the data.

4.2.3 Mass storage. The data collected by the NORD system are recorded by STC 6250 bpi 125 ips magnetic tape units (MTUs). Owing to the 60 kbyte event size, the MTUs are saturated by a trigger rate of 10 events per second, which fills a reel in four minutes.

When the collider luminosity attains the design value of 10^{30} cm^{-2} s^{-1}, the problem of handling over 200 tapes per day will become serious unless a very selective trigger is used to reduce the event rate.

To provide greater capacity of high-rate data recording, a digital video-tape system[9] has been installed which records data at 1 million bits per square inch by helical scanning. The system is a dual-transport development of a configuration which was successfully employed in ISR experiments R605 and R606[10] and is controlled by an HP21MXE computer. Video-tape data are recorded at 11,000 bpi by Miller code in scanlines of 100 kbits. An interleaved data structure is implemented to avoid requiring a fast disk for intermediate data staging. Scanline addressing and the status information required to log the structure are recorded in separate longitudinal tracks, which can be read at search speeds up to 400 ips.

The video-tape system records 9 Gbyte per reel of tape, equivalent to 50 reels of 6250 bpi tape, and can take data at maximum rate on a single reel for over 3.5 hours of running. It will be brought on line when dual selective/open triggers have been implemented and stable behaviour of the experimental apparatus has been achieved.

4.3 Equipment Control and Monitoring

Microprocessor systems are used for the control of all the equipment associated with detector functions, such as power on/off, parameter setting, current and voltage monitoring, and calibration pulse generation.

The host computer (usually the NORD) is able to interact with these systems via CAMAC, to control their operation, and to communicate with the programs they are running.

4.3.1 General-purpose microprocessor controller (GPMC)[8]. This is a single-unit CAMAC module based on the 6800 microprocessor with 16K EPROM, 2K RAM, RS232 and ADLC ports, and a 6800 bus extension to which is connected an interface module (IM) specific to the device to be controlled. According to the application, each IM replaces a well-defined electronics logic and measuring system that would be expensive to implement with standard CAMAC and NIM modules. Different IMs were developed in order to handle the central detector calibration pulse generation, the very forward chamber (VFC) electronics control, and the central detector high-voltage and current monitor. The GPMC firmware runs an interactive monitor, processing commands coming from CAMAC or the RS232 port, the command firmware depending on the IM application.

4.3.2 CAVIAR and SUPER CAVIAR microcomputers. CAVIAR is a CERN-developed stand-alone microcomputer which is used extensively in the laboratory and associated institutes for CAMAC system development, monitoring, and control.

It is an integrated microcomputer system based on the 6800 microprocessor and 9511 floating-point arithmetic and function processor, and the standard unit incorporates 32K RAM, 29K EPROM, a EUR 4600 CAMAC branch driver, an IEEE 488 GPIB controller, an audio cassette interface, two RS232 communication ports, and a raster-scan video monitor with alphanumeric and graphic capability.

The SUPER CAVIAR[11] enhancement includes a memory mapping system, 256K RAM, up to 85K EPROM, an ADLC port, and a real-time clock. Multipage colour graphics are currently being developed.

SUPER CAVIAR firmware includes BAMBI, a high-level interactive programming system with a language similar to BASIC but which uses pre-run compilation to achieve execution speeds substantially faster than BASIC interpreters. The system incorporates a comprehensive range of over 200 assembly-written routines for CAMAC, GPIB and ADLC operations, graphics, histogramming, array handling and remote computer communications.

The main control room CAVIARs and SUPER CAVIARs are the primary interactive interface facilities between the operators and the UA1 experiment complex. They allow direct control and monitoring of the experimental apparatus by keyboard commands or easily written programs, and operate autonomously on the equipment connected to their CAMAC systems. However, each CAVIAR system is seen by the host computer (Fig. 4) as a CAMAC device with which it can communicate programs, data, and control functions for the supervision of the status of all the apparatus.

CAVIARs or SUPER CAVIARS are employed for the following control, monitoring, and development tasks in UA1:

central detector high-voltage, gas, and temperature;

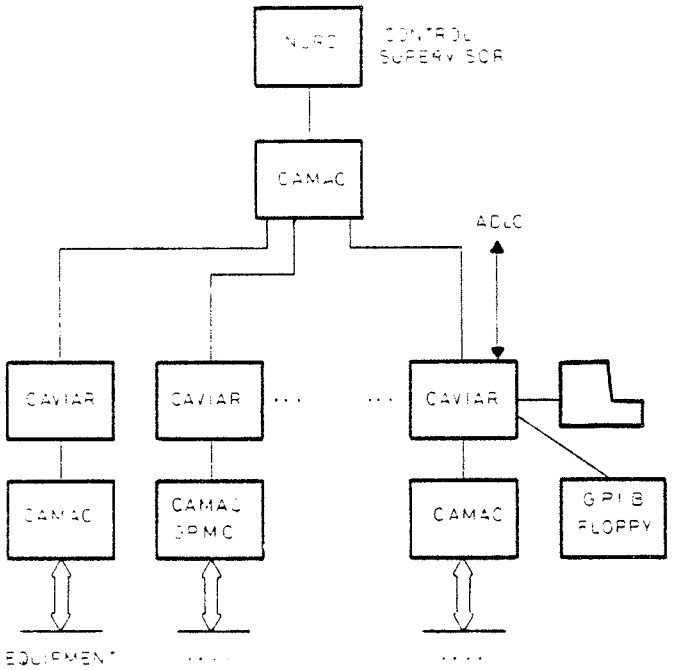

Fig. 4. Configuration of CAVIARs for equipment control.

central detector transient recorder monitor;
central detector ROP control and calibration;
central detector electronics testing (four units);
photomultiplier power supply[12];
trigger processor control;
experiment and collider status;
magnet control;
electronics test and development;
readout setting and control;
local data sampling and monitoring (seven units).

In addition, the spin-off from the CAVIAR program (MVIT, GPMC, ROP development system, electronics production test system) has resulted in a somewhat unified approach to this first large-scale application of microprocessor systems to a complex experimental facility.

4.3.3 Local area network. A simple and cheap serial data-link was developed in order to provide an independent control and data communications path to all the distributed intelligence associated with the front-end electronics, such as the central detector ROPs and the very forward detector GPMC electronics controllers. This local area network is based on the 6854 advanced data-link controller (ADLC)[4] using a data communication protocol based on HDLC. The network is organized as a set of closed loops, each having a SUPER CAVIAR primary station and up to 254 secondary stations (ROPs). Via the ADLC link the SUPER CAVIAR can read or write variable length data blocks at specified addresses in each ROP control processor RAM or send specific commands for initialization, internal calibration, and selection of the ROP data-acquisition mode.

5. Conclusion

The UA1 experiment started taking data at the CERN $p\bar{p}$ collider during the second half of 1981. The major part of the basic software and hardware elements of the data acquisition system was installed and running. During the latest data-taking period in December 1981, half a million events were read and written onto tape.

The experience accumulated so far has shown that microprocessor-based devices play a central role in large and complex experiments such as UA1. Remus CAMAC readout enhanced by the parallel processing, buffering, and partitioning facilities performs satisfactorily at the present scale of the experiment.

However, when introducing multiprocessor facilities for the third-level trigger implementation, the lack of a modular event data-staging structure is felt. Intermediate solutions have been adopted for the near future, whilst FASTBUS would appear to be the most feasible long-term scheme for the event data-collection stage of the system.

Acknowledgements

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