Evaluation of Data Transmission at 80 MHz and 160 MHz Over Backplane, Copper and Optical Links

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Abstract

The bunch clock frequency of the LHC accelerator at CERN is specified as 40.07897 MHz [1]. Most of the LHC experiments will utilize this frequency, its multiples or derivatives as the main frequency of data transmission for their synchronous Trigger and DAQ electronic systems. For example, the triggering system of the Cathode Strip Chamber (CSC) sub-detector at the CMS experiment comprises the on-chamber anode and cathode electronics, the off-chamber boards housed in 9U crates mounted on the periphery of the Endcap iron disks, and one Track Finder (TF) crate located in the underground counting room (Fig.1). Due to the significant amount of data from the front end, the trigger patterns are multiplexed and sent from the CSC chambers over copper cables using the LVDS standard at 80 MHz. For the same reason the data patterns transmitted over backplanes in the peripheral and TF crates are also multiplexed and sent at 80MHz using the GTLP standard. Optical links from the peripheral crates to the TF are operated at 80 MHz as well. Finally, the parallel LVDS links to the Global Muon Trigger (GMT) run at 40 MHz.

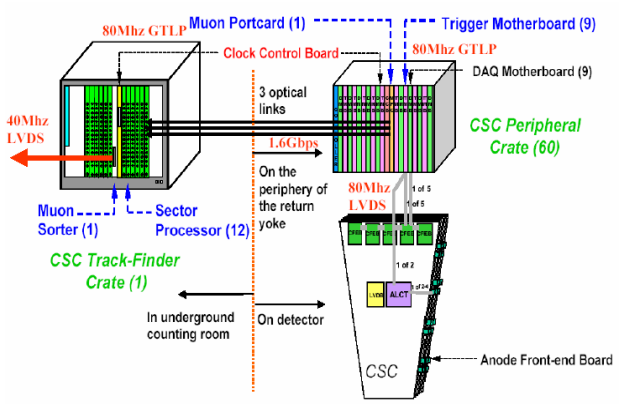

Figure 1: CSC Trigger Electronic System

A proposed Super LHS (SLHC) upgrade [2] would increase the operating frequency of the accelerator, and be challenging for many synchronous data transmission systems. The goal of this work was to evaluate possible solutions for data transmission at 80 MHz and 160 MHz suitable for the SLHC era. We have used an existing hardware designed for the CSC electronic system for evaluation of data transmission at 160 MHz using the LVDS and GTLP logical standards. We have designed a new evaluation board to study the optical links operating at 160 MHz. The results of measurements and possible solutions are presented.

I. GTLP Backplane Interface

Gunning Transceiver-Logic Plus (GTLP) is a widely used logical interface for point-to-point and bussed data transmission over backplane. Within the CSC electronic system it is used for the point-to-point transmission in the peripheral and TF crates at 80 MHz. The total number of data sources is 288 (9 boards) in the peripheral and 384 (12 boards) in the TF crate. The boards that receive all these signals reside in the middle of each crate (the Muon Port Card (MPC) [3] in the peripheral and the Muon Sorter (MS) [4] in the TF crate). Both backplanes also utilize a 40 MHz control GTLP bus. The TF backplane is a 6U, 21-slot multiplayer custom board residing in the 9U crate below the J1 part of the VME64x backplane. A pairs of Texas Instruments SN74GTLPH16912 transceivers are used in the TF crate and pairs of National Semiconductor GTLP16612 driver and Fairchild GTLP18T612 receiver are used in the peripheral crate.

There are three parameters that may be adjusted to optimise the GTLP performance: termination resistance Rt, termination voltage Vt, and a reference voltage Vref for GTLP receivers. Termination resistors of 56 Ohm for all point-to-point GTLP lines are located on the receiver boards (MPC and MS) while the 100 Ohm terminations for a control bus are located on both ends of the custom backplane. The termination voltage is provided from a custom backplane and fixed at +1.5V. The reference voltage Vref can be adjusted (0.9V… 1.1V) with a potentiometer on a receiver board. We found that the best performance (duty cycle close to 50% and widest “safe window”) is achievable with the Vref=0.9V.

In both backplanes the main master 40 MHz clock is distributed to all slots over individual LVDS lines of equal length from a common source, the Clock and Control Board (CCB) [5]. This board carries a mezzanine TTCrq card that is an interface to LHC Timing, Trigger and Control system [1].

All the peripheral and TF boards are based on various Xilinx FPGA devices. They produce internal 80 MHz clocks by doubling the master CCB clock. These 80 MHz clocks are well aligned on all trigger boards and are used to send data to the MPC and MS. After GTLP-to-LVTTL conversion on the MPC and MS boards an input data patterns are clocked in into the FPGA on adjustable 80 MHz clock produced by the DLL or DCM modules in the FPGA. The fine clock adjustments can be as low as 100..250 ps.

We have chosen the MS board for evaluation purposes. The main Xilinx Virtex-2 FPGA on the MS receives as many as 384 80 MHz data bits, performs sorting “4 best tracks out of 36” and transmits the four best selected patterns to the

GMT receiver. Existing MS firmware is based on demultiplexing of all incoming signals down to 40 MHz and further processing and transmission at 40 MHz. The average "safe window" of clocking data in into the FPGA while all 32 sources (on one board) and 384 sources (on all 12 boards) are sending their 80 MHz data patterns was measured as 8.0 and 6.5 ns respectively. The factors that affect the "safe window" are: variations in signal propagation from slot to slot (can be as large as 2 ns), chip-to-chip and channel-to-channel delay variations, delay changes within the transceiver with a number of switching channels, and non-ideal line termination. In overall, we found that the "safe window" of 6.5 ns is sufficient to provide a reliable operation at 80 MHz of the fully loaded TF crate.

The maximum operating frequency of the GTLP transceivers is specified as 150 MHz for the GTLP16612 and 175 MHz for other parts mentioned above. We have used a TF custom backplane for evaluation of data transmission at 160 MHz. The 40 MHz master clock from the CCB was replaced with a 80 MHz master clock and the Xilinx Virtex-2 FPGA produced a doubled clock of 160 MHz to clock data out on a transmitter board and clock it in on a receiver MS board. The main question was whether reliable data transmission at 160 MHz from several sources distributed over backplane within acceptable "safe window" is achievable. For evaluation purposes all the MS inputs were considered 160 MHz signals being demultiplexed down to 80 MHz and processed at this frequency. The sorter unit was modified and proven to work at 80 MHz. We found straightforward to double the performance of the Virtex-2 FPGA from 40 MHz to 80 MHz for a given implementation of the sorter logic.

One data source board called the Muon Tester [6] was placed in slot 6 (farthest from the MS which resided in slot 14) and the "safe window" was measured as 1.25 ns. Then another similar data source board was placed in slot 11 (closest to the MS) and the "safe window" was measured as 1.15 ns. However, when both of these boards were sending data simultaneously at 160 MHz, no "safe window" could be determined. This is not surprising since the difference in propagation delays between these slots is comparable with the measured "safe window". Even for a single 32-bit source, the "safe window" of 1.15…1.25 ns is only ~20% of the theoretical maximum (6.25 ns at 160 MHz) which is not good enough for reliable operation. So, while selected GTLP transceivers are still capable to transmit and receive data at 160 MHz, for our specific application with several 32-bit backplane sources they do not provide an acceptable solution.

II. LVDS Cable and Backplane Interfaces

The Low Voltage Differential Signaling (LVDS) technology provides a unique combination of very low output voltage swing (350 mV), low power consumption (~1.2 mW per load), high speed (up to 1 GHz) and high noise immunity (since the switching noise cancels between two lines). A current mode LVDS driver requires a termination on a receiver end. Several receivers have an integrated termination resistor to simplify the design. Both point-to-point and bussed LVDS options exist; however, we will focus on point-to-point configurations only.

For evaluation we have used a Muon Sorter board that has four 31-bit output LVDS links and one 31-bit input link (Fig.2). Texas Instruments SN75LVDS387 drivers and SN75LVDT386 receivers with integrated 110 Ohm termination are used. The data was sent out and received by the Xilinx Virtex-2 FPGA residing on a mezzanine board.

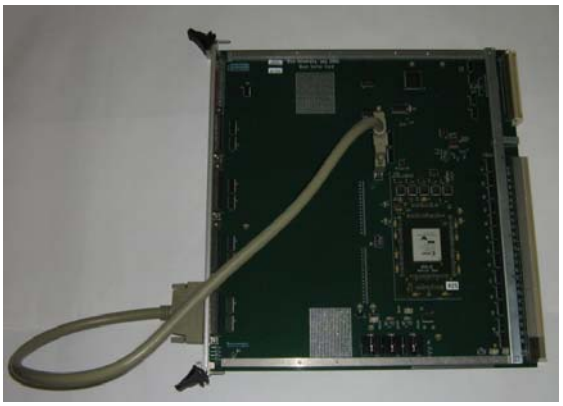

Figure 2: Muon Sorter Board

A Madison Cable 20276 Universal Ultra 320 SCSI 30 AWG 34-pair cable was tested. A non-halogen version of this cable will be used to transmit data from the Regional to Global Muon trigger systems at the CMS. Random 31-bit data patterns were sent out from FIFO_A at 80 MHz or 160 MHz on fixed clock and received after LVDS-to-LVTTL conversion into FIFO_B on an adjustable 80 MHz or 160 MHz clock (Fig. 3).

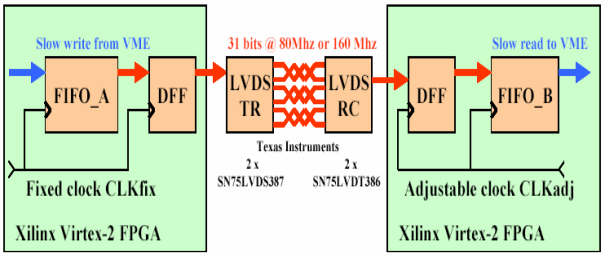

Figure 3: LVDS Testing Setup

It was found that for a 0.9 m cable the "safe window" of clocking data in into FIFO_B was 10.2 ns at 80 MHz and 3 ns at 160 MHz. For a longer 12.7 m (500 in) cable the "safe window" was measured as 9.6 ns at 80 MHz and 3 ns at 160 MHz. We consider these results as perfect for data transmission at 80 MHz and acceptable at 160 MHz. As was mentioned in section I, for a single 32-bit GTLP source link, the "safe window" was measured to be 8.0 ns at 80 MHz. The differential attenuation for a given cable is 0.09 dB/ft at 80 MHz and 0.129 dB/ft at 160 MHz. Allowed attenuation for a given LVDS chipset can be calculated as 20log(100mV/247mV) = -7.9 dB (where +/-100mV is a receiver input threshold and 247 mV is a minimum output voltage magnitude). So, based on allowed attenuation, the maximum cable lengths can be estimated as 26.4 m for data transmission at 80 MHz and 15.5 m for data transmission at 160 MHz. A skew between differential pairs (25 ps/ft

maximum for a given cable) would be below 2.2 ns and 1.2 ns respectively for these lengths.

LVDS backplane or cable links can be used as an alternative to GTLP at 160 MHz. Separate cables from each of 12 source boards in the TF crate can be easily made of equal length to avoid the differences in signal propagation from slot to slot. High density connectors (for example, from Samtec) and the Amphenol Spectra-Strip flat twisted pair cable can be used. For a backplane implementation, families of 5-, 6- or 8-row connectors for differential signaling are available from several vendors, for example, Teradyne VHDM-HSD or FCI Metral series. While the number of signal lines doubles due to the differential nature of the LVDS standard, the number of ground lines can be significantly lower than for the GTLP backplane implementation where a large number of ground pins is required to provide a low impedance path for the return current.

III. Optical and Copper Serial Links

An existing optical link between the CSC peripheral and Track Finder crates is based on the Texas Instruments (TI) TLK2501 gigabit serializer/deserializer (SERDES) and a Finisar FTRJ-8519 optical transceiver. The results of its evaluation at 80 MHz were reported in [7]. However, the Virtex-E FPGA, TLK2501 and FTRJ-8519 optical transceivers do not support data transmission at 160 MHz. We have decided to evaluate another TI device, the TLK3101 [8] and a higher speed Finisar optical transceiver, the FTRJ-8524 [9] (Fig. 4). The FTRJ-8524 transceiver supports data transmission up to 4.25 Gbps. The TLK3101 however is only rated up to 3.125 Gbps, so one of our main goals was testing at the slightly higher data rate of 3.2 Gbps. The internal core and inputs and outputs of the chosen FPGA (Virtex-2 XC2V250) can reliably operate at 160 MHz. An evaluation board [10] with two optical links was designed and built (Fig. 5).

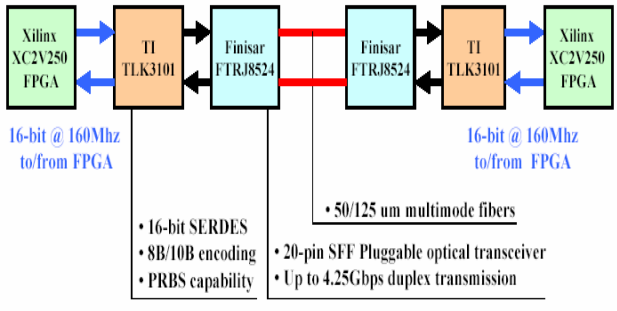

Figure 4: Optical link under evaluation

Our evaluation board carries a TTCrq mezzanine card [11] with the QPLL ASIC which provides one of the sources of 160 MHz clock for the TLK3101 devices and FPGA. The other sources of clock signal for the serializers are an on-board oscillator and the output from an external generator. Both links are identical, independent, duplex and fully controllable via VME. For each link the 16-bit data patterns can be loaded into FIFO_A buffer inside the FPGA and sent out to the TLK3101 TXD[15:0] lines upon VME command. After serial-to-parallel conversion, the RXD[15:0], RX_ER, and RX_DV lines are clocked in into the FIFO_B on recovered RX_CLK signal individually for each link. All FIFO buffers are 511-word deep and available for write and read over VME.

Figure 5: Evaluation Board

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Our tests were conducted with random patterns transmitted from FIFO_A and verified at FIFO_B (Fig. 3) as well as with the Pseudo Random Bit Stream (PRBS) pattern generator embedded into the TLK3101 devices. The data patterns were transmitted between two links on each board and between 4 links on two boards, with optical fibers of 5 m and 100 m length. We ran transmission tests of various configurations for several hours. The results of measurements of the Bit Error Rate (BER) are summarized in Table 1.

Table 1: Results of Measurements

Clock Source	Frequency, MHz	Bit Error Rate (BER)
Epson EG-2101-CA oscillator (peak-to-peak jitter ~ 25 ps)	155.52; 161.132	$< 10^{-14}$ (PRBS), $<10^{-9}$ (Data)**
QPLL ASIC on TTCrq mezzanine board (peak-to-peak jitter ~ 50 ps)	160.3147	$~10^{-14}$ (PRBS)*, $<10^{-9}$ (Data)**
Cardinal Components CPPHV7-A7BC programmable oscillator (jitter ~ 80 ps)	160.3147	$~ 10^{-10}$ (PRBS)
Xilinx XC2V250 Digital Clock Manager (peak-to-peak jitter ~ 250 ps)	40…160	$~ 10^{-9}$ (PRBS)

* 3 errors observed, ~2.3×10^{14} bits transmitted

** Random patterns transmitted from FIFO_A to FIFO_B

A low-jitter (~25 ps peak-to-peak) clock from an EPSON EG-2101-CA oscillator provided an error free data transmission within several hours of operation. The 160 MHz clock from the QPLL is marginal, and the other two clocks, from the programmable oscillator and the Digital Clock Manager of the FPGA are unacceptable due to large jitter.

We have investigated whether the BER depends on the power supply voltage on the TLK3101 parts. While according to the specification, the supply voltage may vary between 2.3V and 2.7V with a typical value of 2.5V, we found that error free data transmission is achievable if the supply voltage is above 2.42V and within the specified range.

We also measured the total link latency. Due to silicon process and implementation variations the total link latency for both TLK3101 serializer and deserializer may vary between 110..145 bit times, or 34..45 ns at 160 MHz. Our measurements conducted at room temperature and 2.5V power for six TLK3101 parts indicated that the total link latency is between 40 and 43 ns at 160 MHz. While the exact value is different at each link initialization in increments of the serial bit clock (310 ps), it has never varied more than the 3 nanoseconds total.

A Molex 73929 SFP copper patch cable as a replacement of Finisar optical modules was also tested. This 5 m long part is made of Amphenol Spectra Strip Skewclear cable with two shielded parallel pairs. The attenuation is 0.57 dB/m at 1.562 GHz and the skew within pair is only 7.14 ps/m. We haven't seen any errors in data transmission test with PRBS patterns within 48 hours, so the BER is below 10^{-14}. Reliable transmission over longer cable can be achieved with the cable equalization using, for example, 3.2 Gbps Maxim MAX3800 Adaptive Equalizer and Cable Driver.

IV. Conclusion

As we have seen, existing GTLP parts can not provide reliable data transmission from multiple (as many as 400) distributed backplane sources at 160 MHz. Cable and backplane LVDS point-to-point links may be a good alternative solution. Reliable operation of the 31-bit LVDS link was demonstrated over 12.7 m long Madison 20276 cable at 80 MHz and 160 MHz.

Based on our experience with three identical evaluation boards (6 links total) in laboratory conditions we can conclude that the TLK3101 devices may provide reliable data transmission at 160 MHz over up to 100 m of 50/125 um multimode optical fiber (with the Finisar FTRJ-8524 optical transceivers) and over 5 m Spectra Strip Skewclear copper cable without equalization. A low jitter (less than 40 ps peak-to-peak) clock for the serializer must be provided. With various clock options, our board can be used for evaluation of other pluggable optical and copper modules as well as for pre-selection of the TLK3101 parts, if required.

Embedded FPGA serializers and deserializers may provide a good alternative to discrete devices like the TLK SERDES available from TI. However, they have a longer latency than the TI TLK devices. Among attractive features of the newest Xilinx FPGA family, the Virtex-4, are up to 24 duplex channels capable to serialize and deserialize data at 106...644 MHz.

V. References

[1] B.G.Taylor. Timing Distribution at the LHC. Available at http://www.cern.ch/TTC/LECC02.pdf

[2] Wesley H. Smith. Trigger and Data Acquisition for the Super LHC. Available at http://lhc-workshop-2004.web.cern.ch/lhc%2Dworkshop%2D2004/1-Plenary%20sessions/6-smith_proceedings.pdf

[3] CMS EMU Muon Port Card Specification. Available at http://bonner-ntserver.rice.edu/cms/MPC2004P.pdf

[4] The MS2005 Muon Sorter Specification. Available at http://bonner-ntserver.rice.edu/cms/MS2005.pdf

[5] The Clock and Control Board Specification. Available at http://bonner-ntserver.rice.edu/cms/CCB2004P.pdf

[6] The Muon Tester Board MT'2004 Specification. Available at http://bonner-ntserver.rice.edu/cms/MT2004.pdf

[7] M.Matveev et al. Optical Link Evaluation for the CSC EMU Trigger at CMS. Available at http://lhc-electronics-workshop.web.cern.ch/LHC-electronics-workshop/2001/posters/matveev2.pdf

[8] http://focus.ti.com/lit/ds/symlink/tlk3101.pdf

[9] FTRJ8524P2xNy Product Specification. Available at: http://www.finisar.com/optics/documents/FTRJ8524P2xNySpecRevH.pdf

[10] Optoboard160 Specification. Available at http://bonner-ntserver.rice.edu/cms/opto160.pdf

[11] The TTCrq Manual. Available at: http://proj-qpll.web.cern.ch/proj-qpll/images/manualTTCrq.pdf