Muralidhar Talupur

CURRENT POSITION

Research Scientist
Strategic CAD Labs
Intel Corporation

CONTACT INFORMATION

RA2-451
Intel Corporation
Hillsboro, OR-97124

Voice: 971-214-1680
Fax: 971-214-1771
E-mail: murali.talupur@intel.com

EDUCATION

Carnegie Mellon University Pittsburgh, PA
Ph.D., Computer Science, **September 2006**
Thesis Topic: Abstraction Techniques for Parameterized Verification
Advisor: Prof. Edmund Clarke

Carnegie Mellon University Pittsburgh, PA
M.S, Computer Science, **December 2002**
Advisor: Prof. Edmund Clarke

Indian Institute of Technology-Madras, Chennai, India
B.Tech, Computer Science, **June 1996 - June 2000**
Thesis Topic: Generative Power of Splicing Systems
Advisor: Prof. Kamala Krithivasan

ACADEMIC DISTINCTIONS

Secured 35th rank in JEE-96, the entrance examination to the Indian Institutes of Technology, which was taken by over 100,000 students all over India.

Awarded fellowship by the School of Computer Science, Carnegie Mellon University.

Received Best Paper Award at FMCAD 2008, one of the premier verification conferences.

Solved a well known open problem in DNA computing as part of Undergraduate thesis.

Secured Merit Prize in State level Junior's Math Olympiad.

RESEARCH EXPERIENCE

Worked on various aspects of Formal Verification including BDD and SAT based model checking, Abstraction Interpretation, Parameterized Verification, and Compositional Reasoning.

Developed a compositional reasoning and abstraction based technique that has been successfully applied to formally and parametrically verify the latest cache coherence protocols being developed at Intel.

As an under-graduate, gave a new characterization for context free languages in terms of a well known splicing based system called *EH(FIN, p[1])* (see Gh. Paun, G. Rozenberg, A. Salomaa, DNA Computing, Springer, 264-266)

INDUSTRIAL EXPERIENCE

Naval Research Laboratory, Washington, DC, USA
Summer Intern **Jun 03 - Aug 03**
Worked on automatic test generation from high level *SCR* specifications using model checkers. Studied the performance of different model checkers in the test generation scenario

NEC Laboratories America, Princeton, NJ, USA
Summer Intern **Jun 04 - Aug 04**
Worked on efficient decision procedures for a fragment of first order logic called *Difference Logic*. Devised a new algorithm for reducing the domains of variables while preserving satisfiability of separation logic formulas.

Strategic CAD Labs, Intel Corp, Hillsboro, OR, USA
Research Scientist **Dec 06 – Present**
Working on developing efficient algorithms for formally verifying the various distributed protocols that are used in a multi-core processor.

TEACHING EXPERIENCE

Teaching Assistant. Formal Languages, Automata and Combinatorics (15-453). Spring 2002, Carnegie Mellon University

Teaching Assistant. Constructive Logic (15-399) Spring 2004, Carnegie Mellon University

PUBLICATIONS

John O'Leary, Murali Talupur, Mark Tuttle. *Protocol verification using message flows: An Industrial Experience.* To appear In Proceedings of International Conference on Formal Methods in Computer Aided Design (FMCAD) 2009

David James, Time Leonard, John O'Leary, Murali Talupur, Mark Tuttle. *Brief Announcement: Extracting models from design documents with Mapster.* In Proceedings of 27th Annual ACM Symposium on Principles of Distributed Computing (PODC) 2008

Murali Talupur and Mark R. Tuttle. *Going with the Flow: Parameterized Verification using Message Flows.* In the Proceedings of the International Conference on Formal Methods in Computer Aided Design (FMCAD) 2008 (***Best Paper Award)***

Murali Talupur, Helmut Veith. *Domain Pattern Abstraction + Ptolemaic Abstract Domains = Environment Abstraction for Concurrent Systems.* In the 2nd International Workshop on Exploiting Concurrency Efficiently and Correctly (EC2) 2008

Murali Talupur, Sava Krstic, John O'Leary, Mark R. Tuttle. *Parameterized Verification of Industrial Cache Coherence Protocols.* In the 8th International Workshop on Designing Correct Circuits (DCC) 2008

Edmund Clarke, Muralidhar Talupur, Helmut Veith. *Proving Ptolemy Right: The Environment Abstraction Principle for Model Checking Concurrent Systems.* In Proceedings of International Conference on Tools and Algorithms for Construction and Analysis of Systems (TACAS) 2008

Edmund Clarke, Flavio Lerda, Muralidhar Talupur
An Abstraction Technique for Real-Time Verification.
In Proceedings of the GM R&D Workshop on Next Generation Design and Verification Methodologies for Distributed Embedded Control Systems, Bangalore, India, January 2007

Edmund Clarke, Muralidhar Talupur, Helmut Veith. *Environment Abstraction for Parameterized Verification*. In Proceedings of International Conference on Verification Model Checking and Abstract Interpretation (VMCAI) 2006.

Malay Ganai, Muralidhar Talupur, Aarti Gupta. *SDSAT: Tight Integration of Small Domain Encoding and Lazy approaches in a Separation Logic Solver*. In Proceedings of International Conference on Tools and Algorithms for Construction and Analysis of Systems (TACAS) 2006.

Kamala Krithivasan, Prahlad Harsha, Muralidhar Talupur. *Communicating Distributed H Systems with Simple Splicing Rules.* Proceedings of the International Conference on Computer Design and Conference on Computing In Nanotechnology (CDES) 2006

Edmund Clarke, Muralidhar Talupur, Tayssir Touilli, Helmut Veith. *Verification by Network Decomposition*. In International Conference on Concurrency Theory (CONCUR) 2004.

Muralidhar Talupur, Nishant Sinha, Ofer Strichman, Amir Pnueli. *Range Allocation for Separation Logic*. In Proceedings of International Conference on Computer Aided Verification (CAV) 2004.

Shuvendu Lahiri, Randy Bryant, Amit Goel, Muralidhar Talupur. *Revisiting Positive Equality* In Proceedings of International Conference on Tools and Algorithms for Construction and Analysis of Systems (TACAS) 2004.

Edmund Clarke, Orna Grumberg, Muralidhar Talupur, Dong Wang. *Making Predicate Abstraction Efficient: how to remove redundant predicates.* In Proceedings of International Conference on Computer Aided Verification (CAV) 2003.

Edmund Clarke, Orna Grumberg, Muralidhar Talupur, Dong Wang. *High Level Verification of Control Intensive Systems using Predicate Abstraction.* In Proceedings of International Conference on Formal Methods and Models for Codesign (MEMOCODE) 2003.

Edmund Clarke, Muralidhar Talupur, Helmut Veith, Dong Wang. *SAT Based Predicate Abstraction for Hardware Verification* Appeared in International Conference on Theory and Applications of Satisfiability Testing (SAT) 2003.

Lakshminarayanan Subramanian, Muralidhar Talupur, Kamala Krithivasan, C. Pandu Rangan. *On the Generative Power of Simple H Systems.* Appeared in Journal of Automata, Languages and Combinatorics, Vol. 5, No. 4, 2000.

Muralidhar Talupur, Kamala Krithivasan. *The generative power of simple H system with permitting contexts.* Submitted to Theoretical Computer Science.

THESES

Muralidhar Talupur. *Abstraction Techniques for Parameterized Verification*.
PhD Thesis, CMU-CS-06-169, Computer Science Department, Carnegie Mellon University, 2006.

Muralidhar Talupur. Generative *Power of Splicing Systems.*
BTech Thesis*,* Computer Science Department, Indian Institute of Technology-Madras, 2000.

TECHINCAL REPORTS

Edmund Clarke, Muralidhar Talupur, Dong Wang. *SAT based Predicate Abstraction for Hardware Verification*.
Technical Report CMU-ECE-CSSI 02-45, CMU, 2002.

Daniel Sleator, Muralidhar Talupur. *Optimal Binary Trees in Online Algorithms*.Technical Report CMU-CS-02-148, SCS, CMU, 2002.