

DESIGN OF THE ILC PROTOTYPE FONT4 DIGITAL INTRA-TRAIN BEAM-BASED FEEDBACK SYSTEM

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Abstract

We present the design of the FONT4 digital intra-train beam position feedback system prototype and preliminary results of initial beam tests at the Accelerator Test Facility (ATF) at KEK. The feedback system incorporates a fast analogue beam position monitor (BPM) front-end signal processor, a digital feedback board, and a kicker driver amplifier. The short bunchtrain, comprising 3 electron bunches separated by c. 150ns, in the ATF extraction line was used to test components of the prototype feedback system.

INTRODUCTION

A number of fast beam-based feedback systems are required at the International electron-positron Linear Collider (ILC) [1]. At the interaction point (IP) a very fast system, operating on nanosecond timescales within each bunchtrain, is required to compensate for residual vibration-induced jitter on the final-focus magnets by steering the electron and positron beams into collision. A pulse-to-pulse feedback system is envisaged for optimising the luminosity on timescales corresponding to 5 Hz. Slower feedbacks, operating in the 0.1 – 1 Hz range, will control the beam orbit through the Linacs and Beam Delivery System.

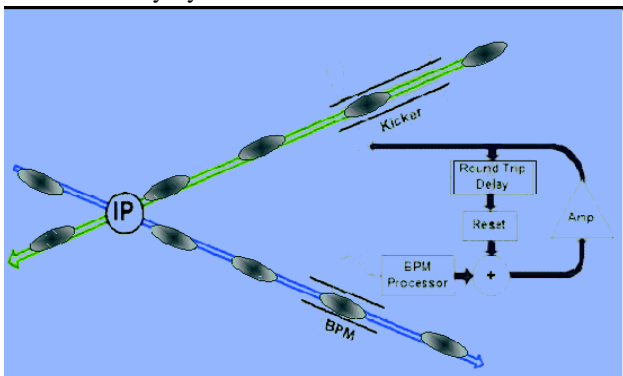


Figure 1: Schematic of IP intra-train feedback system for an interaction region with a crossing angle. The deflection of the outgoing beam is registered in a BPM and a correcting kick applied to the incoming other beam.

The key components of each such system are beam position monitors (BPMs) for registering the beam orbit; fast signal processors to translate the raw BPM pickoff signals into a normalised position output; feedback circuits, including delay loops, for applying gain and taking account of system latency; amplifiers to provide the required output drive signals; and kickers for applying the position (or angle) correction to the beam. A schematic of the IP intra-train feedback is shown in Figure 1, for the case in which the electron and positron beams cross with a small angle.

Critical issues for the intra-train feedback performance include the latency of the system, as this affects the number of corrections that can be made within the duration of the bunchtrain, and the feedback algorithm. Previously we have reported on all-analogue feedback system prototypes in which our aim was to reduce the latency to a few tens of nanoseconds, thereby demonstrating applicability for Linear Collider designs with very short bunchtrains, such as NLC [2], GLC [3] (270ns-long train) and CLIC [4] (< 100ns-long train). We achieved total latencies (signal propagation delay + electronics latency) of 67ns (FONT1) [5], 54ns (FONT2) [6] and 23ns (FONT3) [7].

Here we report on the initial design and first beam tests of an ILC prototype system that incorporates a digital feedback processor based on a state-of-the-art Field Programmable Gate Array (FPGA) chip. The use of a digital processor allows the implementation of more sophisticated algorithms which can be optimised for possible beam jitter scenarios at ILC, but with the penalty of a longer signal processing latency due to the time taken for digitisation and digital logic operations. This approach is now possible for ILC given the long, multi-bunch train in the current design, which includes machine parameter sets with c. 3000/6000 bunches separated by c. 300/150ns respectively.

FONT 4

A schematic of the FONT4 feedback system prototype and the experimental configuration in the ATF extraction beamline is shown in Figure 2. The layout is functionally equivalent to the ILC intra-train feedback system. An

upstream dipole corrector magnet can be used to steer the beam so as to introduce a controllable vertical position offset in stripline BPM ML11X. The BPM signal is initially processed in a front-end analogue signal processor. The analogue output is then sampled, digitised and processed in the digital feedback board to provide an analogue output correction signal. This signal is input to a fast amplifier that drives an adjustable-gap stripline kicker [8], which is used to steer the beam back into nominal vertical position. BPMs ML12X and ML13X serve as independent witnesses of the beam position.

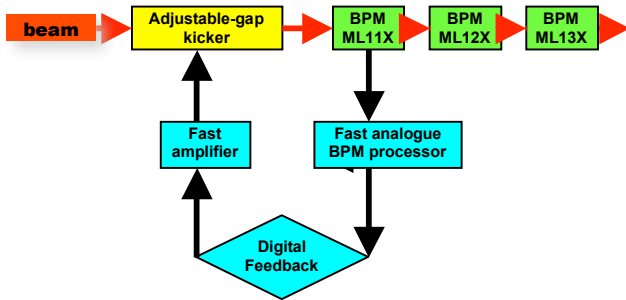


Figure 2: Schematic of FONT4 at the ATF extraction beamline showing the relative locations of the kicker, BPMs and elements of the feedback system.

Since the bunchtrain at ATF comprises 3 bunches separated by c. 150ns, the design latency goal for FONT4 is 140ns. This will allow measurement of the first bunch position and correction of both the second and third bunches. The third-bunch correction allows test of the ‘delay loop’ component of the feedback, which is critical for maintaining the appropriate correction over a long bunchtrain. The constituents of the design latency are shown in Table 1.

Source of delay	Contribution to latency (ns)
Beam time-of-flight	7
Signal return time	15
BPM processor	7
ADC/DAC	40
FPGA processing	25
I/O	3
Amplifier risetime	40
Kicker fill time	3
Total	140

Table 1: Design parameters for the FONT4 system.

ANALOGUE BPM SIGNAL PROCESSOR

The design of the front-end BPM signal processor is based on that for FONT3 [9] and is illustrated in Figure 3. The top and bottom stripline signals were subtracted using a hybrid. The resulting difference signal was band-pass filtered and down-mixed with a 714 MHz local oscillator signal which was phase-locked to the beam. The resulting baseband signal is low-pass filtered. The hybrid, filters and mixer were selected to have latencies of order 1ns, in an attempt to yield a total processor latency of 5-

10ns. The performance of the FONT3 signal processor was reported previously [7,9]. For FONT4 the final low-pass filter was modified to yield a slightly broader output pulse of width c. 7ns (c.f. c. 4.5ns) with a slightly longer latency of c. 7ns (c.f. c. 4ns) (Figure 4).

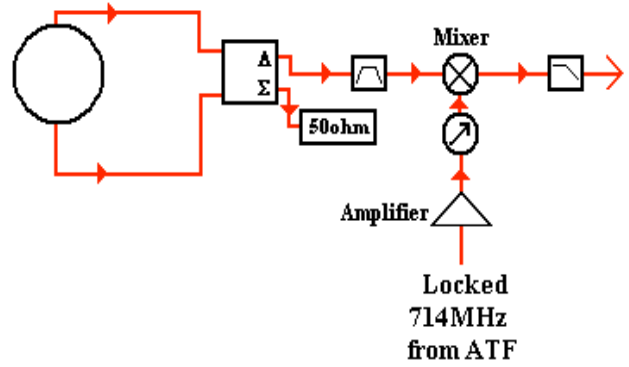


Figure 3: Schematic of BPM signal processor.

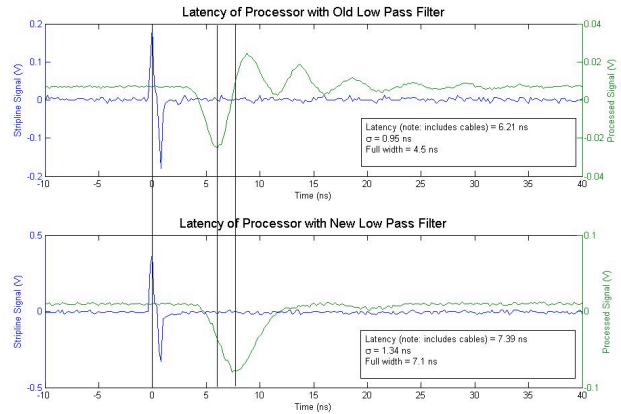


Figure 4: Analogue BPM signal processor outputs (green) for FONT3 (top) and FONT4 (bottom). The bipolar pulses (blue) are the raw stripline response to a single-bunch beam.

DIGITAL FEEDBACK BOARD TESTS

The design of the digital feedback processor board is shown in Figure 5. There are two analogue signal input (output) channels in which digitisation is performed using Analog Devices ADCs (DACs) which can be clocked at up to 100MHz. The digital signal processing is based on a Xilinx Virtex4 FPGA which can be clocked at up to 400MHz. The FPGA is shown on its development board in Figure 6, and the first prototype FONT4 feedback board is shown in Figure 7.

First beam tests were performed in April and June 2006. Figure 7 shows the analogue BPM signal processor output and the corresponding digital feedback board output. The 3 bunches are sampled cleanly. Figure 8 shows a beam position scan: the system response is linear over c. 500um. The initial tests have exercised the basic functionality of the analogue processor and digital

feedback board. Closed-loop tests are planned for winter 2006 and spring 2007.

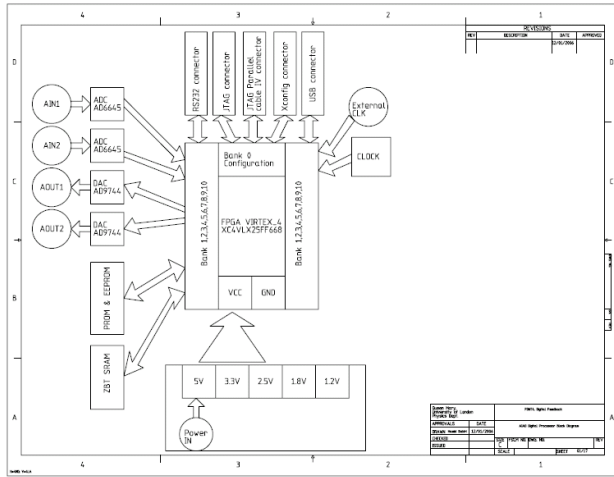


Figure 5: Schematic of digital feedback processor board.

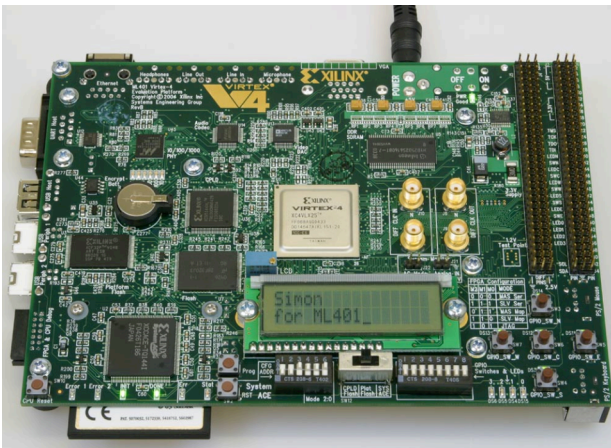


Figure 6: Xilinx Virtex4 development board.

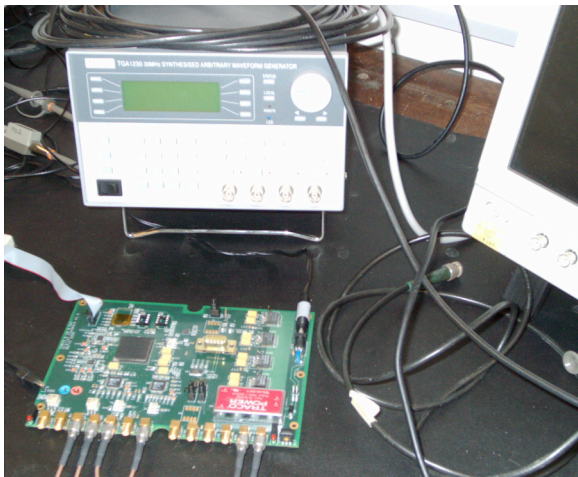


Figure 7: FONT4 digital feedback processor board in bench test.

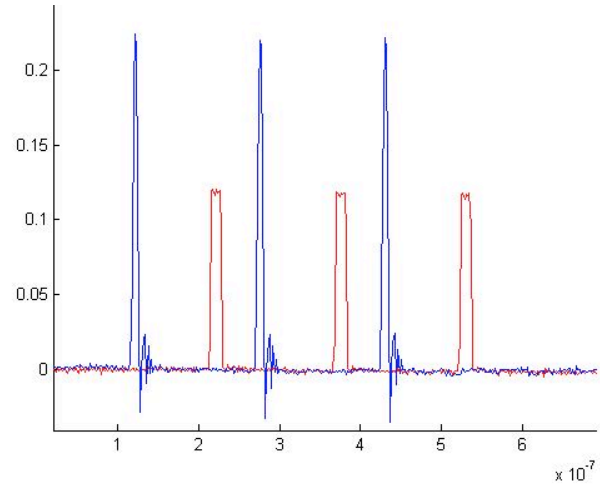


Figure 8: Analogue BPM processor signal (blue) and digital feedback board output (magenta) (V) vs. time (s).

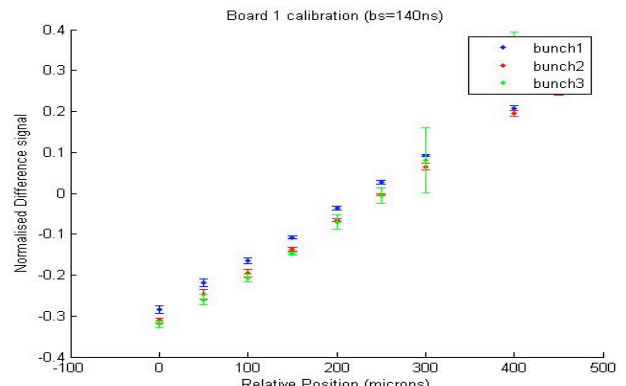


Figure 9: Output of digital board vs. beam position.

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