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Raw data format for the MUON spectrometer

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Abstract

This note[1] defines the format of the MUON spectrometer raw event transmitted to the ALICE DAQ [1]. The payload is in charge of every subsystem. Concerning the spectrometer, two different payloads have to be defined, one for the tracking chambers and one for the trigger chambers.

1 Introduction

The MUON spectrometer consists of absorbers, a dipole magnet, a muon filter (iron wall), a trigger system and a tracking system. The tracking system consists of 156 cathode pad detectors: 16 shaped quadrants and 140 slats. The trigger system consists of 72 resistive plate chambers (RPC). The active modules of the spectrometer (quadrants, slats and RPCs), so-called detection elements, are 228. The dipole magnet deflects the charged particles along the YZ-plane in the ALICE coordinate system [2].

The detection elements of the MUON spectrometer tracking system are distributed over 10 chambers with 1,076,224 readout channels controlled by 16,816 MANU cards (64-channel amplifier-shaper and 12 bits ADC). The data stream is transfered to the front-end controller (CROCUS) via buspatches. Each CROCUS corresponds to one DDL and collects the data stream of one half tracking chamber. There are five front end cards connecting 10 bus patches each. A concentrator CROCUS (CRT) controls the 5 front-end CROCUS (FRT) cards in one crate. There are 20 of those crates. There are two blocks of 25 buspatches in one DDL event. One half-chamber is connected to one DDL concentrating five front end cards corresponding to at most 50 buspatches [3]. The total number of buspatches is 888.

The 4 trigger chambers consist of 20,992 readout channels, connected to 2624 front end cards (8-channel ADULT chip). The 234 local and 16 regional trigger cards control the data stream sent to the readout cards called DARC (1 for 8 regional cards). In the same crate, a global trigger card collects the information of the regional cards and generates the trigger output [4]. The number of DDLs is 2 for the trigger chambers. Each DDL contains the data stream of 4 half-chambers (inside or outside the LHC ring).

For the purpose to run a full reconstruction from raw data to ESD tracks within the package of AliRoot, a method has to be implemented to generate raw data from simulated digits. A framework has been developed by the CERN offline core team [5]. The definition of the so-called payload (raw data sub-event for each system) has to be as close as possible to the real data structure provided by the ALICE experiment. An ALICE raw event includes an event header of 17 words (32 bits) and the DDL structure. The DDL sub-event begins with an equipment header of 7 words followed by a common data header of 8 words [1,7]. The aim of this paper is to define the DDL sub-event container. In the software package AliRoot [6], the number of DDL ranges from 0xA00 to 0xA13 for the tracking chambers (prefix MUONTRK) and from 0xB00 to 0xB01 for the trigger chambers (prefix MUONTRG). The data stream is written in little endian format.

In the following, all words will be considered as 32 bits words.

2 Tracking chamber DDL event

As mentioned above, a CROCUS crate houses five FRT cards, each one containing two DSPs labeled odd and even,respectively. The DDL event has a treelike structure (Russian dolls wise). The DDL event contains, as mentioned before, a standard ALICE header, followed by two data blocks (A and B). A block contains the data from five (at most) FRT CROCUS, Each FRT structure consists of five (at most) bus patches data. Some redundant information exits in the structures for debugging purposes. An overall view of a DDL event is depicted in fig. 1.

2.1 Concentrator CROCUS Block Structure

The block header contains 8 words followed by the data :

- Data key (0xFC0000FC).
- Total length of block.
- Raw data length : length of the block minus the header (8 words).
- DSP identification.
- L1 trigger word.
- Bunch Crossing Id (for mini-event Id, see ref. [1]).
- Event Id in bunch crossing.
- Event Id in orbit number Id.

2.2 Front End CROCUS Structure

The front end CROCUS header contains 8 words followed by the data:

- Data key (0xF000000F).
- Total length of DSP structure,
- Raw data length : length of the DSP structure minus the header (i.e. 10 words).
- Front end DSP identification.
- L1 accept in Block Structure (CRT).
- Mini Event Id in bunch crossing.
- Number of L1 accept in DSP Structure (FRT).
- Number of L1 reject in DSP Structure (FRT).

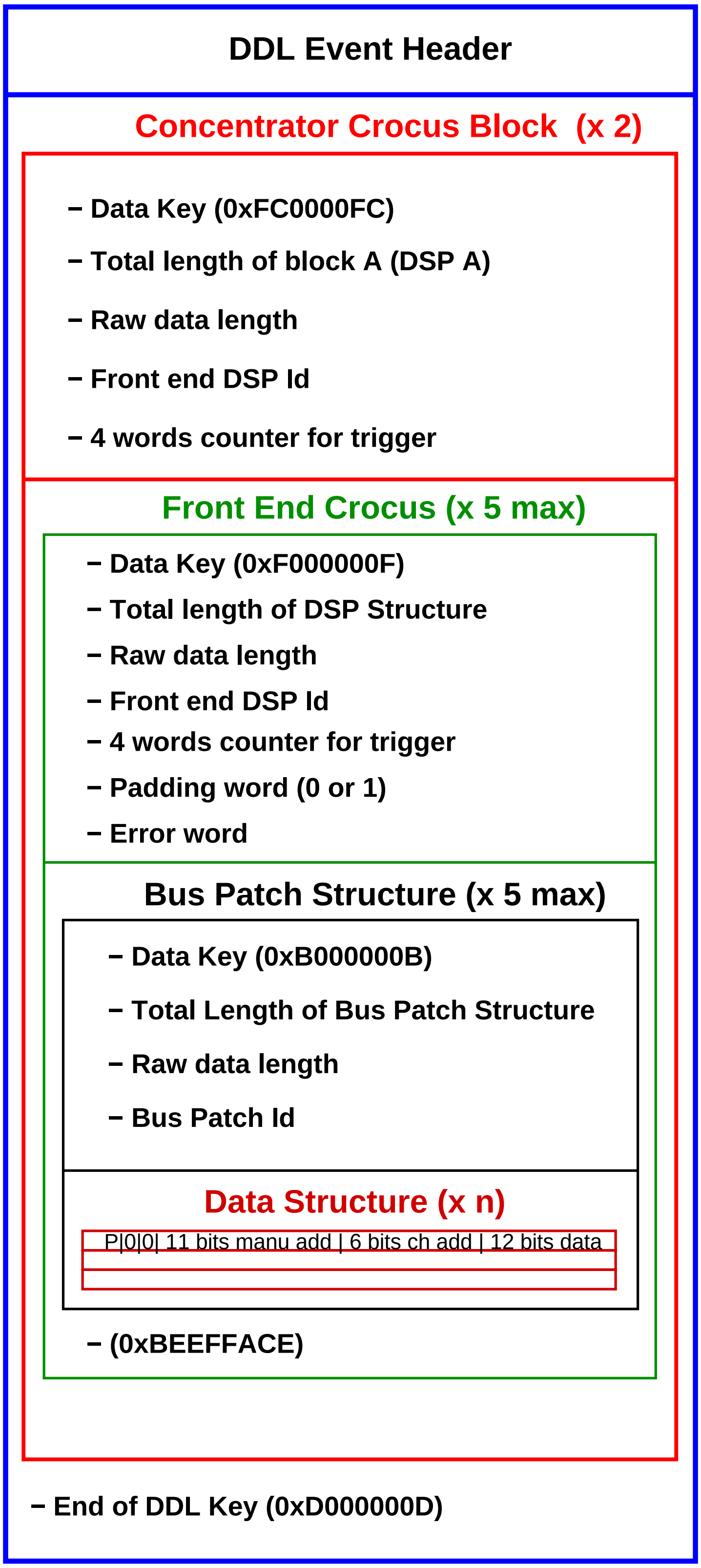

Figure 1. Schematic view of the DDL raw event for tracking chambers.

- Padding flag: this number is set to one if the number of rawdata word is odd and set to zero otherwise.
- Error word.

If the padding flag is set to one, an additional word (0xBEEFFACE) is put at the end of the structure to keep the number of words even.

2.3 Buspatch Structure

The buspatch header contains 4 words followed by the data:

- Data key (0xB000000B).
- Total length of buspatch structure.
- Raw data length: length of the buspatch structure minus the header (4 words).
- Buspatch identification: this allows to identify the buspatch as well as the corresponding detection element.

2.4 Data Structure

The data are packed in 32 bit words; the structure of each word is the following:

- [31]: parity bit : The ADC (MARC) chip set to one the most significant bit (bit 31) of each 32 bit data word if the number of bit equal to 1 in the 31 least significant bits is odd.
- $[29-30]$: must be zero (MBZ).
- $[18-28]$: MANU identification number (11 bits). This number is unique for each detection element.
- $[12-17]$: channel identification number in the MANU card (6 bits).
- $[0-11]$: pad charge digitalized with the ADC (12 bits).

The DDL payload ends with two 32 bit words (0xD000000D) to seperate each Concentrator CROCUS structure.

3 Trigger chamber DDL event

The data flow of the about 21,000 strips will be concentrated in two DARC readout cards. An overall view of a DDL event is depicted in fig. 2. The DDL event header contains 8 additional words, followed by 8 regional controller structures, including the 16 local controller structures. The payload structure

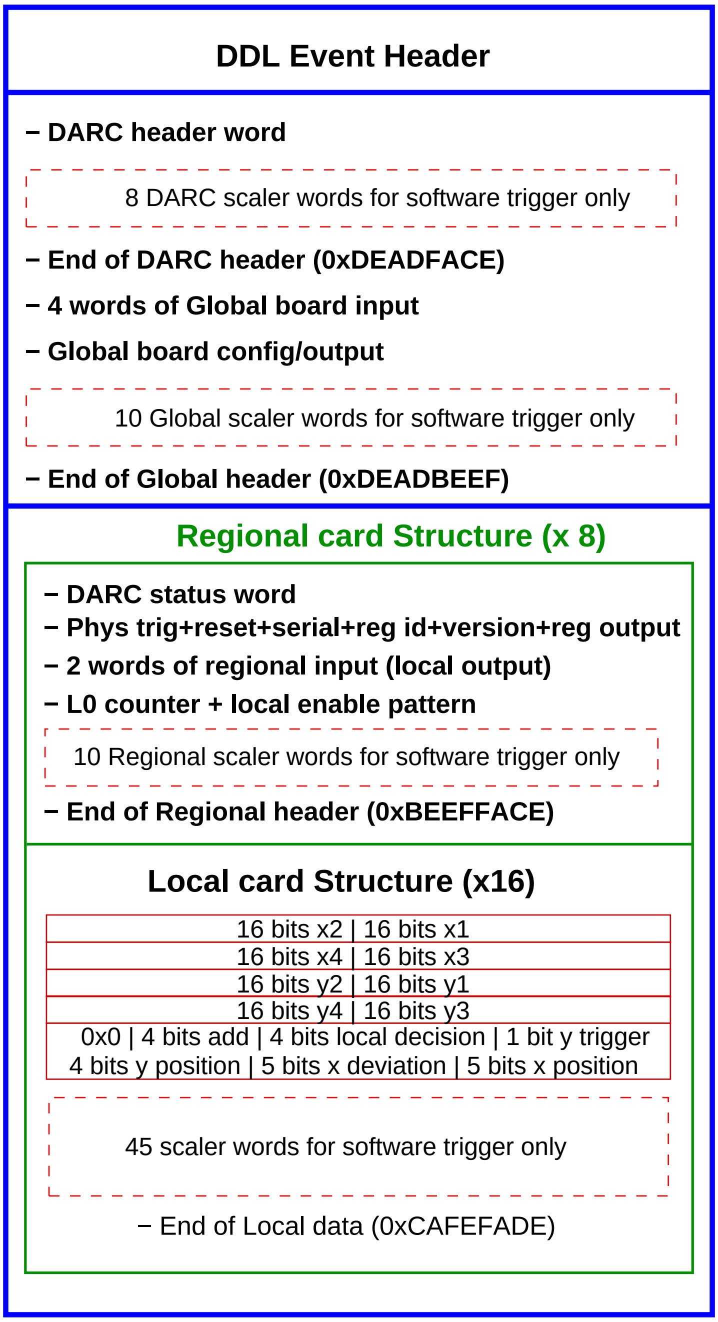

Figure 2. Schematic view of the DDL raw event for trigger chambers.

can be found also in ref. [8]. There are two types of data structure depending on the type of trigger. For a physics trigger, only data from the detectors are read out, while for software triggers additional information (from scalers) is read out as well.

3.1 Header

- Header word:
  - · trigger occurrence (2 bits):
    - 01 = trigger physics
    - 10 = trigger software "Start Of Run"
    - 11 = trigger software "End Of Run"
    - 00 = other trigger software
  - · application type: dimuon, ZDC,... (3 bits),
  - · DARC type: Vadorh, Def,... (3 bits),
  - · serial number (4 bits),
  - · version (8 bits),
  - · VME trigger used (internal) (1 bit),
  - · global card data occurrence (1 bit),
  - · central trigger (or LTU) interfaced (1 bit),
  - · DAQ interfaced (1 bit),
  - · regional cards occurrence (8 bits).
- 8 scaler words (if soft event type)
- separator 0xDEADFACE
- 4 words of global input : 8-bit words coming from each of the 16 regional controllers.
- global card information:
  - · configuration (16 bits),
  - · output (6 bits): unlike sign pair (high and low p_t), like sign pair (high and low p_t) and single muon (high and low p_t).
- 10 scaler words (if soft event type).
- separator 0xDEADBEEF.

The global card information are only present in one DDL (global card data occurrence bit set to one), in the other the words are set to zero. If there is a "software" trigger, scaler information from DARC and Global cards are added (see section "Scalers events" for details).

3.2 Regional card structure

The header of this structure consists of four words:

- DARC status word:
  - · MBZ (2 bits)
  - · error status (8 bits),
    - 1 = physic, 0 = software error
    - regionial occurence
    - full error

empty error
Darc L2 reject error
Darc L2 error
Darc L1 error
Darc L0 error

· FPGA number in card (3 bits),
· MBZ (3 bits),
· physics trigger occurrence (1 bit),
· regional card occurrence (1 bit),
· flag for not fully filled RAM (1 bit),
· flag for not empty RAM (1 bit),
· flag for L2 rejected (1 bit),
· flag for L2 accepted (1 bit),
· flag for L1 (1 bit),
· flag for L0 (1 bit),
· number of events in RAM (4 bits),
· busy word (4 bits).

Whenever the regional board is masked or could not be readout the value of the DARC status word will be set to 0xCAFEDEAD.

- Regional word:

· physics trigger occurrence (1 bit),
· number of reset (6 bits),
· regional controller serial number (5 bits),
· regional crate identification (4 bits),
· FPGA software version (8 bits),
· regional output (8 bits):

two bits for single high p_t muon (00: none, 01: at least one with positive charge, 10: at least one with negative charge, 11 at least one positive and one negative charge);

one bit for unlike sign pair of high p_t muon (bit on if $+-$ or $0+$ or $0-$ or 00);

one bit for like sign pair of high p_t muon (bit on if $++$ or $--$ or $0+$ or $0-$ or 00);

two bits for single low p_t muon (00: none, 01: at least one with positive charge, 10: at least one with negative charge, 11 at least one positive and one negative charge);

one bit for unlike sign pair of low p_t muon (bit on if $+-$ or $0+$ or $0-$ or 00);

one bit for like sign pair of low p_t muon (bit on if $++$ or $--$ or $0+$ or $0-$ or 00).

- 2 words of regional input corresponding to the 16 local controllers data:

· low p_t word (00: none, 01: at least one with positive charge, 10: at least

one negative charge, 11 at least one positive and one negative charge), 2 bits for each local board.
  - · hight p_t word (00: none, 01: at least one with positive charge, 10: at least one negative charge, 11 at least one positive and one negative charge), 2 bits for each local board.
- L0 counter (16 bits) and enable pattern for local board (16 bits).
- 10 scaler words (if soft event type).
- separator 0xBEEFFACE

Followed by the local card structure.

If there is a "software" trigger, scaler information from regional cards are added (see section "Scaler events" for details).

3.3 Local card structure

The local structure format contains 5 words defined as follows:

- 16 bits corresponding to position along X axis in plane 2, first station (x2) and 16 bits corresponding to X in the first plane (x1).
- 16 bits corresponding to position along X axis in plane 4, second station (x4) and 16 bits corresponding to X in the third plane (x3).
- 16 bits corresponding to y2 and 16 bits to y1.
- 16 bits corresponding to y4 and 16 bits to y3.
- 32 bits word (more details can be found in chapter 3.3 in ref. [4]):
  - · 9 bits are set to zero.
  - · 4 bits are used to encode the local card identification number in the crate (0-15).
  - · 4 bits are used to encode the trigger information from the local card decision: 2 bits for high p_t and 2 bits for low p_t trigger (least bits). No trigger: 00, trigger for negative particles: 01, trigger for positive particles: 10, trigger with no deviation: 11.
  - · 1 bit is used for y trigger: trigger occurrence of the local card along the X strips.
  - · 4 bits are used for y position (if there is a trigger, the parameter y trigger is set to 0, if not, the parameter is set to 1 and the y position is equal to 15).
  - · 5 bits are used to encode the x trigger and x deviation information 1 bit is used for the sign of the deviation and 4 bits are used for the deviation: (negative particule: sign = 0 and xdev = 1-15; positive particule: sign = 1 and xdev = 1-15; undefined deviation: sign = 0 and xdev = 0; no x trigger: sign = 1 and xdev = 0)
  - · 5 bits are used for x position.

· 45 scaler words (if soft event type).
· separator 0xCAFEFADE.

For empty or non-notified local card slots, the 5 words are set to the value: 0x10CDEAD.

If there is a "software" trigger, the data structure is replaced by 45 words of scaler information (see next section for details).

3.4 Scalers events

Whenever a "software" trigger (also called "checking" trigger) occurs a set of additional or replacing data will be sent to the DAQ system. There are extra words for the DARC card scalers, global card scalers, regional card scalers and local card scalers. The latter are replacing the "physics" trigger words.

3.4.1 DARC scaler words

The 8 scaler words are the following:

- number of L0 triggers received (16 bits), number of trigger L0 used (16 bits),
- number of L1 "physics" triggers, received (16 bits) and used (16 bits),
- number of L1 "software" triggers received (16 bits) and used (16 bits),
- number of L2 accept triggers, received (16 bits) and used (16 bits),
- number of L2 reject triggers, received (16 bits) and used (16 bits),
- number of clock cycles,
- number of clock cycles during Hold (dead time),
- spare (16 bits), number of prepulses, received (16 bits).

3.4.2 Global card scaler words

The 10 scaler words are the following:

- number of L0 triggers,
- number of clock cycles,
- 6 words for global card output scalers (low and high transverse momentum for unlike, like sign muon pairs and single muons),
- number of Hold (dead time),
- spare word.

3.4.3 Regional card scaler words

The 10 scaler words are the following:

- number of clock cycles,
- 8 words for regional card scalers output,
- number of clock cycles during Hold (dead time).

3.4.4 Local card scaler words

The 45 scaler words are the following:

- number of trigger L0,
- number of Hold (dead time),
- number of clock cycles,
- 8 words for local trigger card scalers (low and high transverse momentum for no trigger, positive charge, negative charge and undefined charge scalers),
- 4×16 words of single counting strips X1 to X4 (or Y1 to Y4) coded on 16 bits each stored two by two in a 32 bits word,
- switches configuration (10 bits) and the ComptXY (1 bit) (set to 0 for X strip configuration and to 1 for Y strip configuration).
- spare.

For empty or non-notified local card slots, the 45 words are set to the value: 0x10CDEAD.

More details on scaler words and switches can be found in ref [4].

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