

# Final Results from the APV25 Production Wafer Testing

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## Abstract

The APV25 is the front end readout chip for the CMS silicon microstrip tracker. Approximately 75,000 chips are required and the production phase is now complete. Each chip on every wafer is subjected to detailed probe testing to verify full functionality and performance, and only chips that pass all tests are selected for mounting on detector modules.

Over several years more than 500 wafers have been tested and results for all chips have been archived. An analysis of the database allows significant comparisons between chips, wafers and wafer production batches, giving a complete and final picture of the spread in yield and performance experienced in this large scale manufacturing task.

## I. INTRODUCTION

The APV25 is a 128 channel chip designed for the CMS silicon microstrip tracker readout. It has been manufactured in 0.25  $\mu\text{m}$  CMOS technology on 200 mm diameter wafers. Figure 1 shows a photograph of a wafer and a floor-plan of an individual chip. A summary of the chip features and performance is given in table 1. More details of the chip can be found in [1,2].

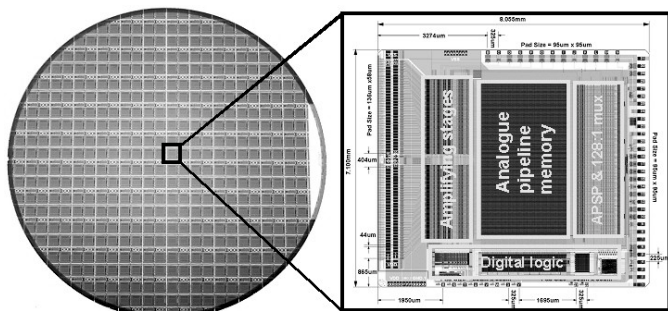


Figure 1: 200 mm APV25 wafer and individual chip floor-plan

Approximately 75,000 APV chips (plus spares) are required to instrument  $\sim 10^7$  microstrip channels. The wafers were delivered in production lots of up to 25 wafers, each wafer containing 360 viable APV sites. We have previously reported [3,4,5] on progress and problems encountered during the several years over which this production task has been spread. Because of wafer yield and hybrid production losses we have probe-tested more than 600 wafers (216,000 chips) to obtain sufficient numbers of APVs to complete the tracker construction.

During testing all chips were identified by wafer name and location on the wafer, maps being produced for subsequent dicing and picking by the hybrid manufacturer. The test results were stored in a database, allowing us to perform detailed analyses comparing performance between chips, wafers and production lots. The results of these analyses provide insight into the stability of performance achievable from such a large-scale manufacturing task.

Table 1: APV25 features and performance

FEATURE	VALUE/DESCRIPTION/COMMENT
front end	128 channels, low noise CR-RC amplifier, 50ns shaping time
analogue pipeline	40 MS/s, 192 cells deep. Allows up to 4 $\mu\text{s}$ level 1 trigger latency, plus buffering for events awaiting readout
pipeline readout	<i>peak or deconvolution</i> operating modes <i>peak mode</i> : 1 sample/channel <i>deconvolution</i> : weighted sum of 3 samples gives single bunch crossing time resolution
output stage	128:1 analogue multiplexer, single differential current output
noise	peak mode: $270 + 38/\text{pF}$ deconvolution: $430 + 61/\text{pF}$
I <sup>2</sup> C slow control I/F	programmable bias registers, operating mode, trigger latency ....
LVDS fast control I/F	40 MHz clock and level 1 trigger
test pulse	on-chip test pulse generator with programmable amplitude and delay
rad-hard	> 100 kGray (10 Mrads)

## II. WAFER TESTING

The on-wafer chip tests were designed to verify both digital and analogue functionality and have been previously described [3,4,5]. Digital tests included verification of the fast and slow control interfaces, on-chip programmable registers, and pipeline control and readout logic. Any digital error resulted in the chip being failed. Analogue tests included pedestals, pulse-shape, gain and noise measurements, pipeline uniformity, individual pipeline element storage capability, and power consumption. Performance was measured in all operational modes for all channels, at full speed (40 MHz). Analogue acceptance thresholds were defined to ensure satisfactory performance for the application. A test time/chip close to one minute allowed a throughput of 2 wafers/day. All the wafers were tested on a single semi-automatic probe-station, over a period of  $\sim 4$  years, the final lot 29 being delivered in Spring 2005.

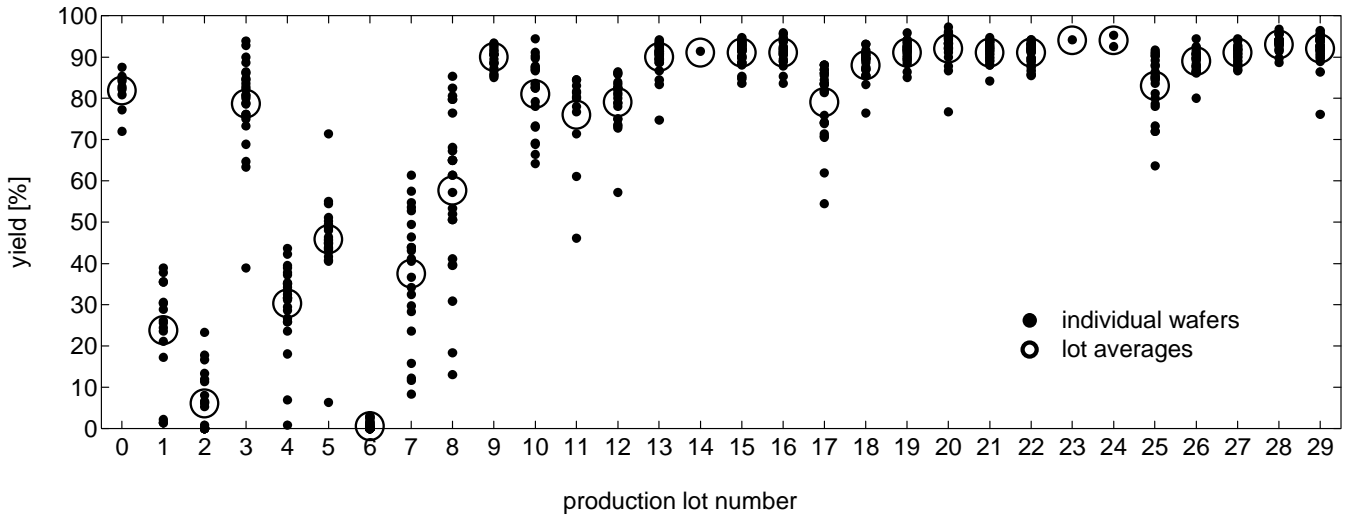


Figure 2: Wafer yield (percentage of pass chips/wafer) dependence on production lot number.

The yields/wafer of chips which passed all tests are shown in figure 2, where results for 605 individual wafers together with lot averages are displayed. The yield problems for some of the earlier lots, prior to lot 9, can be clearly observed, as can the excellent 88 % average yield achieved from lot 9 onwards. The definition of a production lot is based on individual deliveries. In the foundry wafers are processed in lots of 25, and most deliveries contained wafer numbers consistent with that. A few lots (14, 23 and 24) consisted of only one or two wafers which were delivered to satisfy the number of wafers ordered, but which were almost certainly processed at the same time as wafers from previous deliveries.

### III. WAFER PROBE TEST DATA ANALYSIS

In this section we present results from studies of the APV wafer probe testing database. Because of reliability concerns low yield lots have not been used for detector module construction, so the results here are based mainly on data from lot 9 onwards. Where possible we have compared measured performance with SPICE simulations. Process dependent model parameters can vary from their nominal values with a distribution characterised by its standard deviation sigma ( $\sigma$ ). When simulating, sigma can be varied from its nominal value to model the effects of processing variations on circuit operation.

The analysis results are based on data from chips which were passed at wafer probe time. Chips which passed all wafer probe tests are referred to as known good die (KGD).

It is important to note that values for the programmable bias parameters, which define the individual currents and voltages required by the analogue circuits on the chip, were kept unchanged throughout the whole wafer probing task, hence chip-to-chip variations truly reflect differences due to processing.

#### A. Reference and Power Supply Currents

During wafer testing the chip was powered by positive ( $V_{dd}$ , +1.25V) and negative ( $V_{ss}$ , -1.25 V) voltages with respect to ground. (Note that in the CMS system  $V_{ss}$  is defined as ground, and +1.25 and +2.5 V rails are used.) The bias generator circuit takes its reference from a single current source which can be provided either internally or externally.

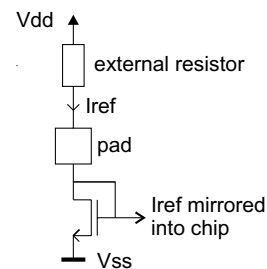


Figure 3: External master reference current generator circuit.

##### 1) Master reference $I_{ref}$ :

When the APV is programmed to select an external current reference the simple circuit shown in figure 3 provides the master reference current  $I_{ref}$ , where the resistor is external to the chip.  $I_{ref}$  can therefore be measured during the probing, its value depending on process variations affecting the threshold and transconductance of the gate-drain connected transistor. Figure 4 shows histograms of external  $I_{ref}$  values from all KGD from all 30 lots. The SPICE simulated values for  $I_{ref}$  are also indicated for process parameters differing in units of sigma from the nominal values. Figure 4 shows that the process has remained centred close to nominal throughout the APV production, with almost all chips giving results within  $\pm 1$  sigma.

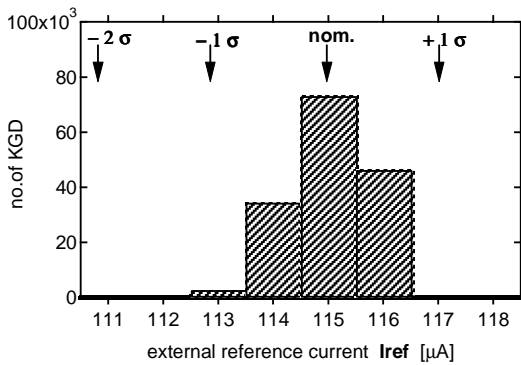


Figure 4: Iref values for all KGD from all lots (0 – 29)

## 2) Power supply currents:

To minimise hybrid components in CMS the internal reference current is used, where Iref is provided internally by a threshold voltage referenced current source. The overall supply currents will depend on how the power consumptions of the individual circuit blocks, analogue and digital, change with processing variations, and will also depend on the value of Iref and the parameters programmed into the on-chip bias generator registers. Figure 5 shows Vdd and Vss supply currents for all production lots (lot 9 onwards). The distributions are narrow, indicating close matching between chips, wafers and lots.

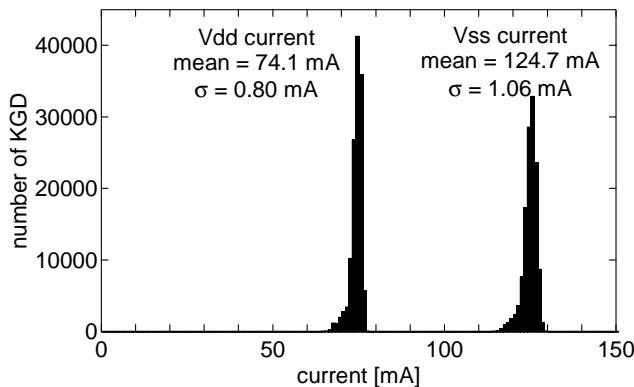


Figure 5: Overall power supply currents for internally generated master reference current Iref, for all KGD from lots 9 - 29.

## B. Pulse Shapes and Gain

During wafer testing the peak and deconvolution mode pulse shapes for all channels are measured using the on-chip test pulse circuit. The two programmable parameters which most strongly affect the pulse shape are the current flowing in the input stage of the shaping amplifier (ISHA) and the voltage controlling the shaper feedback resistor (VFS). These are derived from the master reference current Iref and were programmed with the same value throughout the wafer testing of all lots.

The amplitude of the on-chip test pulse depends on the values of small test capacitors feeding the preamplifier

inputs, which are implemented by two crossed metal routing layers, and are thus sensitive to process variations associated with the definition of the metal lines, and the inter-layer separation.

### 1) Pulse shapes:

Figure 6 shows an intensity plot of normalised average peak mode pulse shapes for all 131,734 KGD from production lots 9 to 29 inclusive (414 wafers), and figure 7 shows the same picture for deconvolution mode. The intensity plots are scaled such that an area is saturated black if it contains more than 5 data points (each data point being a point on a pulse shape curve). Forcing the intensity to saturate in this way allows the close matching to be clearly demonstrated since it allows pulse shapes from individual chips to show up. SPICE simulated pulse shape waveforms are superimposed on figure 6 for different values of sigma, and it can be seen that almost all chips produce pulse shapes within the  $\pm 1$  sigma range.

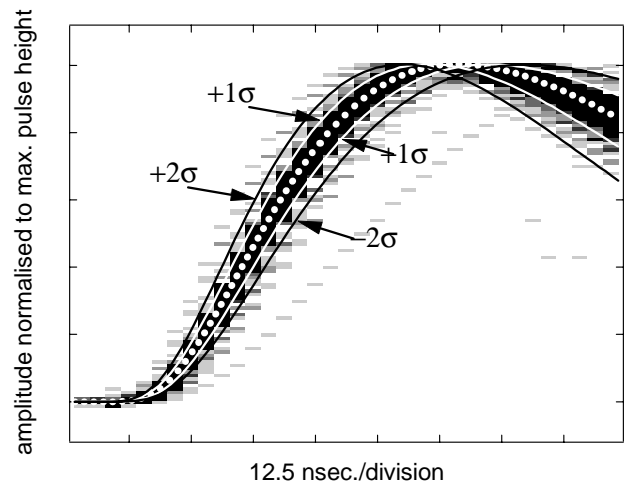


Figure 6: Intensity plot showing normalised peak mode pulse shapes for all KGD from lots 9 - 29, and SPICE simulations for different values of process variation parameter sigma ( $\sigma$ ).

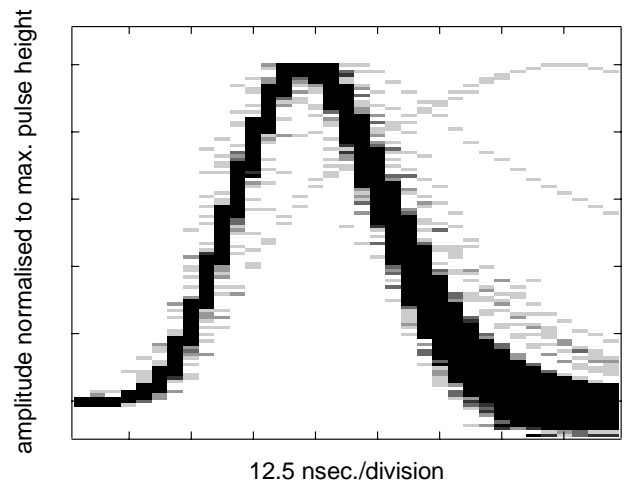


Figure 7: Intensity plot showing normalised deconvolution mode pulse shapes for all KGD from lots 9 – 29.

## 2) Gain:

It is not possible to measure the true gain of the chip because of significant processing variations in the values of the small on-chip test capacitors. Figure 8 shows typical distributions of average chip pulse height, in peak and deconvolution mode, in this case for all pass chips from lot 25. Figure 9 shows the means and standard deviations of these distributions for lots 9 – 29. The lot-to-lot variation in mean pulse height will be dominated by uncertainties in the test capacitors, but in any case the matching is well within requirements.

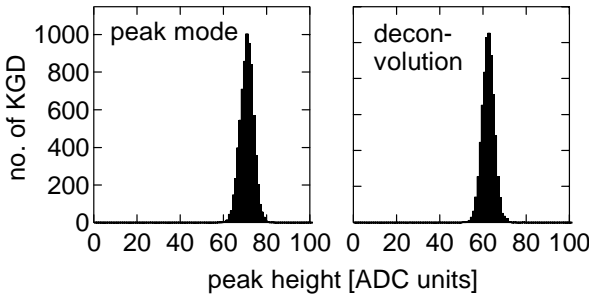


Figure 8: Peak pulse heights for KGD from lot 25.

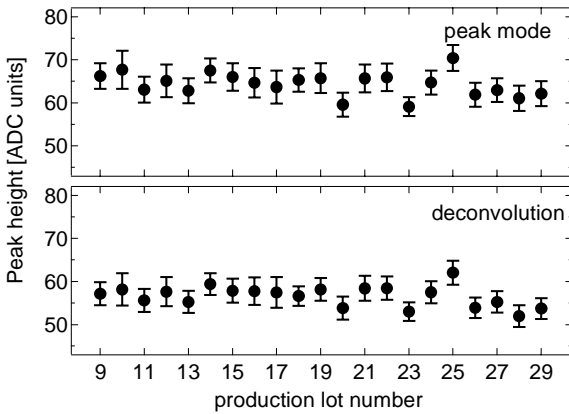


Figure 9: Average peak pulse heights for production lots 9 – 29. The error bars represent  $\pm 1$  standard deviation.

## C. Channel and Pipeline Noise

Measuring noise performance in the probe station environment is difficult because of electrical interference generated by electromechanical components of the machine. For each chip tested the individual APV channel noise is measured, as well as the contribution which arises from non-uniformities in the pipelines.

### 1) Channel noise:

Channel noise is measured in deconvolution mode by computing the rms value of 200 pedestal values acquired

for each of the 128 channels. The chip-to-chip, wafer-to-wafer and lot-to-lot variation is small, so figure 10 contains the accumulated results for all channels for all KGD from production lots 9 to 29. The mean of the distribution is 0.64 ADC units which corresponds approximately [5] to 540 electrons. This is slightly in excess of expectation, but includes a contribution from electrical interference.

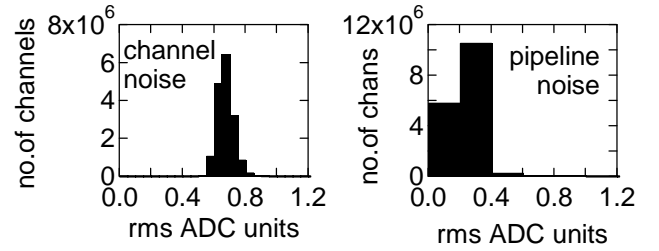


Figure 10: Channel and pipeline noise for all channels for all KGD from lots 9 – 29.

### 2) Pipeline noise:

During the wafer test procedure channel pedestals are acquired for all 192 pipeline locations for all 128 channels. Pedestal variations from location to location along the pipeline constitute an additional noise source in the system, which can be quantified by computing the rms of the 192 pipeline pedestal values for each channel, and figure 10 includes the results. The levels are such that the contribution to the overall system noise in CMS will be negligible.

## D. Output Frame Parameters

Figure 11 shows a picture of an APV output data frame. In the absence of triggers the APV produces synchronization pulses (known as tick marks) which reflect the operating phase of the internal pipeline readout circuitry. The APV output frame consists of a digital header followed by the 128 analogue samples. The digital header replaces a normal tick mark, allowing the external DAQ system to easily recognise that an output frame has started.

The digital header amplitude coincides approximately with the full-scale range of the analogue output levels. The average analogue pedestal level (analogue baseline) can be programmed to be anywhere within the digital header range by means of the voltage offset parameter VPSP.

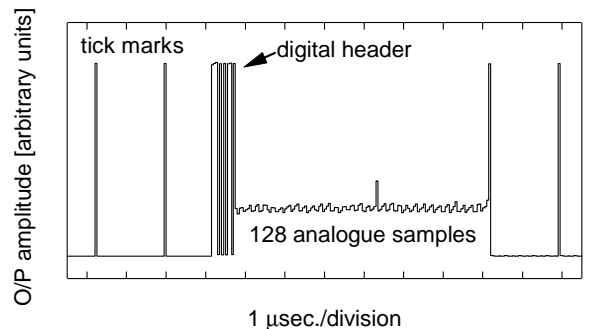


Figure 11: APV25 output data frame.

### 1) Digital header amplitude:

The digital header high and low levels are set by two on-chip current references. The repeatability of the amplitude of the digital header is of some significance in the CMS system because it is used in the setup procedure for the transmission links off the detector. Figure 12 shows the distributions of the average digital high and low levels, and the amplitudes, which are the differences between the high and low levels, for a typical lot. The mean values and standard deviations of these distributions for lots 9 – 29 are shown in figure 13, where only small lot-to-lot variations are observed.

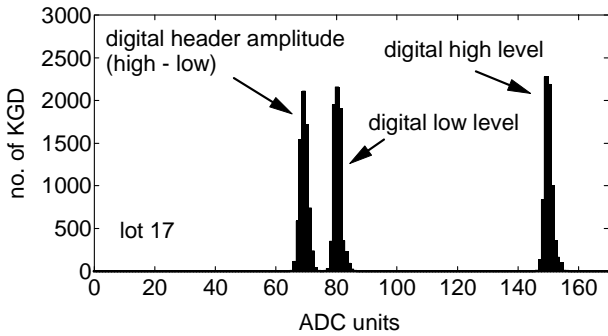


Figure 12: Digital header high and low levels, and the digital header amplitude, for all KGD from lot 17.

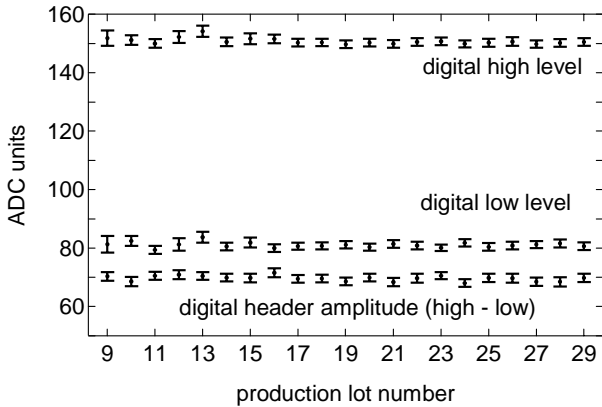


Figure 13: Average digital header high, low and amplitude parameters from all KGD from lots 9 – 29. The error bars represent  $\pm 1$  standard deviation.

### 2) VPSP:

The bias generator parameter VPSP sets the average analogue baseline level in the APV output frame. It works by introducing an offset in the pipeline readout circuitry resulting in small differences in the value required to set the same baseline position in peak and deconvolution modes. The sensitivity to this parameter is such that it is the only parameter which is varied during wafer testing, and it is tuned to position the baseline at approximately 25% of the digital header range as in figure 11. For each lot we have calculated the mean VPSP value required to achieve the 25% level, and its standard deviation, and these are shown in figure 14 for both peak and deconvolution modes. The

lot-to-lot variation can be seen to be small, and the chip to chip variation within lots is even smaller.

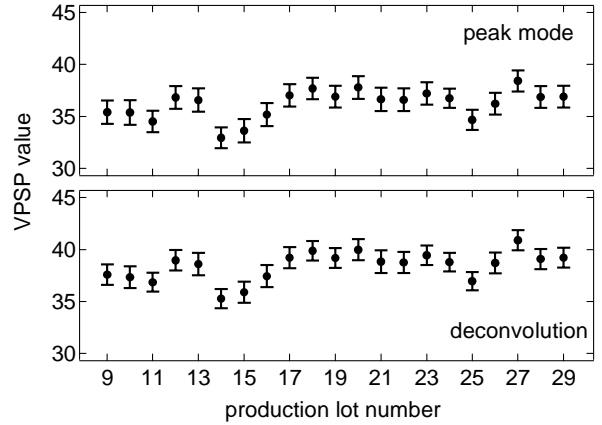


Figure 14: VPSP values

## IV. CONCLUSIONS

More than 600 APV25 wafers have been screened over a period of ~ 4 years to provide sufficient numbers of chips to instrument the CMS silicon microstrip tracker. After early yield problems were solved an average yield of 88 % was achieved.

An analysis of the archived test data shows that close chip-chip and wafer-wafer matching has been maintained throughout the production period

## V. ACKNOWLEDGEMENTS

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## VI. REFERENCES

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