CURO - A current based readout ASIC for a DEPFET pixel based vertex detector at the ILC

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Abstract

For a fast readout of a DEPFET pixel matrix at the ILC with line rates of 20 MHz and more, the 128 channel CURO II ASIC has been designed and fabricated in a 0.25 μm process. Due to the current signal of the DEPFET sensor, the architecture of the chip is completely based on current mode (SI) techniques. The architecture comprises of correlated-double-sampling in the analog front end with current memory cells and a simultaneous current compare. Zero suppression of the data is done on chip as well by a fast hitscanner. Measurements show that the performance of the readout chip complies with the requirements of the ILC.

I. Introduction

The DEPFET (**DEP**leted **F**ield **E**ffect **T**ransistor) pixel detector [1] is one of the technology options presently discussed for a vertex detector at the ILC (International Linear Collider). A detailed overview of the proposal can be found in [2]. The most important requirements concerning the readout chip are an on chip zero suppression and an operation at a line rate of 20 MHz. Furthermore, a noise figure of ENC $< 100\,e^-$ is desirable.

To offer a readout perfectly adapted to the current signal of the DEPFET detector, a current-mode operation was chosen, the CURO (**CU**rrent **R**ead**O**ut) architecture. Furthermore, an operation in the current domain offers a very convenient and accurate subtraction of two currents, which is needed for an on chip pedestal subtraction. Due to the current based operation, the performance of the readout chip is given for current signals. The current values can be converted into a signal charge by the internal amplification g_q of the DEPFET detector. Present sensors with a conservative design achieve an amplification of about 283 pA/e^-. It can be assumed that future sensors with a more aggressive layout will achieve an amplification of up to 1 nA/e^- [3].

Furthermore, the CURO II chip has been successfully operated in a prototype system for the readout of a 64×128 DEPFET pixel matrix [4]. In a recent testbeam, a noise performance of ENC $\approx 220\,e^-$ and a signal-to-noise ratio of S/N > 140 has been achieved [5].

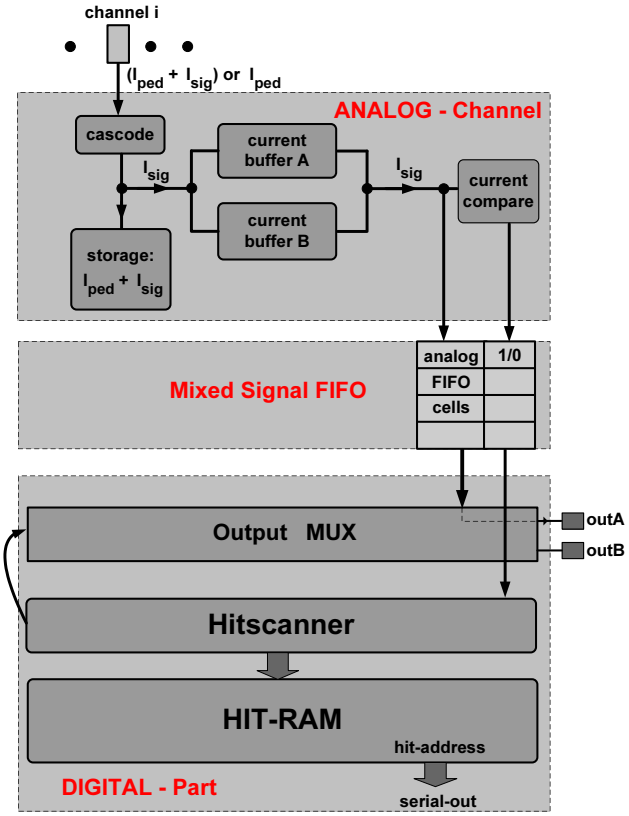

Figure 1: Schematic overview of the CURO-Architecture.

II. Architecture of the readout chip

The readout principle of the CURO architecture is illustrated in figure 1. It consists of three major parts. An analog part, a mixed-signal FIFO and a digital part. To keep the overview clearer, only one channel is shown for the analog part and for the mixed signal FIFO. Switches for the routing of the various currents at the junctions are not shown for simplicity.

To provide a low input impedance for the DEPFET current the first stage of the analog part is realized by a regu-

lated cascode. The readout of one matrix row is performed as follows. After one row in the sensor matrix has been selected for readout, the signal current of the pixel superimposed on a pedestal current $I_{sig} + I_{ped}$ is stored in a current memory cell. Details concerning the design of the current memory cell can be found in [6]. The row is then cleared and the remaining pedestal current provided by the sensor I_{ped} is automatically subtracted at the memory cell. The resulting signal current I_{sig} is stored alternately in two buffer cells. Due to the alternating storage in the buffer cells, the analog front end can hand over a signal current, while the signal current from the previous cycle is used for hit detection.

The hit detection is performed by comparing the signal current with a programmable threshold. Afterwards, the digital hit information is stored together with the analog value in a small mixed signal FIFO. The FIFO derandomizes the hit rate fluctuations to a constant rate. Simulations show that a FIFO depth of 4-8 rows is enough to cope with the occupancy expected at the ILC [7]. The currents in the FIFO below the threshold are not relevant and the digital pattern can be used to switch off the appropriate analog FIFO cells to save power. One can think of a more sophisticated clustering logic, keeping the neighbors of a seed pixel as well, for example. Note, that the whole front end is operated by one single clock, synchronous to the row clock of the matrix. All control signals for the complex analog part are derived from this clock inside the chip.

To empty the FIFO, a fast hitscanner, originally proposed for the readout of micro strip detectors [8], is used. The hitscanner analyzes the digital hit pattern and finds up to 2 hits per cycle. Their addresses including a row stamp are stored in a HIT-RAM and the analog values are multiplexed to 2 output nodes where they are digitized by two external ADCs. The ADCs can in principle, be integrated onto the chip as well. The HIT-RAM should be large enough to store all hits of a bunch train, so that it can be read out conveniently during the long pauses between the trains. After zero suppression the expected data volume of a whole bunch train for a 128 channel chip is below 100 kB for the innermost layer. The integration of an adequate RAM is therefore trivial. For the outer layer the amount of data will be even smaller due to the lower background rate. After the RAM is read out, the hit coordinates can be associated with the values digitized by the ADCs.

III. Results

The $4.5 \times 4.5\,mm^2$ CURO II chip is shown in figure 2. The chip has been fabricated in a TSMC $0.25\,\mu m$, 5 metal process. With a design and fabrication process similar to the pixel and strip readout chips used at the LHC, which have been proven to sustain radiation doses higher than 50 MRad [9], CURO II is expected to cope with the radiation doses at the ILC (≈ 200 kRad). Compared to the general CURO architecture introduced in section II, CURO II implements only one analog FIFO row. Therefore, the analog readout has to be interrupted if more than two hits are found in a row. For a continuous analog readout which can cope with higher occupancies the analog FIFO size can be scaled easily to a suitable size in a future chip version. Furthermore, a continuous binary operation with high occupancies is possible, as the full digital FIFO size is implemented.

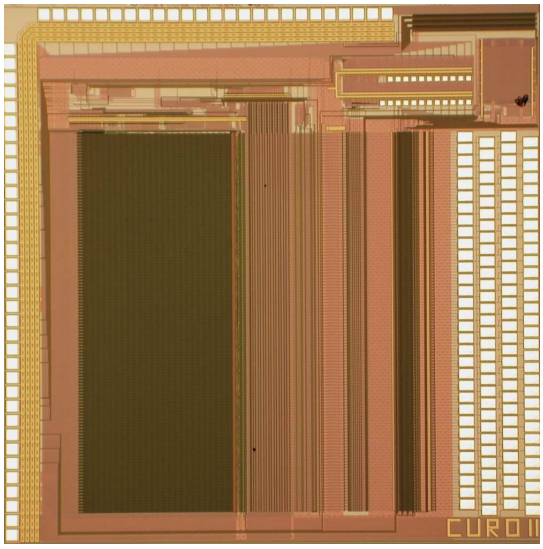

Figure 2: Micro photograph of the $4.5 \times 4.5\,mm^2$ CURO II chip fabricated in a $0.25\,\mu m$ process.

Linearity of the analog part

To offer standalone testability of the analog part, a global test current source is implemented on the chip. The capacitive load at the input node using the test current source has been estimated to approximately 10 pF. All measurements concerning the analog part are performed at 24 MHz since this maximum analog frequency is given by the present test system. This frequency corresponds to 48 MSPS[1] since two samples are done in one clock cycle.

The linearity of the complete analog part, e.g. the input cascode and 3 successive sampling stages (pedestal subtraction, buffer and FIFO cell), is shown in figure 3 for channel 12. A linear fit yields a transfer characteristic of 1.00 ± 0.01. The integral non-linearity for a dynamic range of $12.5\,\mu A$ is INL=2.3 %. Assuming a signal of 4000 e^- for a MIP in a $50\,\mu m$ thin detector and an amplification of $1\,nA/e^-$ of the DEPFET device, this range complies with the signal range of approximately three MIPs.

The transfer characteristic for all 128 channels are shown in figure 4. Both plots are zero suppressed. Due to the properties of the memory cell, the transfer behavior

[1] **M**ega **S**amples **P**er **S**econd

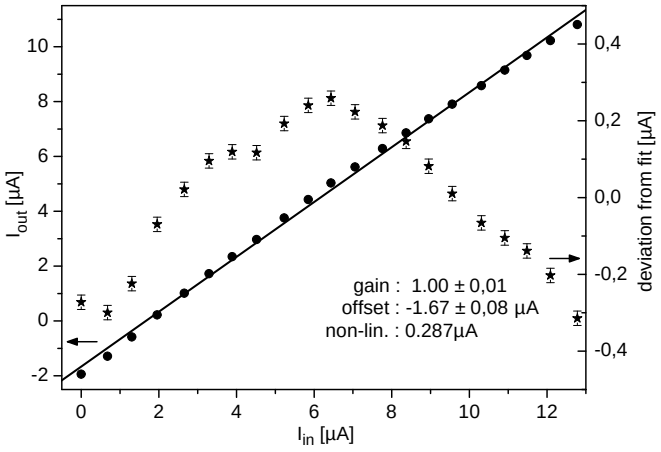

Figure 3: Linearity of one analog channel of CURO II. The output current is plotted as a function of the input current and the deviation from a linear fit is shown.

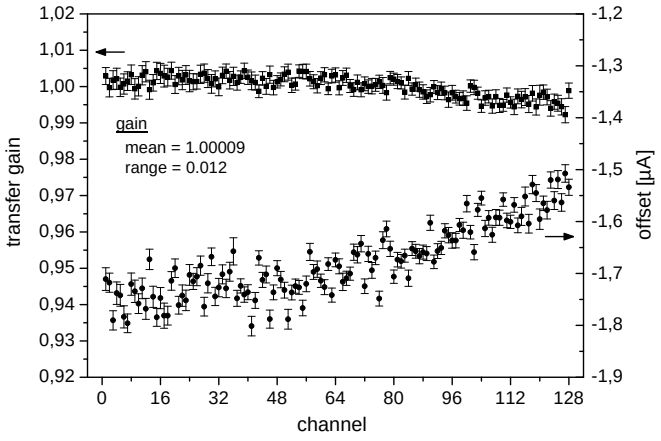

Figure 4: Homogeneity of the transfer gain and offset of the analog part for all 128 channels of CURO II.

is, in first order, insensitive to fluctuations of the supply voltage and a narrow dispersion of the transfer gain with a mean deviation from a perfect transfer of $9 \cdot 10^{-5}$ and a total range of 0.012 is achieved. Such techniques have not been taken into account for the offset where a much broader dispersion is observed. However, any inhomogeneity in the offset is of minor importance since it can be compensated by a threshold calibration using a 5 bit DAC integrated in the comparator unit (not shown in figure 1).

Pedestal subtraction

The performance of the pedestal subtraction has been measured by sweeping the pedestal current of the test source for a constant signal current. An accurate pedestal subtraction is needed since a global threshold will be used for the hit detection in the comparator stage. In the ideal case, the output of the analog part is independent of the pedestal for a given signal. The more the output current

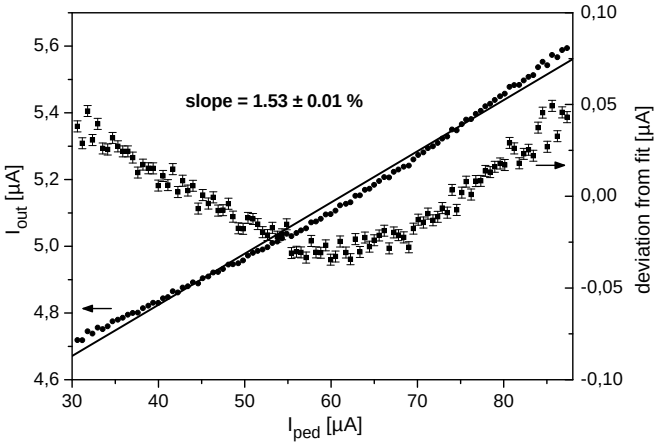

Figure 5: Performance of the pedestal subtraction. The output current is plotted as a function of the pedestal current for $I_{sig} = 6.8\,\mu$A.

depends on the pedestal (i.e. the worse the pedestal subtraction is performed), the higher the comparator threshold needs to be set to compensate the pedestal variation. A channel wise dispersion of the pedestals in a matrix could also be compensated by the calibration unit implemented in the current comparator. Inhomogeneities within a matrix column, on the other hand, cannot be compensated by this calibration. Further on, the number of rows in a ladder of the vertex detector is much larger than the number of columns. Hence, a much higher pedestal dispersion is expected within a column and an accurate pedestal subtraction is needed. Figure 5 shows the observed output current of the chip as a function of the pedestal current for a constant signal current of $6.8\,\mu$A. The plot is zero suppressed. Although a linear dependence is not necessarily expected, a linear fit is used to qualify the pedestal subtraction. A slope of $1.53 \pm 0.01\,\%$ is observed. Assigning this performance to a DEPFET matrix with a statistical spread of $5\,\mu$A in the pedestals, a variation of 75 nA would remain after pedestal subtraction. This variation can be further reduced by an off chip fixed pattern correction. For the on chip hit detection using a global threshold, this performance is more than sufficient.

Noise contribution to the readout

The dominant noise contribution of the CURO II chip is given by the current memory cells in the analog part. It has been measured by observing the response of the comparator stage when sweeping the threshold for a given input current. The measurement has been performed at room temperature. As shown in figure 6, the ideal step response of the comparator is convoluted with the Gaussian noise distribution of the analog front end. An error function is fitted to the comparator response and a noise of $\sigma = 43 \pm 1$ nA is found. Since the current comparator is located behind the pedestal and the buffer stage

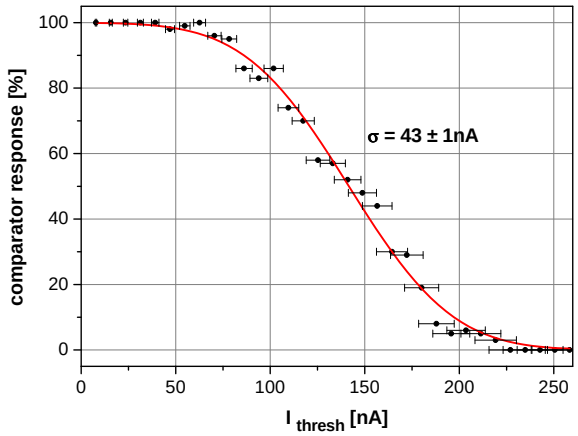

Figure 6: Noise contribution of the CURO II chip comprising an internal test current source and two sample stages. The comparator response has been fitted by an error function.

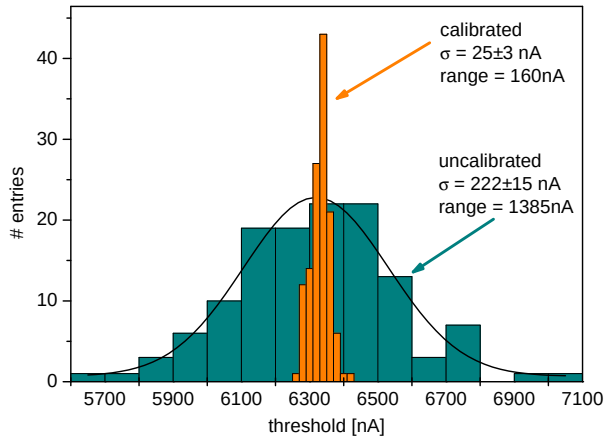

Figure 7: Channel dispersion of the comparator threshold before and after the internal calibration.

(see figure 1), this noise figure comprises of 2 memory cells and the test current source. Subtracting the noise of the current source of $i_{RMS} \approx 23\,nA$ after CDS (Correlated Double Sampling) in quadrature, the contribution of one current memory cell is $i_{RMS} = 26.0 \pm 0.8\,nA$. This number is in good agreement with the calculated value of 24.8 to 27.3 nA. With a total number of three sampling stages for the complete chip, the total noise would be $i_{RMS} = 45 \pm 1\,nA$ for the readout chain. This noise figure is fixed by the bandwidth of the sampling circuit and will neither depend on the used sampling frequency nor on the load capacitance of the sensor. However, the expected total noise has not been confirmed yet due to prominent pick-up noise in the present test system.

Channel dispersion

Any inhomogeneity in the analog channels of the chip will cause a threshold dispersion in the comparator unit. To tune all channels to a global threshold, a 5 bit DAC is implemented in every channel for calibration. The remaining dispersion after calibration should not exceed the noise performance since both figures, added in quadrature determine a lower limit of the threshold that can be used for hit discrimination. By performing threshold scans by the comparator unit as shown in figure 6 for every channel, the dispersion of the chip can be measured. Figure 7 shows the mean value of an error function fit applied to the comparator response, before and after an internal calibration of all 128 channels. Without calibration, a dispersion of 1385 nA ($\sigma = 222 \pm 15\,nA$) is observed. Such a dispersion is not tolerable since it is a factor of 5 times higher than the noise performance of the analog part. After applying the internal calibration the remaining dispersion is reduced to $\sigma = 25 \pm 3\,nA$, which is well below the noise value of the analog part. Hence, the channel dispersion in the chip imposes no limit to the threshold for hit discrimination.

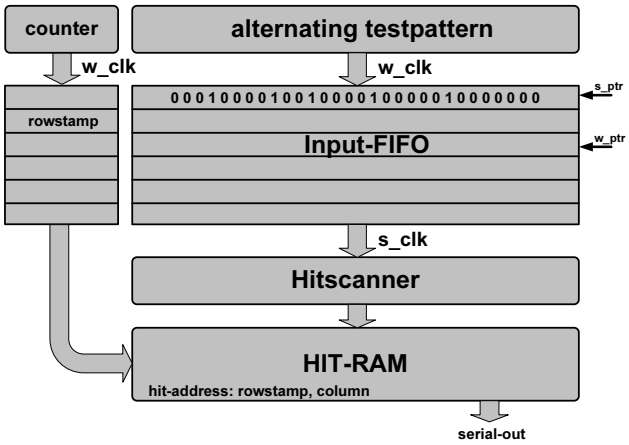

Figure 8: Schematic overview of the configuration for the digital tests.

Zero suppression and digital tests

To test the functionality of the digital part a programmable testpattern has been implemented on the chip. The schematic overview of the test configuration is shown in figure 8. The testpattern can be operated in a ring configuration so that an alternating and known pattern is applied in every cycle. After the HIT-RAM is read out, the identified hits can be compared to the alternating test pattern. The tests show that the zero suppression works up to a frequency of 110 MHz. With up to two hits found in one clock cycle the digital part outperforms the expected occupancy at the innermost layer of the vertex detector of 1.7 hits every 20 MHz by more than a factor of 5.

Power Consumption

The total power consumption of the CURO II chip has been measured at the nominal supply voltage of 2.5 V. The power consumption as a function of the operating

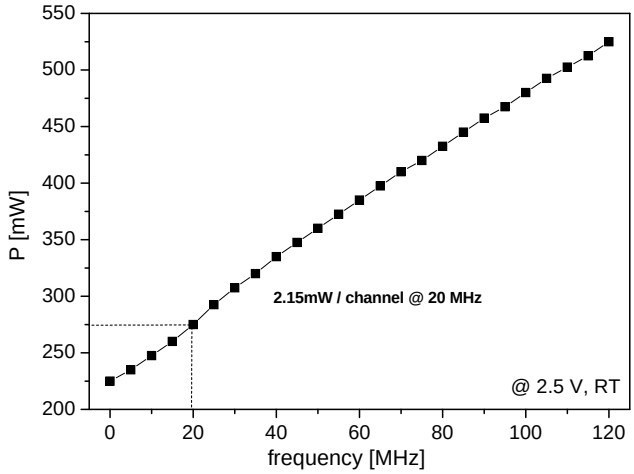

Figure 9: Total power consumption of the 128 channel readout chip CURO II as a function of the operating frequency.

frequency is shown in figure 9. A static power consumption of 1.75 mW per channel has been measured at a very low frequency (10 kHz). A total power consumption of 2.15 mW per channel is observed at 20 MHz.

IV. Conclusion

The 128 channel, CURO II ASIC has been designed and fabricated in a 0.25 μm process for a fast readout of a DEPFET pixel matrix at the ILC. The chip shows full functionality. The analog part of the chip has been operated at a frequency of 24 MHz (corresponding to 48 MSPS), which is faster than the required line rate of 20 MHz. The expected noise performance of the complete readout chain with 3-fold sampling is $i_{RMS} = 45 \pm 1$ nA. Assuming an internal amplification of the DEPFET detector of 500 pA/e^- up to 1 nA/e^-, the required noise figure below ENC=100 e^- is achievable. Zero suppression in the digital part has been successfully tested up to 110 MHz, outperforming the expected occupancy at the ILC by more than a factor of 5. With minor extensions the chip can be used for the readout of a full DEPFET pixel based vertex detector at the ILC.

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