ALICE Silicon Strip Detector Module Assembly with Single-Point TAB Interconnections

M.Oinonen[1], J.Aaltonen[2], I.Kassamakov[2], S.Nikkinen[1], Z.Radivojevic[1,3], H.Seppänen[1,2], M.Österberg[2]
V.Borshchov[4], A.Listratenko[4], V.Antonova[4], I.Tymchuk[4], M.Protsenko[4], J.Kostyshin[4], G.Zinovjev[5]
A.P.de Haas[6], P.G.Kuijer[7], G.J.L.Nooren[6,7], C.J.Oskamp[6], A.N.Sokolov[6], A.van den Brink[6]
F. Agnese[8], D.Bonnet[8], O.Clausse[8], M.Imhoff[8], C.Kuhn[8], J.R.Lutz[8], M.H.Sigward[8]
M.Bregant[9,10], L.Bosisio[9,10], P.Camerini[9,10], G.Contin[9,10], N.Grion[9], F.Faleschini[9], G.V.Margagliotti[9,10],
O.Borysov[9]

[1]Helsinki Institute of Physics, P.O.Box 64, FIN-00014 University of Helsinki, Finland
[2]Electronics Research Unit, Department of Physical Sciences, P.O.Box 64, FIN-00014 University of Helsinki, Finland
[3]Nokia Reseach Center, P.O.Box 407, FIN-00045, Helsinki, Finland
[4] SRTIIE, 40/42, Primakov str., UA-61010 Kharkiv, Ukraine
[5]National Academy of Science of Ukraine, UA-03143, Kiev-143, Ukraine
[6]Universiteit Utrecht, Faculteit Natuur- en Sterrenkunde, Princetonplein 5, NL-3584 CC Utrecht, Netherlands
[7]NIKHEF, 41882, NL-1009 DB, Amsterdam, Netherlands
[8]Institut de Recherches Subatomiques, 23 Rue du Loess, BP28, F-67037, Strasbourg, France
[9]INFN Trieste, Via A. Valerio, 2, I-34127 Trieste, Italy
[10]Universita' di Trieste, Via A. Valerio, 2, I-34127 Trieste, Italy

Abstract

The silicon strip detector (SSD) modules cover the two outermost layers of Inner Tracking System of ALICE. The SSD collaboration performs the module assembly in several locations in Europe. Mass production of the SSD modules was launched during autumn 2004 and presently all the sites are producing the SSD modules successfully. The bonding yield of spTAB interconnections is approaching close to 100%. This paper describes the assembly phases and bond process development for SSD modules, including discussion on the most probable root-causes of failures and the long-term reliability of the interconnections.

I. INTRODUCTION

The two outer layers of the Inner Tracking System (ITS) of the ALICE experiment [1] at the CERN Large Hadron Collider are made of silicon strip detector (SSD) modules. Altogether 1698 SSD modules will be installed in the ITS during 2006. Due to material budget and geometrical reasons bumpless single-point Tape Automated Bonding (spTAB) technique [2, 3] has been chosen to join the SSD components together. Description of an SSD module can be found in previous contributions to this proceeding series [3-6]. In total, the 1698 modules contain 20376 front-end chips with altogether 2.6 million channels and over 7 million bonds.

Since the ALICE experiment will take data for more than 10 years the assembly project requires careful process tuning for reliable final products. In addition, long-term reliability investigations allow for estimating the magnitude of the maintenance needs during the ALICE era.

II. ASSEMBLY PHASES

The SSD module assembly takes place in four locations in Europe: Kharkov/Ukraine, Helsinki/Finland, Strasbourg/France and Trieste/Italy. All the Al-polyimide flexes [7] are manufactured in Ukraine under supervisory of SRTIIE institute in Kharkov [8]. In addition, assembling of the so-called subhybrids is made in this institute. The three other sites take care of the final SSD module assembly and of chips and sensors production. The Netherlands group in Utrecht & NIKHEF plays a very strong role in the quality controlling of the assembly processes.

All the components are tested before assembly and the results are fed in the production database. Assembly process is characterized by 4 larger phases (Fig. 1). At first, subhybrids – containing passive SMD components on a flex - are assembled by using gluing and spTAB technique. Secondly, each HAL25 front-end chip is assembled into framed chips by spTABbing a so-called chipcable on its pads and later the active area of the chip & cable combinations is cut out for hybrid assembly. Eventually, 2 hybrids and, particularly, the input leads of the chipcables are bonded on silicon strip sensor. The assembly contains large amount of auxiliary operations: compound protection of the bonds, electrical testings and protection of sensor bonds by gluing. Finally, the geometry of the ITS requires the hybrids to be folded on top of the sensor.
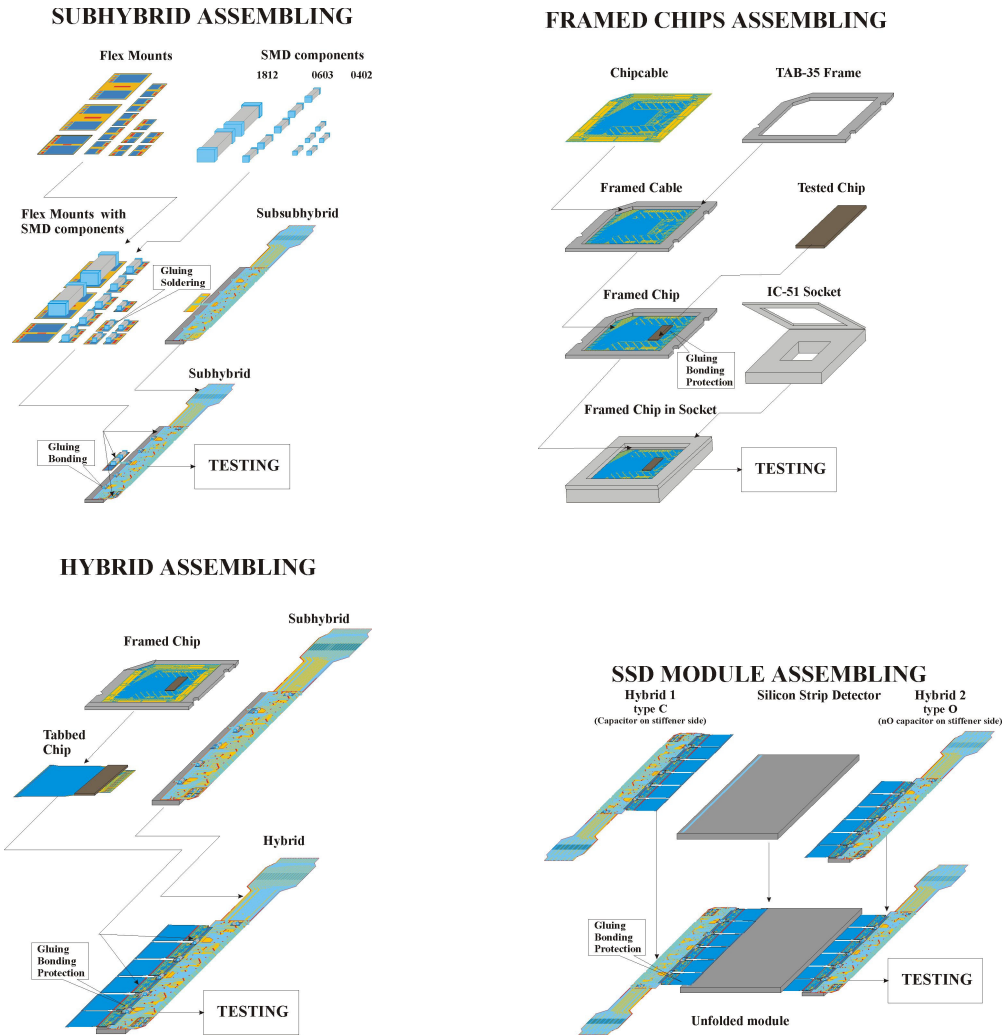
SUBHYBRID ASSEMBLING

Flex Mounts

SMD components
1812   0603   0402

Flex Mounts with
SMD components

Subsubhybrid

Gluing
Soldering

Subhybrid

Gluing
Bonding

TESTING

FRAMED CHIPS ASSEMBLING

Chipcable

TAB-35 Frame

Framed Cable

Tested Chip

Framed Chip

IC-51 Socket

Gluing
Bonding
Protection

Framed Chip in Socket

TESTING

HYBRID ASSEMBLING

Framed Chip

Subhybrid

Tabbed
Chip

Hybrid

Gluing
Bonding
Protection

TESTING

SSD MODULE ASSEMBLING

Hybrid 1
type C
(Capacitor on stiffener side)

Silicon Strip Detector

Hybrid 2
type O
(nO capacitor on stiffener side)

Gluing
Bonding
Protection

TESTING

Unfolded module

Figure 1: Assembly phases of the ALICE SSD module production.

III. SINGLE-POINT TAPE AUTOMATED BONDING IN SSD MODULES

A. Components and interconnections

In the components used, thin traces made of pure Al on a polyimide flex act as conductors. The Al traces can be ultrasonically bonded into Al pads on a Si die (chip-to-flex) or on another polyimide flex (flex-to-flex) through etched openings in the polyimide (Fig 2). Due to the ribbon shape and the softness of the Al traces extremely low bonding force can be applied for the SSD components (down to 10 cN). In Table 1 relevant properties of the components are given.

The technique has potential also in the field of microelectronics, where extremely thin and bendable dies and interconnections are required. So far, TAB interconnections have been used, for instance, in smart cards, LCD screens and inkjet printers.

Bond

Al lead

Etched window
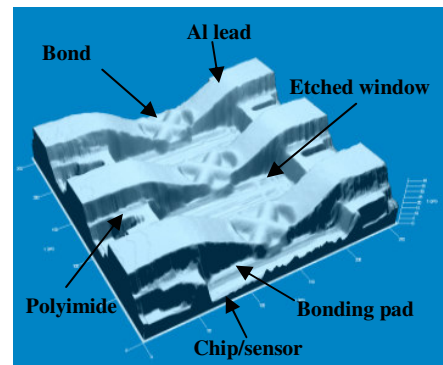
Polyimide

Bonding pad

Chip/sensor

Figure 2: 3D image of three spTAB interconnections. Bonds are made through opening etched in the polyimide base. The bond tool – when pressing the Al towards the bond pad - leaves a specific mark on the lead. The image has been recorded by Laser Scanning Microscopy.

Table 1: Properties of the components used in the SSD modules concerning the ALICE spTAB process. Three chipcable versions are used per module. This explains the number of bonds at the output zone (54 or 57).

Property	Sensor zone	Chip input zone	Chip output zone	Subhybrid zone	All
Conductor width (μm)	36	36	36	80	
Conductor thickness (μm)	14	14	14	14	
Polyimide thickness (μm)	12	12	12	12	
Contact pad dimensions (μm)	50 x 220	63 x 120	95 x 95	140 x 720	
Pitch of contact pads (μm)	95	80	125	250	
Bonds / component	1540	128	54 or 57	198	
Amount of components	1698	20376	20376	3396	
Amount of bonds (total)	2.61E+6	2.61E+6	1.12E+6	6.72E+5	7.02E+6

B. Equipment

Due to need for fast and standardized production scheme for the SSD modules, a decision was made to aim for fully automated ultrasonic (US) bonding process. Both university laboratories performing the assembly – Helsinki and Strasbourg – have chosen a similar bonder for this purpose: F & K Delvotec 6400. Main reason for the selection was the need to maintain very precise alignment –

within few μm - between the components during the bond process. The movable bondhead in the bonder serves this purpose very well since the component location is fixed. In addition, the bonder is capable of performing bonds with low force - around 10-15 cN. All bonders operate with 60 kHz ultrasonic frequency. In addition, a semiautomatic bonder Kulicke & Soffa 4523AD featuring a 60 kHz ultrasound generator is used in Helsinki for bonding the tabbed HAL25 chips into subhybrid flexes.
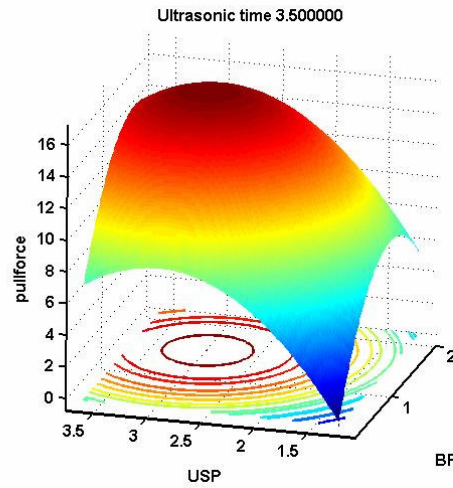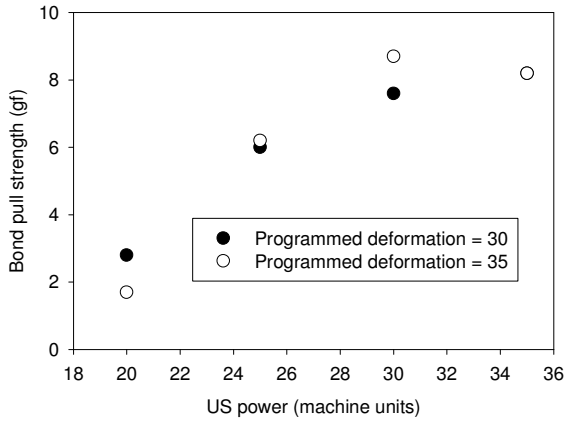

Figure 3: Examples of the typical results of the bond pull tests. Left: Bond pull strengths for chip bonds as a function of US power and with two typical "Programmed deformation" machine parameters (F & K Delvotec 6400). Right: Bond pull strength surface for hybrid bonds (K & S 4523AD). BF = bond force, USP = ultrasonic power, pull force = bond pull strength in gf.

IV. BOND QUALITY ASSURANCE

A. Pull tests

Typical results obtained via the manual, gramometer-made, pull tests for chip bonds are shown in Fig. 3 (left). The plot as a function of US power was obtained with F & K

Delvotec and with two preset deformation requirement of the Al trace by using bond force = 10 g (machine units) and US time 10 – 90 ms (US power stopped when the required deformation was reached). Each point is a result of 4 individual bonds.

Bond process parameters for chip and hybrid bonds have also been cross-checked with the Labview-controlled pull tester described in ref. [9]. The right plot in Fig. 3 shows the

results of bonds on subhybrid zone made with K & S 4123 AD bonder [10]. The US time was selected to be 3.5 machine units (~65 ms) and the bond force and US power was varied. Maximum bond pull strength until failure of about 15 gf (1 grams-force = 1 cN) was obtained and high quality bonds with ~12 gf strength were obtained within fairly wide bond process window – a typical feature of 60 kHz bonding machines.

Both methods give consistent results: typically the bond pull strength for a high quality bond reached 6 - 9 gf for bonds on chip/sensor and 12 - 15 gf for bonds on subhybrid zone. The larger bond pull strengths for the bonds on the subhybrid zone compared to chip/sensor bonds can be explained by larger width of the Al traces.

B. Bond breaking mechanisms and strengths

Nondestructive Scanning White-Light Interferometer (SWLI) [11] has been used to study bond breaking mechanisms and correlation between bond pull strength and bond height (Fig. 4). The results have been plotted in Fig. 5 for chipcable input bonds onto chip [9].
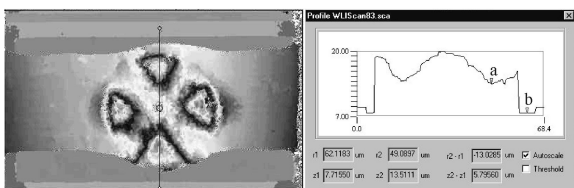

Figure 4: Left: SWLI scan of a bond. Right: profile of the bond along the line indicated in the left scan. The bond height can be measured between a) the lowest point of the bond and b) the bond pad.

Heel break type of bond failure occurs when the bond interface holds larger pull force than the wire/trace. This leads to breaking of the wire/trace under pulling, usually from the deformed interface between the bonded and the untouched material. In Fig. 5, these are shown as open circles. Under excess of bond force or US power, heel breaks are characterized by low pull strengths and low bond heights. On the other hand, too low bond parameters induce too weak or even unattached bonds leaving the trace partially or completely lifted off from the bond pad. Under pull force test such a bond shows also small strength. This behavior corresponds to lift-off cases with small bond pull strength but large bond height in Fig. 5 (closed circles).

Maximum pull strength of about 8 gf was obtained with bond heights of 3 μm. Taking 6 gf as acceptance limit for a high quality bond, "pass height" for a chipcable input bond is about 3 ± 1 μm. The error bars given can be understood based on the above discussion: beyond the error limits the above-described effects are more pronounced. The region of maximum pull strength is characterized by mixture of both lift-offs and heel breaks partly also due to difficulties to distinguish one from another type. Particularly, in these bonds a large part of Al trace is left attached on the pad after peeling

the cable off. This seems to be a characteristic feature for a high quality spTAB interconnection within our application.
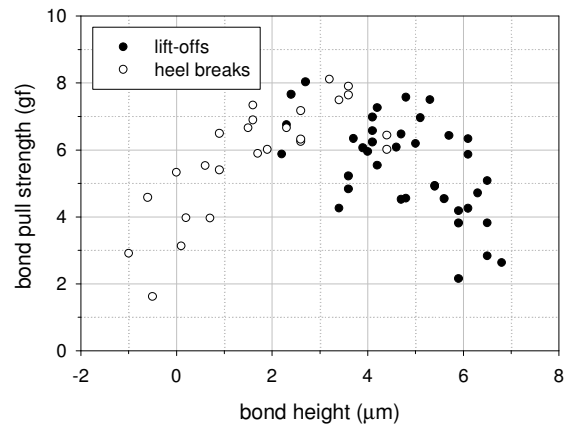

Figure 5: Bond height measured with the SWLI technique versus the measured bond pull strength for chipcable input bonds [9].

Due to the low bonding forces applied the spTAB technique is very sensitive to pad/lead contaminations. In addition, the bonding quality has been observed to be very sensitive to variations in the chipcable geometry: flatness and bonding window sizes. During the mass production practically all of the observed bonding failures seem to be lift-off type and induced by contaminations or cable geometry. For the sole industrial production site in Trieste, precautions for these are taken by using optical scanning of the microcables [12].

C. Electrical tests

Electrical functionality test for front-end chips [13] provides indirect information on the bond quality. However, one chiptest takes 30 s of time and for bond quality confirmation during mass production this is too much. Therefore, a special setup was prepared at IReS, Strasbourg for all the production sites, relying on the test of the protection diodes functionality in the front-end chips to check the electrical connections. This allows immediate testing of the connections to the bonded chip within <5 seconds.

Fig. 6 shows the yields of individual chip bonds during the mass production sessions in Helsinki. These results were obtained via the diode tests immediately after the first go with the automatic bonding machine. Average yield for individual bonds – defined as *(Bonds - Bond failures)/Bonds * 100 % -* reached 99.74 %. The dip during March-May 2005 – with only 92 % bonding yield - was related to a new production facility starting up its chipcable manufacturing. The same problems were observed also in other bonding centers and the origin was revealed to be partly contamination and partly too narrow openings in the cables. The TAB technique allows for correcting the bonding failures fairly easily: correction efficiencies of >80% can be easily reached but depending on the failure root cause. Low force and US power applied in this gentle process can most likely remove only brittle Al_2O_3

layers always present on the Al surfaces, but not likely the other contaminants.

Similar yields have been observed in other assembling sites in Strasbourg and Trieste, as well. Based on these results, one can conclude the whole ALICE SSD collaboration has tuned the automatic bonding processes well enough to be able to produce high quality spTAB interconnections.
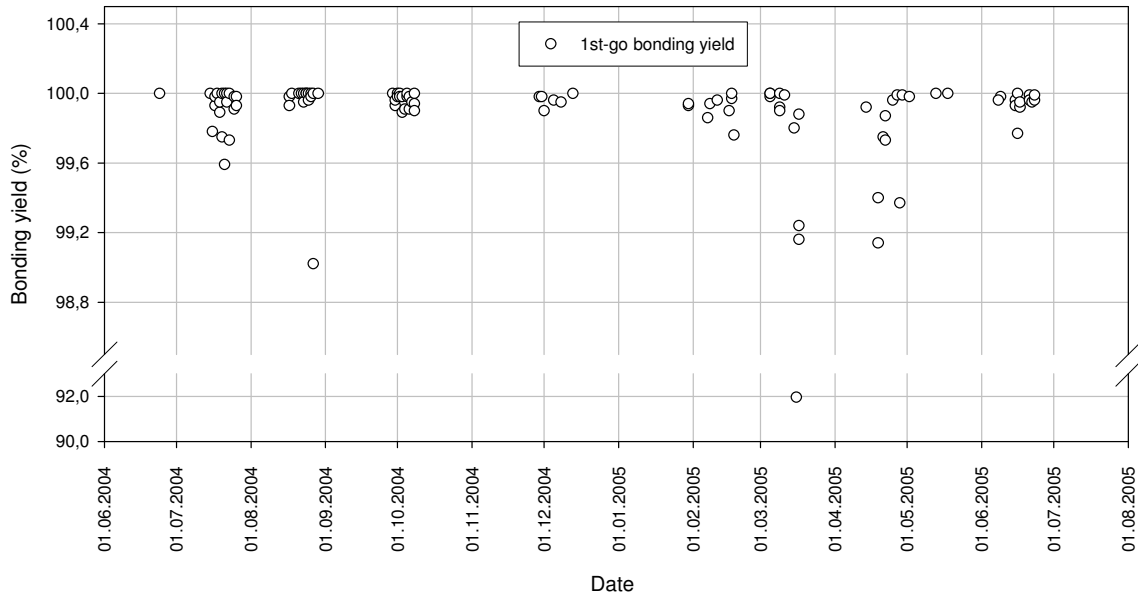

Figure 6: Bonding yield determined using diode tests along with the mass production phase in Helsinki for chip bonds. Each dot corresponds to 10 - 90 chips. The empty gaps between the sessions have been used mostly to produce the full modules with the same bonding machine.

D. Long-term reliability tests via thermal cycling

Long-term reliability of the spTAB interconnections and assemblies has been studied with thermal cycling chambers at SRTIIE / Kharkov, in the Finnish Meteorological Institute (FMI) / Helsinki and at the Helsinki Institute of Physics (HIP). The method described in [14] was used to estimate the time-to-first-failure (*TTFF*) for the bonds and assemblies. The results are given in Table 2.

In general, the interconnection failures on compound-protected framed chips under thermal cycles were noticed to commence always from the end of the bond row and successively proceed towards the center. This observation indicates thermal stresses to be responsible for these failures since the thermal expansion-based stresses are the largest at this position. The behavior is well known in the microelectronics industry [15].

The Coffin-Manson exponent *m* is an experimental quantity that defines the acceleration factor (*AF*) for failures by the relation $AF = (\Delta T_{test}/\Delta T_{pract})^m$ [13]. For Al-Al wire bonds, this has been determined to be $m = 3.5$ under thermal cycling [16, see also 14]. In the case of framed chips it was noticed that the only failures induced by cycling are the bond failures. Therefore, before more detailed experimental information on *m* is available, we adopt the value $m = 3.5$ for the *TTFF* estimation for both bonds and framed chips.

Table 2: Results of the long-term reliability studies of the ALICE assemblies. The estimates have been obtained requesting 60% confidence level (*TTFF* = time-to-first-failure).

	Chip bonds	Framed chips	Subhybrids	Subhybrids
test location	FMI/ HIP	FMI/ HIP	SRTIIE	HIP
samples	4732	26	2	6
ΔT_{test} (°C)	100	100	160	65
N_{cycles}	>782	>782	>150	>389
m	3.5	3.5	2	2
TTFF(years)	>> 20	>> 20	> 9.6	> 12.3

Analysis can also be performed for subhybrids. The analysis of the results is more challenging due to lack of complete knowledge of the failure modes to determine the applicable Coffin-Manson exponent. The exponent has been estimated to be 3-5 for hard metals and 6-9 for brittle materials whereas soft metals like solders, the value is 1-3 [14]. For conservative lifetime estimate for the flexible subhybrids we adopt the value $m = 2$.

The chip bonds and chips will most likely last the whole ALICE running period. However, during the tests it was also noticed that bonds with smaller pull strength will fail earlier.

Two experiments on subhybrids show more or less consistent results: over ~10 year lifetime. The analysis for hybrids and full SSD modules is presently under way although - as much more complicated objects - identifying of their failure modes is much more challenging task. Also, it should be noted that experimental information on the Coffin-Manson exponents for all the observed failure modes would be desirable. Therefore, reliability studies as a function of applied stress would be needed.

V. STATUS OF THE ALICE SSD MODULE ASSEMBLY

Until the end of July 2005, altogether 13600 framed chips, 1600 hybrids and 420 modules have been produced in three sites summing up to 3.45 million bonds. Auxiliary operations like complete testing and folding of the modules have been taken in use in all the sites during summer 2005. Installation of the SSD modules in ladders is foreseen to start during autumn 2005.

All these operations challenge the quality of the SSD module interconnections. By careful investigations on the interconnection quality of the components the collaboration paves the way for successful operations with the complete Inner Tracking System of ALICE and for future maintenance tasks.

VI. ACKNOWLEDGMENTS

VII. REFERENCES

[1] http://aliceinfo.cern.ch/index.html
[2] J.H.Lau, Handbook of Tape Automated Bonding. Van Nostrand - Reinhold 1992.
[3] J.-R.Lutz et al., in Proc. of 5th Workshop on Electronics for LHC Experiments, Snowmass, September 1999.
[4] ALICE Technical Design Report of the Inner Tracking System, CERN / LHCC 99-12, 18 June 1999.
[5] J.-R.Lutz et al., in Proc. of 9th Workshop on Electronics for LHC Experiments, Amsterdam, September 2003.
[6] C.Hu-Guo et al., in Proc. of 7th Workshop on Electronics for LHC Experiments, Stockholm, September 2001.
[7] A.P.de Haas et al, in Proc. of 8th Workshop on Electronics for LHC Experiments, Colmar, September 2002.
[8]http://greybook.cern.ch/programmes/experiments/lhc/instit utes/ALICE063370.html.
[9] H.Seppänen et al., in Proc. of the SPIE International Symposium "Photonics North 2004", September 27-29, Ottawa, Canada, 2004.
[10] I.Kassamakov, H.Seppänen et al., to be published (2005).
[11] J.P.Aaltonen at el., Research Programme on Future Mechnanical Engineering, 2000-2003, p. 120-126, (2003), TUKEVA Final Report.
[12] O.Borysov, M.Bregant, ALICE Internal report, ALICE-INT-2004-015, 2004.
[13] A.Sokolov et al., ALICE Internal Note, ALICE-INT-2004-028, CERN, 2004.
[14] JEDEC Publication, JEP122B, August 2003, JEDEC Solid State Technology Association, Arlington, VA, USA, p. 18-23.
[15] C.F.Dunn, J.W.McPherson, Reliability Physics Symposium, 1990. 28th Annual Proceedings, IEEE International, 27-29 March 1990, p. 252 – 258.
[16] K.J.Dittmer et al., Mat. Res. Soc. Proc. Vol 390, 1995, p. 251-256 and R.C.Blish II, Reliability Physics Symposium, 1997, 35th Annual Proceedings., IEEE International, 8-10 April 1997, p. 110 – 117.