Fast CMOS Binary Front End for Silicon Strip Detectors at LHC Experiments

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Abstract—We present design and test results of the front-end circuit developed in a 0.25 μm complementary metal-oxide semiconductor technology. The aim of this work is to study the performance of a deep submicron process in applications for fast binary front ends for silicon strip detectors. The channel comprises a fast transimpedance preamplifier working with an active feedback loop, two stages of the amplifier-integrator circuits providing 22 ns peaking time, and a two-stage differential discriminator. A particular effort has been made to minimize the current and the power consumption of the preamplifier, while keeping the required noise and timing performance. For a detector capacitance of 20 pF noise below 1500 e$^-$ equivalent noise charge (ENC) has been achieved for 300 μA bias current in the input transistor, which is comparable with the levels achieved in the past for the front end using a bipolar input transistor. The total supply current of the front end is 600 μA and the power dissipation is 1.5 mW per channel. The offset spread of the comparator is below 3 mV rms.

Index Terms—Front-end electronics, low noise circuits, noise modeling, noise optimization.

I. INTRODUCTION

THE aim of the presented work is to study the performance of a deep submicron process in applications for fast binary front-ends for silicon strip detectors as used, for example, in the ATLAS Semiconductor Tracker. Although the front-end application-specific integrated circuits (ASICs) have been already developed and produced for silicon detectors in all Large Hadron Collider (LHC) experiments, it is worth to study the possibility of further improvements of the performance and radiation hardness of the front-end ASICs using submicron technologies. On the other hand, given the trends in the technology, one needs to investigate performance of the new processes and develop new circuits, which are suitable for realization in submicron processes.

A particular goal of this work is to develop a front-end circuit, which is compatible with the requirements of the binary readout architecture as implemented in the ABCD ASIC for readout of silicon strip detectors in the ATLAS Semiconductor Tracker [1]. The ABCD chip has been developed in the DMILL technology, a BiCMOS radiation-hardened process with a minimum feature size of 0.8 μm. The front-end circuit of the ABCD design employs extensively bipolar transistors. The critical requirements of the chip regarding the noise, matching of the comparator, and power consumption are satisfied by circuit designs, which use advantages of the bipolar transistors.

The parameters of the ABCD ASIC, which are known to satisfy the requirements of the ATLAS Semiconductor Tracker, are used as a reference for the presented new development using a commercial 0.25 μm CMOS process.

II. DESIGN OF SINGLE CHANNEL

The schematic diagram of one channel of the ABCDC1 chip is shown in Fig. 1. Each channel comprises three basic blocks: fast transimpedance preamplifier, shaper providing additional amplification, and integration of the signal, and differential discriminator stage.

A. Preamplifier Design

The preamplifier is based on a classical cascode configuration with an NMOS input transistor of size 2000 μm/0.5 μm. The nominal bias current of the input transistor is in the range 300 to 600 μA, which allows for operating that device close to weak inversion and, consequently, ensures a low value of the excess noise Γ factor. The total gate capacitance of the input transistor for the nominal bias is in the range of 4 pF. The dimensions of the input transistor were optimized using the Enz, Krummenacher, Vittoz (EKV) parameterization, taking into account the channel thermal noise, the gate induced current noise, and correlation of these two noise sources as well as the flicker noise.

The active feedback circuit offers much lower parasitic capacitance of the feedback loop compared to a resistive feedback using low-resistivity polysilicon resistors available in the process used. Although the noise performance of the active feedback is worse than in case of a passive feedback resistor, as will be shown later, it is still possible to keep its noise at the acceptable level by proper choice of the feedback current. The nominal value of the feedback current of 0.8 μA provides the required fast discharge of the preamplifier with a time constant of about 13 ns as well as an acceptable level of the parallel noise, of about 400 e$^-$ equivalent noise charge (ENC). For silicon strip detectors with a total strip capacitance of 20 pF, the series noise dominates the ENC anyway.

An additional branch of the current source load connected directly to the input transistor supplies the required bias current without degradation of the cascode output impedance. The open-loop gain of the preamplifier is about 83 dB and the gain-bandwidth product is in the range of 600 MHz. This results in a low input impedance of the preamplifier, of the order of 120 to 200 Ω at the central frequency of the shaper bandwidth (Fig. 2).
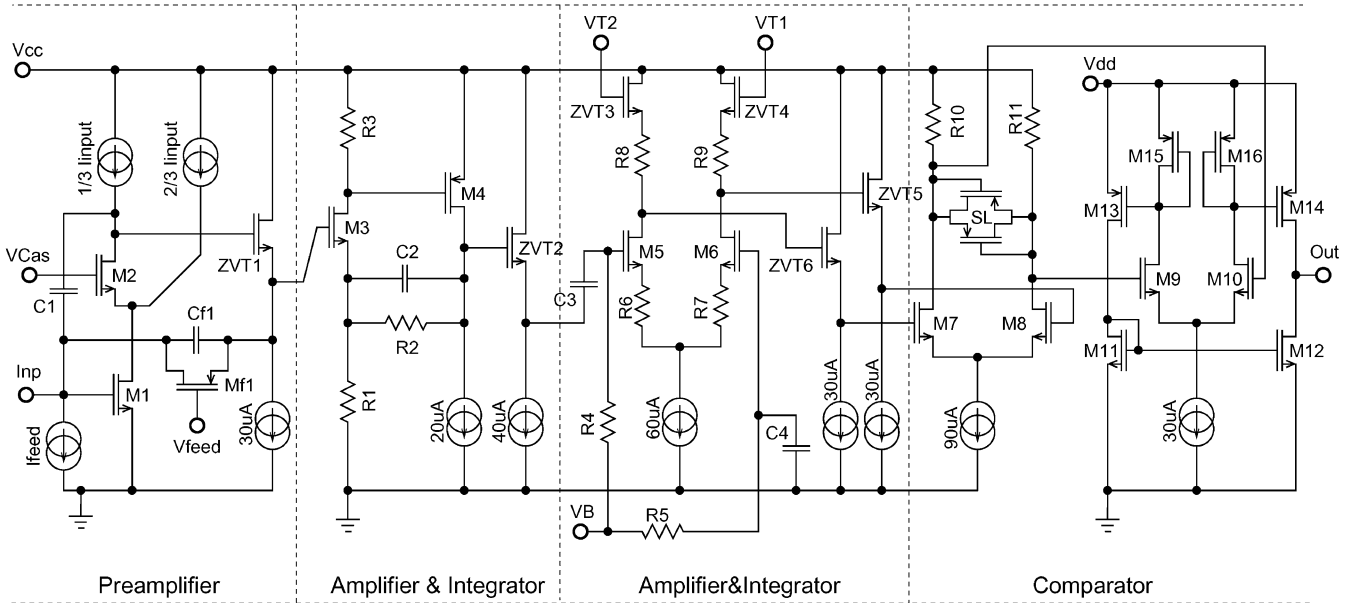
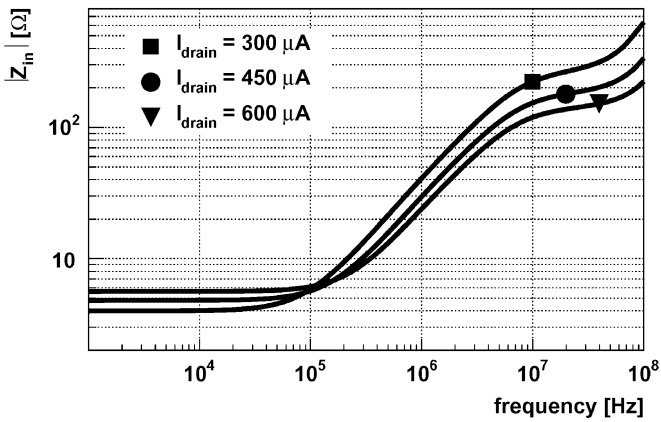Fig. 1.   Schematic diagram of one channel of the ABCDC1 chip.

Fig. 2.   Input resistance of the preamplifier simulated for 800 nA bias current of the feedback transistor and various input transistor bias currents.
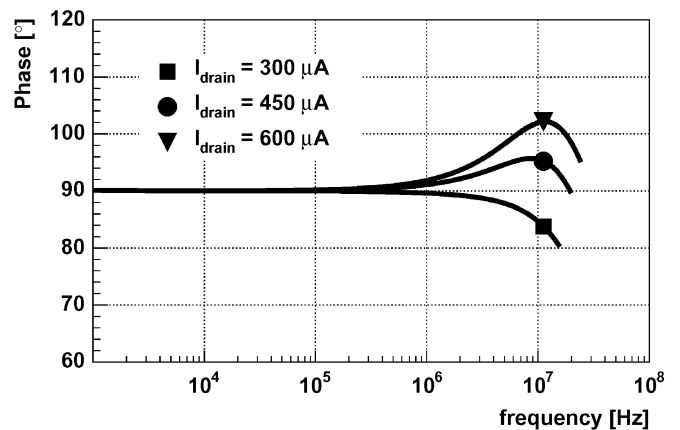

Fig. 3.   Simulation of the preamplifier phase margin for 800 nA bias current of the feedback transistor, nominal 20 pF input capacitance, and various input transistor currents.

Low input impedance ensures small crosstalk between channels via the interstrip capacitance and a relatively small loss of input charge on the detector capacitance.

The phase compensation of the preamplifier stage is provided by two capacitors Cf1 and C1 with the total capacitance of 190 fF, which also decreases the input impedance for high frequencies. A large phase margin, above $80°$, is obtained for a wide range of bias conditions of the preamplifier and the feedback circuit. The simulation results of phase margin for different bias condition are shown in Fig. 3.

The principle of the active feedback preamplifier (AFP) is described in [2]. Transistor Mf1 is placed in the feedback path of the cascode stage instead of a conventional feedback resistor as in a classical transresistance amplifier. Transistor Mf1 works in saturation and is biased in moderate inversion. For the nominal bias current of 0.8 μA, the transconductance of Mf1 is about 8 μS, which is equivalent to a 120 kΩ feedback resistor. The pulse gain of that stage for a nominal bias condition (300 to 600 μA input transistor current, 0.8 μA feedback current) and 20 pF input capacitive load is about 4 mV/fC.

B. Shaper Design

The first integrator stage is built from a voltage amplifier consisting of two cascaded common-source amplifiers. The following differential pair, which is ac coupled to the first integrator stage, provides an adjustment of the gain and of the peaking time of the entire signal chain. The entire preamplifier-shaper circuit has a gain of 60 mV/fC and a peaking time of 22 ns.

The differential pair translates the external differential threshold voltage VT1-VT2 for the internal threshold of the comparator. A fully differential structure of the comparator provides very good rejection of the common-mode noise from the digital power supply and good threshold uniformity. The goal of the design is to keep the threshold spread below 5% of the nominal threshold value, i.e. 60 mV corresponding to 1 fC of the input charge. This requires the comparator offset spread be below 3 mV rms.

C. Comparator Design

The differential gain of the comparator input stage is $\sim$28 dB. A high gain in combination with threshold voltage ranging from

0 to 800 mV may lead to saturation of the stage. To prevent the saturation, a swing limiter based on PMOS devices has been employed. The second section of the comparator is a classical two-stage amplifier with very high dc gain (∼72 dB). The current switched during the transitions is limited by the current source which biases that stage.

The last stage of the comparator is supplied from the digital power supply. It has been found that this configuration of the power supply provides a very high rejection of the interferences (up to 56 dB) from the digital power supply to the analogue part of the circuit (comparator input). The dc gain of the comparator is in the range of 100 dB, and the minimum overdrive of the comparator for fast pulses delivered from the shaper is roughly 3 mV.

An important parameter of the discriminator is the time walk. In our case, this parameter is defined for the comparator connected to the whole front-end amplifier. Thus, we combine all timing effects, peaking time of the amplifier, and response delay of the comparator itself into one number. The time walk is defined as the difference of the comparator response delays for input charges of 1.2 and 10 fC while the comparator threshold is set at 1 fC. For a nominal input load and bias of the front end, the total time walk has been simulated to be 12 ns.

III. NOISE OPTIMIZATION OF THE PREAMPLIFIER STAGE

As already mentioned, for the intended application for readout of long silicon strips, the series noise of the preamplifier is dominant. Since the peaking time of the shaper (22 ns) is defined by the required timing resolution, it cannot be tuned to optimize the ENC of the system, and the only possibility to reduce the noise in this case is to increase the transconductance of the input transistor. For the MOS transistors, this can be done by increasing the transistor bias current and by optimization of the transistor dimensions. Increasing the width of the transistor gate moves the operating point closer to weak inversion and improves the device transconductance. Increasing the gate width results also in an increase of the total area and total capacitance of the gate, which increases the series noise contribution to the ENC. For a given detector capacitance, a clear optimum for the size of the input transistor can be found.

An important parameter, which has to be taken into account, is the bias current of the input device. It contributes significantly to the power consumption of the whole chip and, therefore, it should be considered together with the noise performance for the final choice of the architecture (single ended) and the input device type (NMOS).

The choice of the gate length of the NMOS transistor is determined by minimization of the excess noise factor Γ, which becomes worse in short-channel devices. For the used 0.25 μm technology, a gate length of 0.5 μm for the NMOS devices ($\Gamma = 1.3$ [3]) is optimal from this point of view. Further increase of the gate length does not affect the Γ factor and leads to the enlargement of the total gate area, which degrades the noise performance.

In order to describe accurately the noise performance of the MOS transistor for a wide range of the bias currents and transistor dimensions, one must calculate precisely the transconductance and intrinsic gate capacitances for each current density. In our work, we have used an analytical EKV model [4], which provides continuity between weak, moderate, and strong inversion. Since the presented analysis is focused on the noise performance of MOS devices, we simplify the general model assuming that the transistors work in saturation between the weak and moderate inversion. The definitions of physical constants and model parameters used in the calculation are given in Table I.

A. Modeling of the Transconductance and Intrinsic Gate Capacitance

The classical formulae describing the transconductance in the EKV model are given by (1)–(3). The specific current I_S used for the normalization is described as

$$I_S = 2n\beta U_T^2 \quad \text{where } \beta = K_P \frac{W}{L}, \quad U_T = \frac{kT}{q} \quad (1)$$

The transconductance of the MOS transistor is normalized to the maximum value, which can be reached in the weak inversion. The function used for interpolation of the transconductance between strong and weak inversion for a given drain current I_D is described by

$$G(I_f) = \frac{1}{\sqrt{I_f + \frac{1}{2}\sqrt{I_f} + 1}} \quad \text{where } I_f = \frac{I_D}{I_S} \quad (2)$$

Finally, the transconductance of an MOS transistor biased in weak and moderate inversion is given by

$$g_m = G(I_f)\frac{I_D}{nU_T} \quad (3)$$

Fig. 4 shows a comparison between the transconductance simulated with the EKV model and measured for an NMOS transistor of dimensions 2000 μm/0.5 μm, covering the weak and moderate inversion regions of operation.

Another transistor parameter which needs to be calculated is the gate capacitance. It is a sum of the intrinsic gate capacitance and the gate-to-source and gate-to-drain overlap capacitances. For an MOS transistor working in saturation, the intrinsic gate
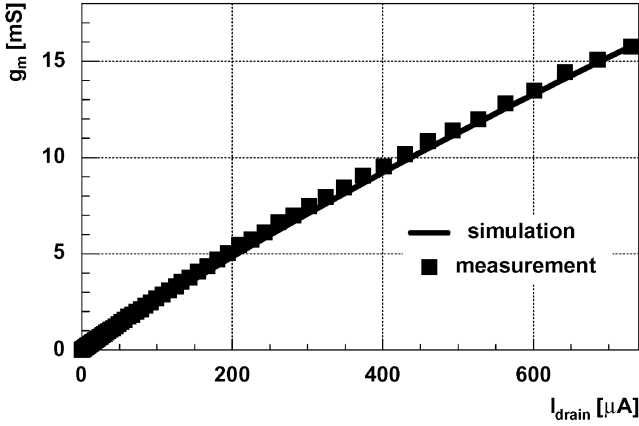
TABLE I
DEFINITIONS OF PHYSICAL CONSTANTS AND MODEL PARAMETERS FOR CMOS 0.25 μm TECHNOLOGY USED IN THE ANALYSIS

k	Boltzmann's constant	1.3806×10^{-23} J/K
q	Electron charge	1.6021×10^{-19} C
ε_{OX}	Permitivity of SiO$_2$	3.45×10^{-11} F/m
T	Temperature	K
f	Frequency	Hz
ω	Angular frequency	$2\pi f$ rad/s
n	Slope factor	1.45
t_{OX}	Effective gate oxide thickness	6×10^{-9} m
K_P	Transconductance parameter $\mu_0 C_{OXU}$	NMOS 300 μA/V^2
		PMOS 70 μA/V^2
W, L	Width and length of the transistor	μm

Fig. 4. Comparison between measured and calculated transconductances of an NMOS transistor of dimensions 2000 μm/0.5 μm for a wide range of drain current.

capacitance has two components described by the following formulae:

— gate-to-source capacitance

$$C_{\mathrm{GS}} = C_{\mathrm{OX}} \left(\frac{1}{I_f G(I_f)} + \frac{3}{2} \right)^{-1} \quad \text{where } C_{\mathrm{OX}} = WL \frac{\varepsilon_{\mathrm{OX}}}{t_{\mathrm{OX}}} \tag{4}$$

— gate-to-bulk capacitance

$$C_{\mathrm{GB}} = C_{\mathrm{OX}} \frac{n-1}{n} \left(1 - \frac{I_f G(I_f)}{1 + \frac{3}{2} I_f G(I_f)} \right) \tag{5}$$

The two overlap capacitances: gate-to-drain and gate-to-source are of the order 0.4 fF/μm for the technology used. Note that for the transistor dimensions considered, these capacitances contribute a large fraction of the total gate capacitance.

B. Modeling of Noise

For calculation of the thermal noise, we use the model proposed by van der Ziel [5], but slightly modified for weak and moderate inversion regions [4]. For relatively large MOS transistors, as used in the input stage of our design, we take into account the gate-induced current noise (GIC), since its spectral density is proportional to the gate capacitance C_{OX}.

Taking into account both transconductances g_m and g_{mb}, contributing to the channel thermal noise, the spectral density of the thermal noise i_{nd} in the MOS transistor can be described by the following equation [4]:

$$\overline{i_{\mathrm{nd}}^2} = 4kTG_{N\mathrm{th}}\Delta f \quad \text{where } G_{N\mathrm{th}} = \gamma(g_{\mathrm{mb}} + g_m) = \gamma n g_m \tag{6}$$

The bias dependent parameter γ takes values from $1/2$ to $2/3$ for the ideal transistor operating in the weak and the strong inversion, respectively. The model works well for long channel devices. The excess noise observed in short channel devices can be modeled using numerical methods [6]. In a more practical

approach, one introduces an excess noise factor Γ. It can be incorporated together with an interpolating function $F_n(I_f)$ determining the γ factor for a given region of operation ([4] and [7])

$$\gamma = F_n(I_f)\Gamma \quad \text{where } F_n(I_f) = \frac{1}{1 + I_f} \left(\frac{1}{2} + \frac{2}{3} I_f \right) \tag{7}$$

For the process used, the Γ factor is between 1.3 and 1.25 for NMOS and PMOS transistors with gate lengths greater than 0.5 μm and 0.4 μm, respectively, working in the weak and moderate inversion regions [3].

The spectral density of the high-frequency GIC noise was originally analyzed by van der Ziel for an ideal MOS transistor working in saturation and strong inversion [5]. According to [6], the high-frequency GIC excess noise rises together with the excess thermal noise. This is expected since the origin of the GIC noise is the coupling of fluctuations of the current thermal noise from the transistor channel. Consequently, the gate-induced current noise for a nonideal device, independent of the region of operation can be estimated as follows [5]:

$$\overline{i_{\mathrm{ng}}^2} = 8\gamma kT g_{\mathrm{gs}}\Delta f \quad \text{where } g_{\mathrm{gs}} = \frac{4}{45} \frac{\omega^2 C_{\mathrm{OX}}^2}{n g_m} \tag{8}$$

For complete evaluation of thermal noise in the MOS transistor, one has to take into account the correlation between channel thermal noise i_{nd} and gate-induced noise i_{ng}. For the correlation coefficient equal to $j\sqrt{5/32}$ [5], one obtains the correlation term as

$$\overline{i_{\mathrm{ng}} i_{\mathrm{nd}}^*} = \frac{\gamma}{6} \omega C_{\mathrm{OX}} 4T\Delta f \tag{9}$$

The next source of noise taken into account in this analysis is the flicker noise. In the commonly used model of the flicker noise, the current noise generator is placed in between the drain and source of the MOS transistor. The power spectral density is given as

$$\overline{i_{\mathrm{nf}}^2} = \frac{K_a}{f} \frac{g_m^2}{C_{\mathrm{OXU}}^2 WL} \Delta f \quad \text{where } C_{\mathrm{OXU}} = \frac{\varepsilon_{\mathrm{OX}}}{t_{\mathrm{OX}}} \tag{10}$$

For the process used, the technology-dependent parameter K_a is equal to 6×10^{-27} and 1×10^{-27} C^2/m^2 for NMOS and PMOS devices, respectively. These are worst case post-radiation values [3].

The equivalent schematic of the transimpedance preamplifier including all discussed noise sources related to the input transistor and the feedback circuit is shown in Fig. 5.

C. Calculation of the Preamplifier Output Noise

Assuming that the circuit is linear, one can identify the contributions to the output noise from each noise source described by (6), (8), and (10), separately. Although for the elementary noise sources, the propagation of the noise fluctuation to the preamplifier output may be calculated directly in the frequency domain, the calculation of the correlation term between thermal and GIC
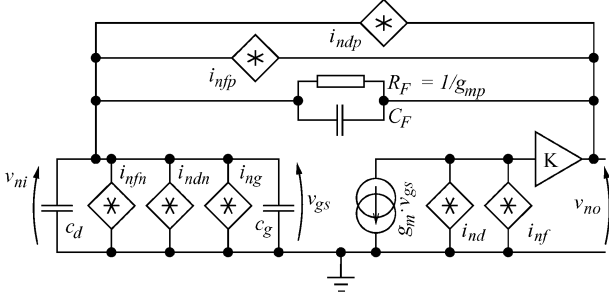
Fig. 5. Equivalent schematic of the MOS transimpedance preamplifier with active feedback including all noise sources related to the input transistor and feedback circuit.

noise is more complex. For clarity, let us consider only two noise sources i_{ng} and i_{nd}.

Assuming sufficiently wide bandwidth and high gain of the preamplifier stage and using elementary network theory, one finds the output noise in the time domain as

$$v_{no}(t) = \frac{i_{nd}(t)}{g_m} Z_F Y_T + i_{ng}(t) Z_F \qquad (11)$$

where

$$Y_T = Y_F + Y_g + Y_d, \quad Z_F = \frac{1}{Y_F} = \frac{R_F}{1 + j\omega\tau_f},$$
$$\tau_f = R_F C_F$$
$$Y_d = j\omega c_d, \quad Y_g = j\omega c_g \qquad (12)$$

Expanding the noise sources for Fourier series

$$i_{nd}(t) = \sum_{n=-\infty}^{\infty} a_n \exp(j\omega t) \qquad (13)$$

$$i_{ng}(t) = \sum_{n=-\infty}^{\infty} b_n \exp(j\omega t) \qquad (14)$$

$$v_{no}(t) = \sum_{n=-\infty}^{\infty} d_n \exp(j\omega t) \qquad (15)$$

and inserting them into (11), one finds the following relation between n-terms of Fourier series:

$$d_n = a_n \frac{Z_F}{g_m} Y_T + b_n Z_F \qquad (16)$$

Consequently, the spectral density of the output noise is given as

$$\frac{\overline{v_{no}^2}}{\Delta f} = \overline{d_n d_n^*} = \overline{\left(a_n \frac{Z_F}{g_m} Y_T + b_n Z_F\right)\left(a_n^* \frac{Z_F^*}{g_m} Y_T^* + b_n^* Z_F^*\right)} \qquad (17)$$

After some algebra, one obtains

$$\frac{\overline{v_{no}^2}}{\Delta f} = \overline{a_n a_n^*} \frac{|Z_F|^2}{g_m^2} |Y_T|^2 + \overline{b_n b_n^*} |Z_F|^2$$
$$+ 2\mathrm{Im}[\overline{b_n a_n^*}] \frac{|Z_F|^2}{g_m} |Y_T| \qquad (18)$$

Then, using (6), (8), and (9), one obtains the following expression for the spectral density of the output noise:

$$\frac{\overline{v_{no}^2}}{\Delta f} = \frac{\overline{v_{no\_id}^2}}{\Delta f} + \frac{\overline{v_{no\_GIC}^2}}{\Delta f} + \frac{\overline{v_{no\_corr}^2}}{\Delta f} \qquad (19)$$

where

$$\frac{\overline{v_{no\_id}^2}}{\Delta f} = \frac{4kT\gamma n}{g_m}\left(\omega^2(c_d+c_g+C_F)^2 + \frac{1}{R_F^2}\right)\frac{R_F^2}{1+\tau_f^2\omega^2} \qquad (20)$$

$$\frac{\overline{v_{no\_GIC}^2}}{\Delta f} = \frac{32}{45}kT\gamma\frac{\omega^2 C_{OX}^2}{ng_m}\frac{R_F^2}{1+\tau_f^2\omega^2} \qquad (21)$$

$$\frac{\overline{v_{no\_corr}^2}}{\Delta f} = \frac{8}{6}\frac{\gamma kT}{g_m}\omega^2 C_{OX}(c_d+c_g+C_F)\frac{R_F^2}{1+\tau_f^2\omega^2} \qquad (22)$$

Keeping in mind that c_g is much larger than C_F, one can simplify (20) for the frequencies within the bandwidth of the shaper stage to

$$\frac{\overline{v_{no\_id}^2}}{\Delta f} = \frac{4kT\gamma n}{g_m}\omega^2(c_d+c_g+C_F)^2\frac{R_F^2}{1+\tau_f^2\omega^2} \qquad (23)$$

In a similar way, one can find the contribution of the flicker noise to the preamplifier output noise as

$$\frac{\overline{v_{no\_f}^2}}{\Delta f} = \frac{K_a}{fC_{OXU}^2 WL}\omega^2(c_d+c_g+C_F)^2\frac{R_F^2}{1+\tau_f^2\omega^2} \qquad (24)$$

D. Noise Optimization of the Input Transistor

Because of the limited preamplifier bandwidth and compromise between the bandwidth and power consumption of the following stages, it is not feasible to match the time constants in all signal processing stages, as in the case of the ideal CR-(RC)^n shaper. The overall shaping function of the front-end amplifier can be represented by one stage of CR-(RC)^1 filter with a time constant equal to 13 ns, followed by two stages of integrators with a time constant equal to 4 ns, and one ac coupling with the time constant of 300 ns. Since there is no analytical solution for the amplitude response of the real circuit, we approximate the real transfer function with the ideal CR-(RC)^3 filter characteristic, applying numerically calculated correction factors for the considered noise sources. The correction factors for noise related to the input transistor and feedback circuit are equal to 0.999 and 1.18, respectively. They have been applied to the calculated ENC figures (Figs. 6, 7, and 11) but not to the analytical formulas (27)–(33), showing ENC in case of ideal CR-(RC)^3 shaping.

The rms noise at the output of ideal CR-(RC)^3 shaper σ_{nfo} can be calculated as

$$\sigma_{nfo} = \left(\int_0^\infty \frac{\overline{v_{no}^2}}{\Delta f}\frac{1}{\left(1+\tau_f^2\omega^2\right)^3}\partial f\right)^{\frac{1}{2}} \qquad (25)$$

where v_{no} represents all partial contributions of thermal noise, GIC noise, correlation term, and flicker noise sources related to
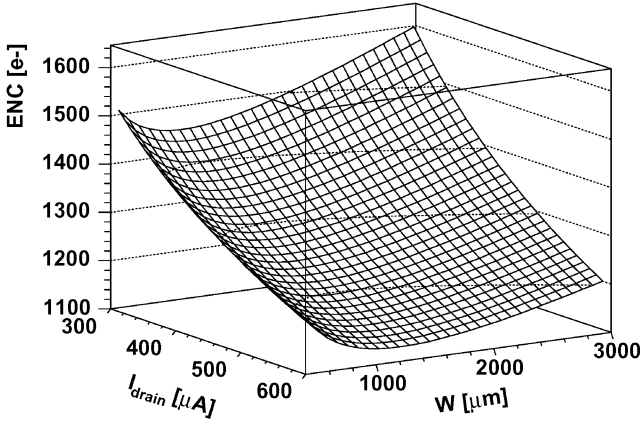
Fig. 6. ENC as a function of bias current and input transistor width for 22 ns peaking time and detector capacitance of 20 pF.
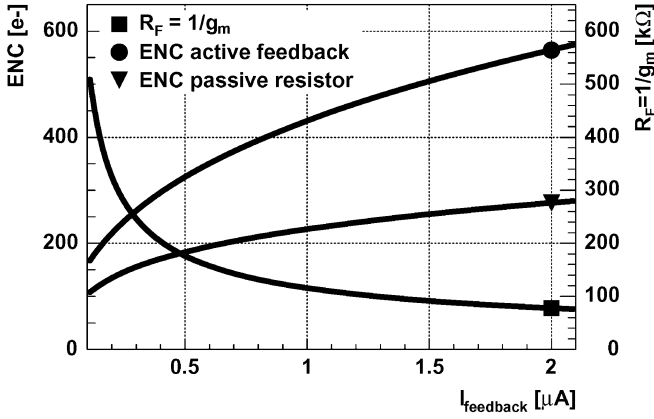

Fig. 7. Comparison of the ENC generated by an active feedback and by a passive resistor of the same equivalent resistance for the peaking time of 22 ns. The left axis shows the ENC and the right axis shows the equivalent feedback resistance.

the input transistor ((21)–(24)). Finally, the ENC is calculated as following:

$$\text{ENC}[e^-] = \frac{\sigma_{nfo}}{q\text{Gain}} \quad \text{where Gain} = \frac{9}{2e^3}\frac{1}{C_F} \quad (26)$$

Each term of (25), corresponding to a different noise source, can be integrated separately to find the partial contribution to equivalent noise charge. The contributions of the thermal, GIC and flicker noise as well as correlation terms related to the input transistor are as follows:

$$\text{ENC}_{\text{Id}}[e^-] = \frac{e^3}{12\sqrt{3}}\sqrt{\frac{4kTn\gamma}{g_m}\frac{c_d + c_g + C_F}{\sqrt{t_{\text{peak}}}}}\frac{1}{q} \quad (27)$$

$$\text{ENC}_{\text{GIC}}[e^-] = \frac{e^3\sqrt{2}}{9\sqrt{15}}\sqrt{\frac{kT\gamma}{ng_m}\frac{C_{\text{OX}}}{\sqrt{t_{\text{peak}}}}}\frac{1}{q} \quad (28)$$

$$\text{ENC}_{\text{If}}[e^-] = \frac{e^3\sqrt{2}}{9\sqrt{3}}\sqrt{\frac{K_a}{WL}\frac{c_d + c_g + C_F}{C_{\text{OXU}}}}\frac{1}{q} \quad (29)$$

$$\text{ENC}_{\text{corr}}[e^-] = \frac{e^3}{18}\sqrt{\frac{kT\gamma}{g_m}\frac{\sqrt{C_{\text{OX}}(c_d + c_g + C_F)}}{\sqrt{t_{\text{peak}}}}}\frac{1}{q} \quad (30)$$

The final ENC figure shown in Fig. 6, taking into account all considered noise sources, can be obtained by quadratic summing of the partial contributions (27)–(30).

For the nominal detector capacitance of 20 pF and the peaking time of 22 ns, there is shallow optimum for the width of the input transistor between 1000 and 2000 μm. In the presented design, the width of the input transistor is set to 2000 μm, which helps to keep the excess noise factor Γ low as it tends to increase toward the strong inversion region [3].

E. Modeling of the Noise Contribution of the Active Feedback Loop

The equivalent schematic of the amplifier, including the noise sources associated with the feedback PMOS transistor and the NMOS current source (which determines the feedback current) is shown in Fig. 5. Both components contribute channel thermal noise (i_{ndp} and i_{ndn}) as well as flicker noise (i_{nfn} and i_{nfp}). One may depict the noise spectra density related to the feedback circuit $v_{\text{no\_feed}}$ at the preamplifier output as

$$\frac{\overline{v_{\text{no\_feed}}^2}}{\Delta f} = \frac{R_F^2}{1 + \tau_f^2\omega^2}\left(\overline{i_{nfn}^2} + \overline{i_{nfp}^2} + \overline{i_{ndn}^2} + \overline{i_{ndp}^2}\right) \quad (31)$$

Assuming a CR-(RC)^3 shaper circuit and computing the integrals for the flicker and thermal noise separately for the NMOS and PMOS transistor, one obtains the expressions for the corresponding ENC contributions from each noise source. The ENC contribution from the thermal noise of each feedback transistor is given as

$$\text{ENC}_{\text{th}}[e^-] = \frac{e^3}{18}\sqrt{\frac{5}{3}}\sqrt{kTn\gamma g_m t_{\text{peak}}}\frac{1}{q} \quad (32)$$

Note that the definite integrals of the components related to the flicker noise of feedback devices do not converge for frequencies decreasing toward zero. The problem is resolved by taking into account the ac coupling between preamplifier-shaper and discriminator stages, which helps to filter that noise. Assuming the time constant of the ac coupling in the presented chip to be roughly 300 ns, one obtains the following expression for the ENC due to the flicker noise of each feedback transistor:

$$\text{ENC}_{1/f}[e^-] \approx 2.3g_m t_{\text{peak}}\sqrt{\frac{K_a}{WL}}\frac{1}{C_{\text{OXU}}}\frac{1}{q} \quad (33)$$

Fig. 7 shows the ENC (left axis) and the equivalent feedback resistance (right axis) as a function of the feedback current. The same plot shows for comparison, the noise of an equivalent passive resistor.

The current required to obtain the feedback resistance in the range of 120 kΩ is around 0.8 μA. For this current, the parallel noise due to the AFP circuit is about 400 e$^-$ ENC, whereas the noise of a passive resistor in the feedback would be about 200 e$^-$ ENC. As mentioned before, the use of AFP instead of simple resistive feedback was determined by the possibility of obtaining a much higher bandwidth of the preamplifier stage.

IV. TEST RESULTS

In the prototype chip of area 4×4 mm^2, we have placed 56 regular channels and eight analog channels consisting of a preamplifier and shaper. The dimensions of one channel are:
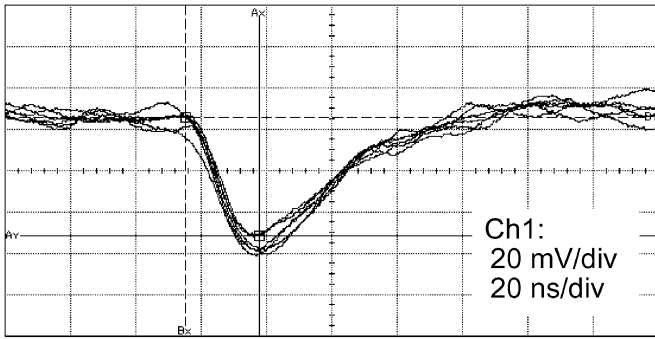
Fig. 8.   Response of the preamplifier/shaper stage to a charge signal of 3.5 fC for 800 nA feedback current, an input transistor bias of 300 μA, and 20 pF input load capacitance (ENC of about 1500 e$^-$).

$42\ \mu$m $\times$ 2 mm. The functionality of the full chain can be tested by issuing calibration pulses distributed to all channels with four calibration lines. Each channel has an internal 100 fF capacitor connected between its input and a calibration line. Every fourth channel can be tested simultaneously when one calibration line is used. The basic analog parameters of the amplifier were measured for different bias and input capacitance using the analog test channels.

The gain, offset, and noise of the full chain including the comparator were evaluated by scanning the discriminator threshold for a given input charge applied from a pulse generator. For each threshold value, a series of pulses was applied and the fraction of these pulses that fired the comparator was measured. By performing these measurements for several values of calibration signals, we have extracted the gain, offset, and noise of the full chain.

A. Analog Measurements

The response of the preamplifier shaper for nominal bias, input capacitance of 20 pF, and input charge of 3.5 fC is shown in Fig. 8.

The dynamic range and linearity of the analog chain for nominal as well as for the corner process parameters and limited power supply are shown in Fig. 9. Good linearity is maintained up to input charges of 12 fC. One can observe a few percent change in the gain for chips from the corner runs and almost no difference for the lowered power supply.

The measurements of the peaking time and noise as a function of the input capacitance for different values of the input transistor bias are shown in Figs. 10 and 11, respectively. Small dependence of the peaking time on the input capacitance (<100 ps/pF) confirms the low value of the input impedance of the preamplifier. The noise performance of the amplifier agrees well with the presented noise model. For the nominal input capacitance 20 pF and 300 μA input transistor bias current, the ENC is of the order of 1500 e$^-$.

B. Full Signal Chain Measurements

The measurements of the full signal chain were performed for all channels equipped with the test capacitors to evaluate the channel-to-channel variation of the gain, comparator offset, and time walk. The gain and ENC for the nominal bias conditions agree well with the values obtained for the test channels.
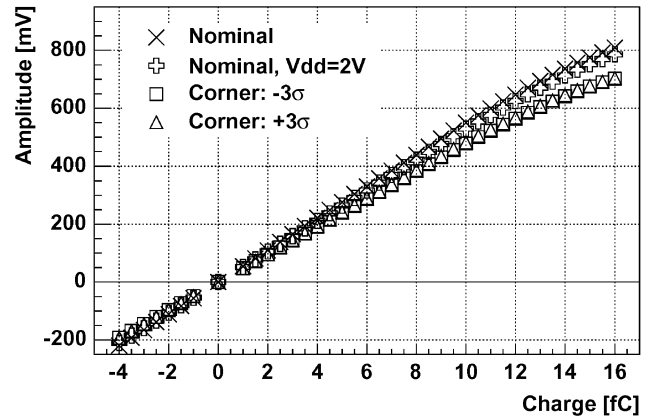

Fig. 9.   Linearity of the FE amplifier for various corners of the process parameters as well as for the nominal and limited power supply.
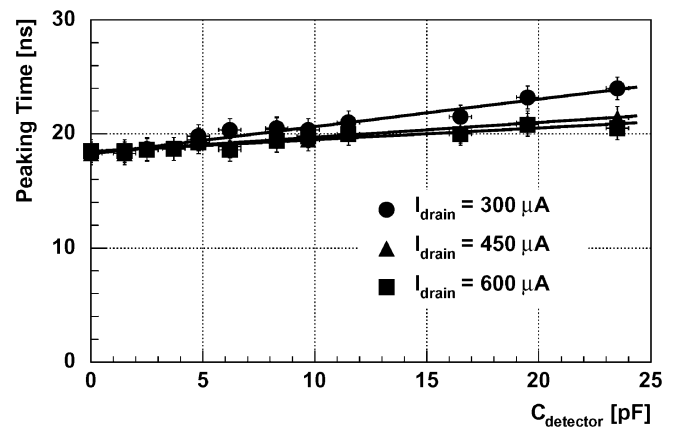

Fig. 10.   Peaking time of the open channel as a function of the input capacitance for different bias of the input transistor and 800 nA feedback current.
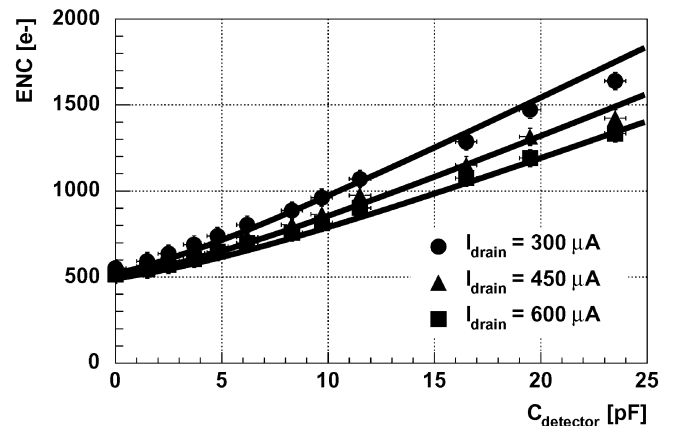

Fig. 11.   ENC as a function of the input capacitance measured for different bias currents in the input transistor (points) and calculated noise using the noise model based on EKV parameters (lines). The feedback bias current was set to 800 nA.

The distribution of the channel gain in one typical ABCDC1 chip is shown in Fig. 12. The gain was extracted from the threshold scans done for 1, 2, 3, and 4 fC input charge, in the linear region of the amplifier. The mean value of the gain is 60 mV/fC and the rms spread is well below 1%.

The distribution of the comparator offset is shown in Fig. 13. The rms value of the offset spread is around 3 mV for all chip
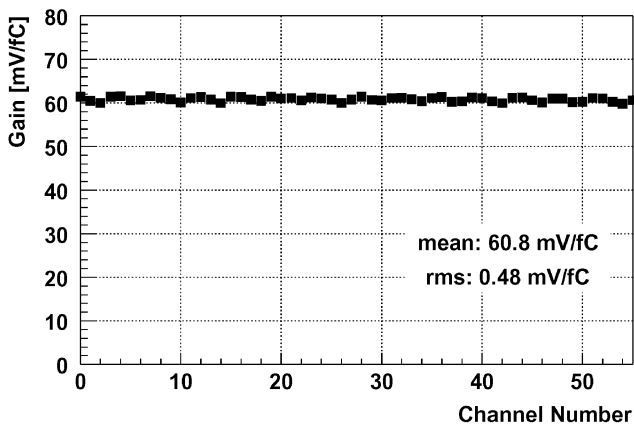
Fig. 12. Distribution of the channel gain across the ABCDC1 chip biased with nominal currents.
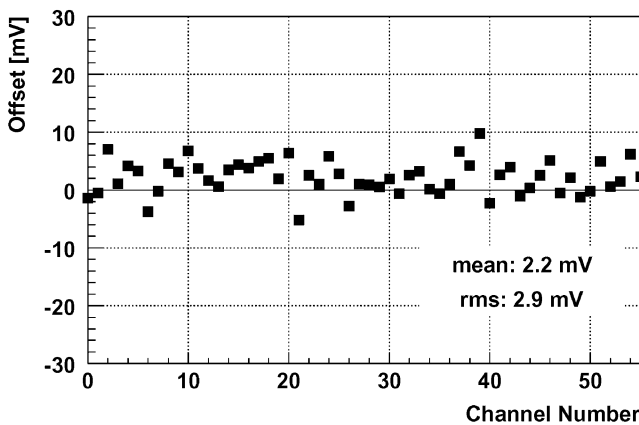

Fig. 13. Distribution of the comparator offset across the ABCDC1 chip for nominal bias conditions.
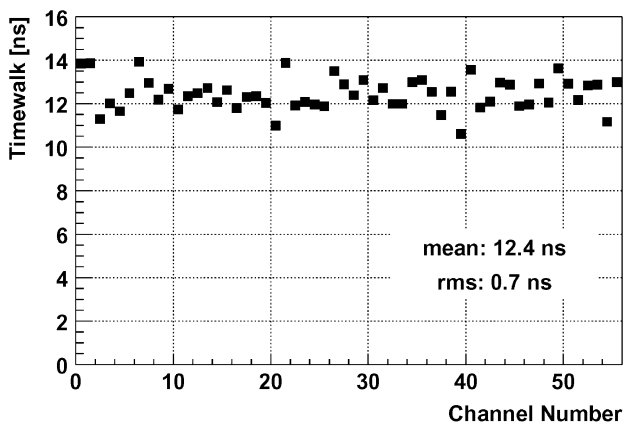

Fig. 14. Distribution of the time walk across the ABCDC1 chip working with nominal bias conditions.

samples measured, which is about 5% of the response to 1 fC charge. Fig. 14 shows the distribution of time walk in one typical ABCDC1 chip. A common threshold voltage equivalent to 1 fC charge was applied to all channels; thus, we may expect an ad-

ditional variation of the measured time walk due to the variation of the effective threshold from channel to channel. The average value of 12.5 ns agrees well with the simulation.

V. CONCLUSION

The developed ABCDC1 ASIC meets all of the requirements and demonstrates that the binary front-end for silicon strips detectors as used in the ATLAS Semiconductor Tracker can be built in a 0.25 μm CMOS process. For a detector capacitance of 20 pF noise below 1500 e$^-$ ENC has been achieved for 300 μA bias current in the input transistor, which is comparable with the levels achieved in the ABCD front end using a bipolar input transistor. The total supply current of the front end is 600 μA and the power dissipation is 1.5 mW per channel. The peaking time for the nominal bias conditions is about 22 ns. The time walk measured for input charges between 1.2 and 10 fC for the threshold set at 1 fC is 12 ns.

Noise optimization has been performed using a noise model based on the EKV characterization of MOS transistors. The model takes into account the channel thermal noise, the gate-induced current noise and correlation of these two noise sources as well as the flicker noise. The calculated ENC figures agree well with the experimental data.

The functionality of the ABCDC1 chip has been tested for a wide range of the bias currents and power supply voltages. The performance of the chips processed with nominal and corner technology parameters is very comparable. Good linearity is maintained up to 12 fC input charge for all possible corner parameters and for the power supply voltage reduced down to 2 V.

A very good uniformity of the gain, with channel-to-channel spread less than 1% rms, has been obtained. The spread of the comparator offsets is below 3 mV rms for all measured samples, which is about 5% of the amplifier response to 1 fC input charge. No noticeable degradation of basic electrical parameters as well as of matching has been observed after X-ray irradiation up to a dose of 10 Mrad.

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