POSTERS

SEVERAL USES OF MC 68000 IN CAMAC SYSTEMS

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ABSTRACT

Camac is the universally used standard in High Energy Physics experiments. In order to give to technicians a debugging and trouble shooting tool and to physicists a cheap system for apparatus test we have developed an Autonomous Camac Branch Driver using the MC 68000, 16 bits, microprocessor. To achieve it we have designed a powerful Camac interface and an interactive software allowing very simple use of this tool. In the same way we have also designed an Auxiliary Crate Controler, with an associated 64 K to 256 K words (16 bits) memory, for data acquisition and preprocessing at the Camac Crate level.

Keeping in mind the same idea we are designing a new Branch Driver with a large memory, devoted to data acquisition and working as a frontal processor, at the Camac Branch level, for the main experiment computer.

The recent appearance of 16 bit microprocessors allows the possibility to give a cheap solution to a lot of problems in Camac acquisition systems in High Energy Physics experiments. In addition to improving triggers by fast on line data processing, the power of a fast 16 bit processor can be used to reduce event acquisition time by paralleling a number of processors or reducing data before transfer in the main computer of the experiment.

One can imagine the placing of such processors in different points of acquisition systems : essentially, in a Branch Driver position, in a Crate Controller position or as a concentrator in an Auxiliary Branch Driver Position.

In 1980 we designed a Camac interface to the Motorola MC 68000 microprocessor which appeared to us to be the most appropriate for this kind of work.

This microprocessor has a very large addressing capability (16 Mbytes, on 23 bits), to separate buses for addresses and data.

The buses work in the asynchronous handshaked data transfer mode. In addition this microprocessor has an internal 32 bit structure and data path. The Camac parallel Branch Highway is also an asynchronous handshaked bus with separate addresses and data lines. A Camac Branch operation is fully described by a 17 bit word (F,C,N,A). So if we consider Camac Addresses FCNA as a part of the 68000 memory space we cut only a small part (1/64) of microprocessor addressing capacity. It becomes possible to interweave a Camac cycle inside the 68000 bus addressing cycles, taking care of a Camac non-response by a time out watch dog to prevent 68000 bus locking.

To perform a Camac function with no data transfer (test or command, F8 = 1) one can execute a "TST FCNA" instruction. The only necessary answers are the state of X and Q bits. If the function produces a false X this is a serious malfunction and an interrupt is per-

formed. The state of the Q line is reflected on data line D15 which sets the "N" indicator in the 68000 Status Register (Q = 1 → Negative operand). This can be immediately used by a conditional branch instruction.

To perform a 16 bit data transfer function we use an instruction like "MOVE FNCA, MEMORY" or "MOVE MEMORY, FNCA". (See timing diagram on Fig. 1). For 24 bit data transfer we simply use a MOVE.L instruction (32 bit instruction) in place of a MOVE instruction (16 bits). This instruction performs two successive memory accesses (Most significant word, Least significant word). With regard to the direction of transfer, given by F16, we must memorize one word or the other in the coupler. On Camac Writing, Most Significant Word is memorized and the Camac cycle occurs on the second memory access. On Camac Reading, the Camac cycle is performed first and Least Significant Word is memorized until the second memory access. Logical diagram (Fig. 2) shows the data path in both cases.

During a data transfer function, X and Q cannot be read at the same time as data. They are latched in a STATUS Register at a specific Camac Address and can be tested by a "TST STATUS" instruction.

Note that the whole process is non-interruptable, because the Camac Cycle is executed inside the MC 68000 instruction cycle. In data transfer mode an interrupt can occur between Camac "MOVE" and "TST STATUS" instructions. Then the interrupting routine must store "STATUS" on stack and restore it at the end of the routine completion.

The Autonomous Branch Driver (baptised "M68Kmac") is designed around the M68KDM design module, sold by Motorola. This card is coupled to the Branch Driver interface card by an EXORCISER type bus (8 bits, 6800 based bus) extended to 16 data lines. For simple use of this bus we adopt a special format for Camac Addresses taking into account the fact that functions using F4 are reserved or non-standard (Fig. 3). Only one level of interrupt is trigged by three possible sources : no X answer, Time Out or Branch Demand. In addition M68Kmac acts as a Branch Terminator. With a 8 MHz processor a Camac Branch Cycle is performed in only 2.75 µsec (16 bits read or write).

M68Kmac can operate two RS232 ports : one for a display terminal and another for a host computer of mass storage connection. A transparent mode is available for cross-software development on the host. A slight modification of the M68KDM card allows the possibility to use up to 64 Kword of RAM and 16 Kword of EPROM.

This autonomous Branch Driver is used in small stand alone systems essentially for tests, debugging and trouble shooting or with Branch Mixers in larger systems.

At the lowest level we can use 68000 based Camac controlers for Auxiliary Crate Controlers or as an Auxiliary Branch Driver.

For both applications we designed a double slot Camac module with one common card for the 68000 processor and a specific second card for each use.

The first card contains the 68000 processor with its clock and auxiliary circuits and sockets for up to 24 Kword of EPROM and 4 to 8 Kword of RAM. There is also two RS232 ports, as on the 68Kmac, for the terminal and the host computer. Programs can be loaded in

the 68000 memory through this port in Motorola "S" format. Interconnection between cards is made by a bus following "VERSABUS E" specification. This allows the possibility to integrate commercial cards in the future.

The Auxiliary Crate Controler card contains all Camac interface and RAM. It is designed to be used with type A2 Crate Controler and to generate Dataway Camac cycles using the Request/Grant procedure described in ESONE 6500e. A typical application of such an Auxiliary Crate Controler is to perform preprocessing or calculation on data read in its own crate and then send results to the main computer. In order to facilitate communication between the main computer and the 68000, RAM is accessible both by the 68000 bus and by the main computer as a standard Camac module in DMA or in single action mode. Thus the main computer can easily fetch results in the 68000 auxiliary Crate Controler memory. It can also directly load programs onto ACC memory and start its execution by sending a F25 function causing a non-maskable interrupt to the 68000. LAMs coming from CCA2 are connected to 68000 interrupt lines through a vector generator. Each LAM can be enabled or masked under 68000 control.

This card can receive up to 128 Kword dynamic RAM. Using a 8MHz processor, and if the Dataway is free at Request time, a Camac cycle can be achieved in less than 2 µsec. A block diagram of the A.C.C. is shown on Fig. 4.

The third part of the system is the Auxiliary Branch Driver Card. As in the ACC it contains RAM which is connected both to the 68000 bus and to the Dataway providing to the main computer the possibility to access it directly via the main Camac Branch. The Branch Driver part is practically the same as in the M68Kmac. The main difference is in LAM processing. In addition to the vector generator used as in the ACC to interrupt the 68000 processor, a mask register, directly set by the main computer, allows the possibility to connect one, or more, auxiliary Branch GL lines to the L line of the dataway. Fig. 5 shows the logical diagram of the Auxiliary Branch Driver. Due to the number of components RAM is limited to 64 Kwords. For the largest applications it will be possible to use a 3 slot Camac module with a 256 Kword RAM card.

As with the M68Kmac the Camac Branch cycle is performed in 2.75 µsec with a 8 MHz processor.

All these applications use EPROM resident monitor MACSBUG supplied by Motorola. Links to a large computer by Camac or via the RS232 host port bring the possibility to develop Software using cross tools. Actually, we use Cross-assembler and cross Pascal compilers. Camac routines described in ESONE SR/01 are implemented and can be called from Pascal programs.

In addition for hardware debugging or for local tests in stand alone mode, we have developed a powerfull interactive software baptised "TESCAM" which is very simple to use. TESCAM is EPROM resident on most systems. It performs Camac functions, arithmetical and logical operations on data and can build 8 histograms of 512 bins each, which can be shown on a 4010 type display terminal. With TESCAM a Camac function is performed in 40 µs in single action mode or in only 6 µs in automatic mode (repeating n times the same function).

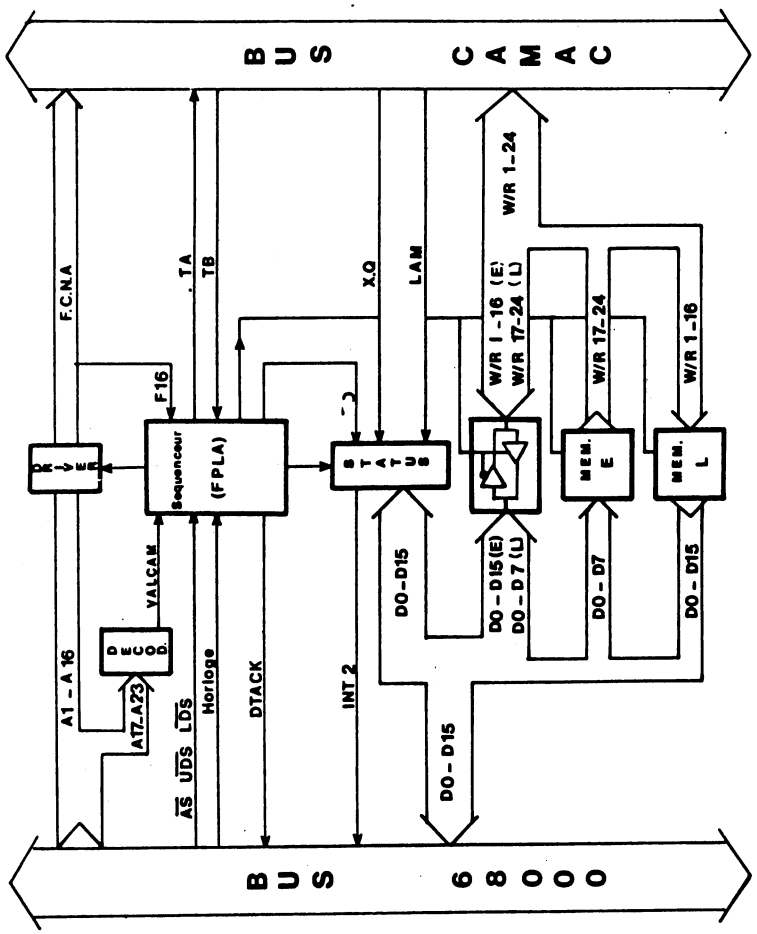
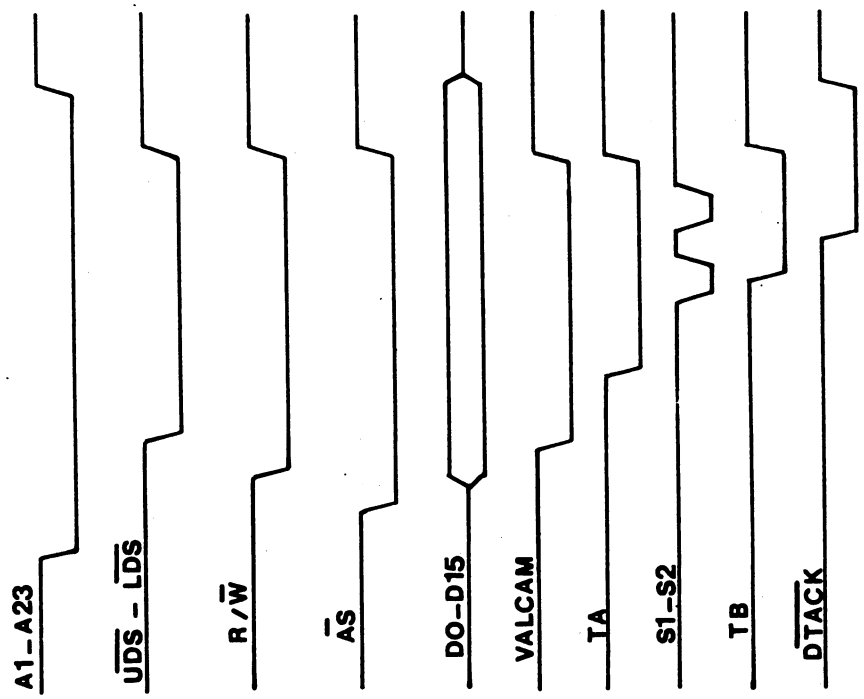
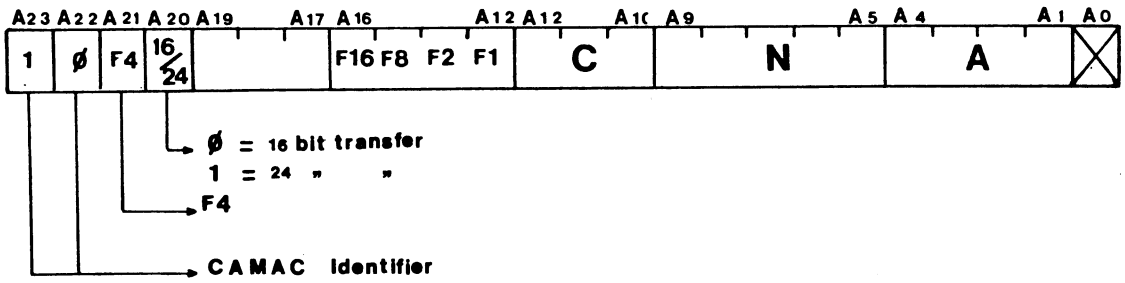


Fig. 2



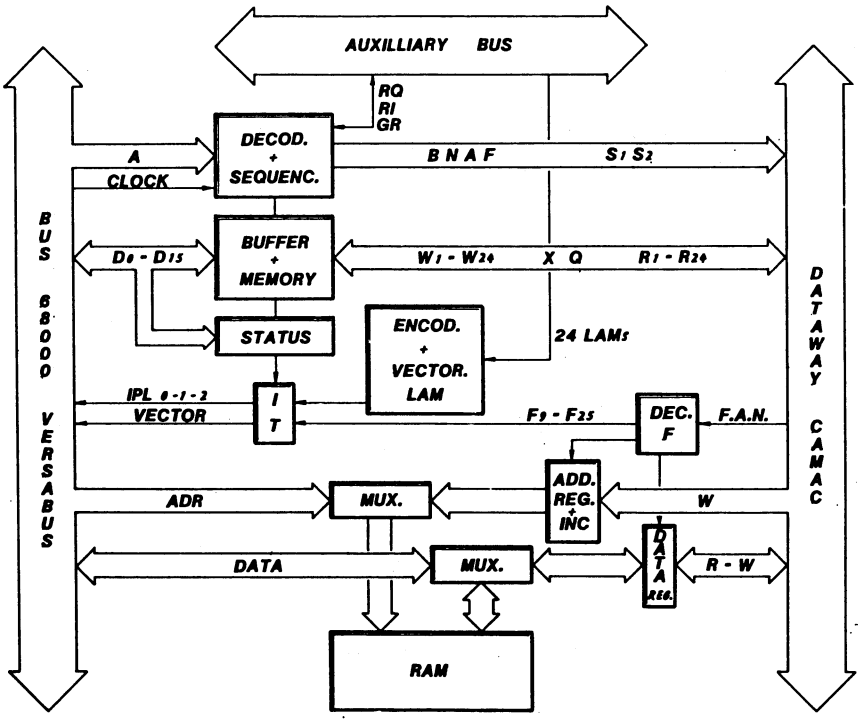
Timing of 16 bit Camac Write cycle

Fig. 1



M68Kmac Addressing Format

Fig. 3



AUXILLIARY CRATE CONTROLER CARD

Fig. 4

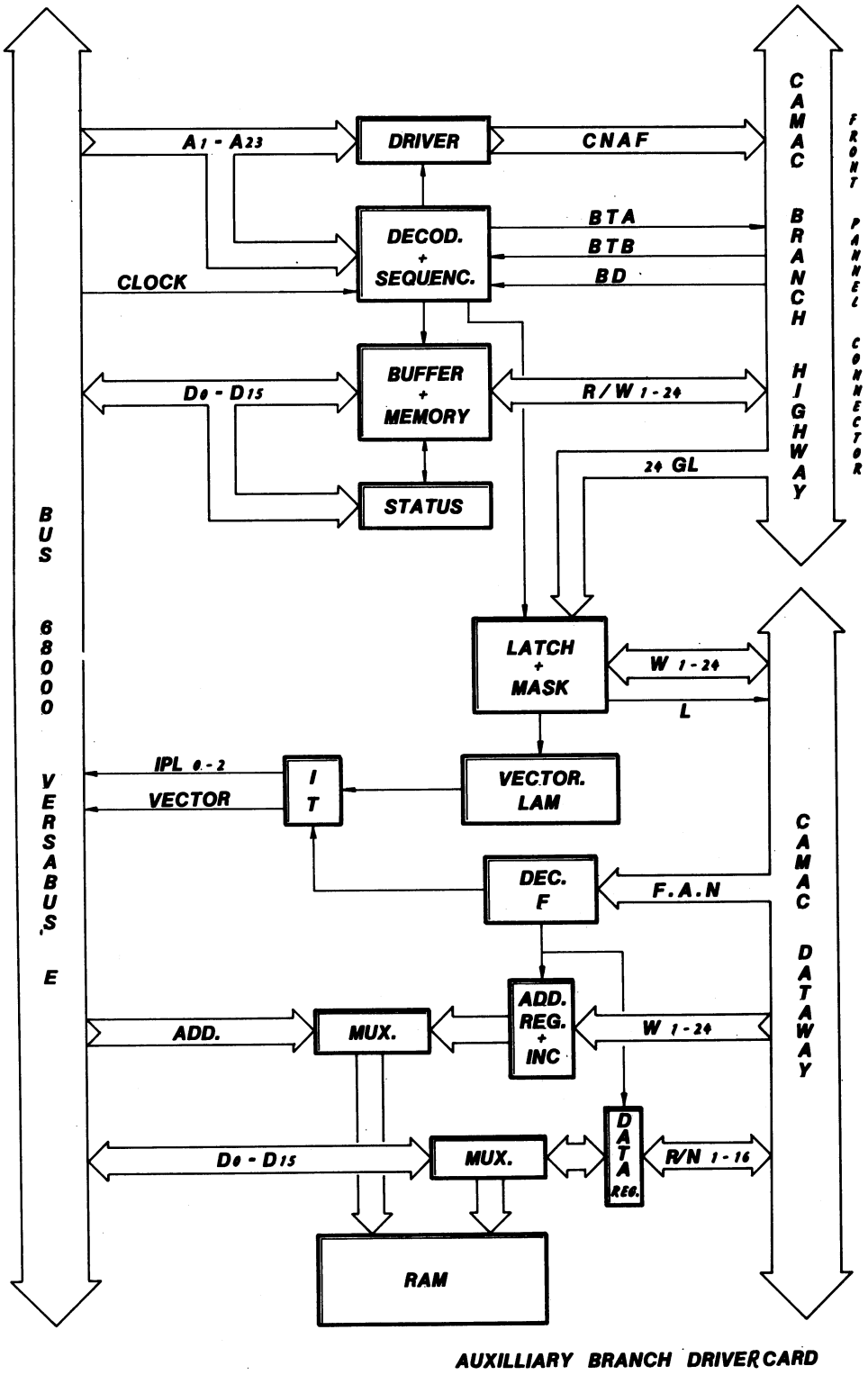

BUS 68000 VERSABUS E
A1 - A23
DRIVER
CNAF
CAMAC BRANCH HIGHWAY
FRONT PANNEL CONNECTOR
DECOD. + SEQUENC.
BTA
BTB
BD
CLOCK
BUFFER + MEMORY
D0 - D15
R/W 1 - 24
24 GL
STATUS
LATCH + MASK
W 1 - 24
L
IPL 0 - 2
VECTOR
I T
VECTOR. LAM
DEC. F
F.A.N
CAMAC DATAWAY
ADD.
MUX.
ADD. REG. + INC
W 1 - 24
D0 - D15
MUX.
DATA REG.
R/N 1 - 16
RAM
AUXILLIARY BRANCH DRIVER CARD

Fig. 5