MICROPROCESSOR EVENT ANALYSIS IN PARALLEL WITH CAMAC DATA ACQUISITION

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ABSTRACT

The Plessey MIPROC-16 microprocessor (16 bits, 250 ns execution time) has been connected to a Camac System (GEC-ELLIOTT System Crate) and shares the Camac access with a Nord-10S computer. Interfaces have been designed and tested for execution of Camac cycles, communication with the Nord-10S computer and DMA-transfer from Camac to the MIPROC-16 memory. The system is used in the JADE data-acquisition-system at PETRA where it receives the data from the detector in parallel with the Nord-10S computer via DMA through the indirect-data-channel mode. The microprocessor performs an on-line analysis of events and the result of various checks is appended to the event. In case of spurious triggers or clear beam gas events, the Nord-10S buffer will be reset and the event omitted from further processing.

One can speed up the data acquisition by introducing a fast dedicated microprocessor into the Camac system. For the JADE experiment at PETRA we are using a MIPROC-16 microprocessor[1] which performs with roughly 8-times the speed of the actual data acquisition computer, a NORD-10S[2]. We built and tested CAMAC interfaces for this fast microprocessor.

The interfaces are designed that either the MIPROC-16 takes the task of reading and structuring all CAMAC data and serves in this way as an additional buffer to a main data acquisition computer or it performs simultaneously with the event readout, controlled by the main computer, a fast pattern recognition to reduce the data rate. All interfaces are placed in a GEC-ELLIOTT Automation System Crate[3] and are independent of any main computer. They allow to perform the following tasks: autonomous control of the CAMAC system, handling of 16 different external interrupts, flexible communication with other command sources (computers) via a mailbox-system and DMA transfer between CAMAC dataway and the microprocessor memory.

We will introduce in the following some relevant features of the microprocessor itself, describe in detail the interfaces to the System Crate and explain the use in the JADE data acquisition system.

The MIPROC-16 is a 16 bit word-length microcomputer operating at an execution cycle time of 250 ns. Its main features are 64 K words directly addressed PROGRAM memory and 64 K words address range DATA memory. 256 word pages are accessible in a single instruction. Other data memory locations can be addressed through two index registers, one of which has an autoincrement mode (fig. 1). The processor has a multilevel, maskable, vectored interrupt hardware. A powerful monitor is available as firmware and is used to load, start and debug programs written in assembler, cross compiled on the Nord 10S. The communication with the monitor is via a serial link either through an extra terminal or directly to the main computer. Peripherals are connected onto the MIPROC-16 unified data bus.

For the execution of CAMAC cycles we designed the MIPROC-CAMAC interface which uses the unique feature of the GEC-ELLIOTT System Crate[3], that several sources of command (computers) can have access to the same CAMAC System via the System controller. A priority

arbitration system insures a proper interlock between these command sources. The MIPROC-CAMAC interface resembles closely the Nord-10 to CAMAC interface designed by CERN[4] and consists of five registers: 16 bit data low, 8 bit data high, 16 bit command low, 16 bit command high and 16 bit control and status (see table 1 for more details). Three different maskable interrupts to the MIPROC are possible, a missing Q/X response, error (CAMAC cycle timeout) and FIN interrupt for a correctly finished CAMAC cycle. The MIPROC can load each register in a single instruction and start the CAMAC cycle. During the execution time of the CAMAC cycle (typically 2-3 μs) the MIPROC has time for several instructions in its running program as e.g. to analyse the previous data or to prepare the next CAMAC call.

A special LAM-GRADER unit allows a mapping of 16 Lam's (G19-G124) gated by an Interrupt Vector Generator (IVG) (ref. 3+4) to 8 different interrupts of the MIPROC-16.

The layout of the MAIL BOX Interface for communication with the main computer is shown in fig. 2. It has two sets of registers. One for messages and control information from the MIPROC to the Nord which is loaded via the MIPROC data bus and read via the CAMAC READ lines, the other is for communication in the opposite direction. The COMMAND register (16 bits) allows to code 5 different interrupts in either direction (fig. 2). Each interrupt can be polled by further branching on the specific content of the command word.

For simple one word messages a MESSAGE register is available whereas for fast data-block transfers a 16 bit x 16 word FIFO is implemented. The CONTROL and STATUS register contains information on FIFO-status, interrupts and serves as a mask to the different interrupts.

The DMA-interface is built for a fast data transfer either from the MIPROC memory to the CAMAC READ lines or from the CAMAC WRITE lines to the MIPROC memory. For the actual data transfer to/from the MIPROC, the processor is halted for only one cycle of 250 ns allowing for several instructions to be executed between CAMAC transfers. A very useful feature is the implemented Indirect Data Channel (IDC) mode. It permits a data transfer from a CAMAC module anywhere in the system to the present master of the System Crate and in parallel to a slave which is the IDC-module (the DMA-interface in our case) acting as a spy on the CAMAC dataway. This allows e.g. the main computer to read data from CAMAC into its own memory while the MIPROC gets the same data (in the same CAMAC cycle) in its memory (see below for an application).

The MIPROC is used in the JADE data acquisition system where it performs an on-line data reduction. The layout of computers and their interconnection is shown in fig. 3. The MIPROC-16 and the Norsk Data Nord 10S both have access to the CAMAC system through the GEC-ELLIOTT System Crate. The System Crate physically occupies two CAMAC crates to accomodate all necessary branch couplers and Miproc interfaces. A pair of simple link modules connects the dataway bus lines of the two crates. The dataway strobe signals S1 and S2 are buffered and regenerated in a "slave controller" in the control station of the expansion crate. The event readout is started and controlled from the Nord 10S computer after an interrupt from the hardware trigger logic. Only during the readout of the JADE drift-chamber the IDC mode is set in the System Crate which causes the data to go simultaneously to the Nord and the Miproc memory. The Miproc starts analysis immediately after receiving

the first data word with a format check and setup of pointers for the subsequent analysis. After the complete readout of the detector the hardware trigger logic is enabled to accept already the next trigger while the MIPROC might still be busy with the analysis of the event. The result of this analysis is finally transferred via the FIFO in the MAILBOX interface with a delay of 5-15 ms depending on the particular event (fig. 4) and appended to the event in the Nord-10 buffer. For events which are clearly identified as background (e.g. with a vertex outside the fiducial volume) the buffer is cleared, otherwise the event is passed over to the Nord 50 for further analysis (fig. 2). A rejection rate of 50 - 70% has been achieved with a z-vertex cut (along the beam direction) using the program described in ref. 5. A refinement of the hardware track finding logic by an other program running in the MIPROC-16 cuts the data rate by additional 20%.

ACKNOWLEDGEMENT

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REFERENCES

[1] MIPROC-16, Plessey Microsystems, Water Lane, Towcester, Northamptonshire NN127JN, England

[2] Nord-10S, Reference Manual, Norsk Data A.S., Lørenveien 57, Postboks 163ØKern Oslo 5, Norway

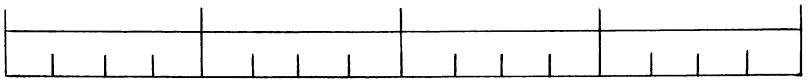
[3] GEC-ELLIOTT Process Automation Limited, System Crate Catalogue now Fisher Control Limited, New Parks Leicester LE3 1UF, England

[4] J.P. Vanuxem, CERN CAMAC Note 60-00 (1976)

[5] J. Olsson et al., Nucl. Instr. Methods 176 (1980) 403

Programmed I/O MIPROC - CAMAC Registers

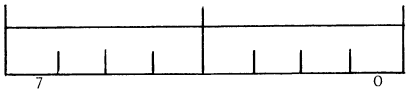
TABLE 1



DATLO

data register low word

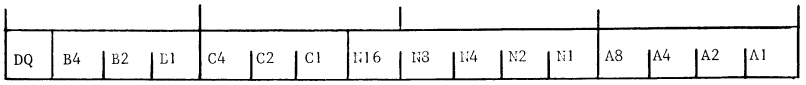
read : INA hex 98
loaded: OTA hex D8



DATHI

data register high byte

read : INA hex 99
loaded: OTA hex D9



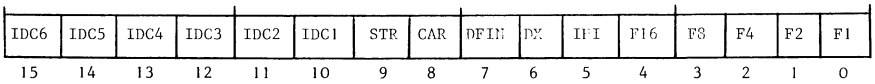
COMLO

command register low word

read : INA hex 9A
loaded: OTA hex DA

bit

0 - 3	A	address
4 - 8	N	station
9 -11	C	crate
12 -14	B	branch
15	DQ	demand Q-response



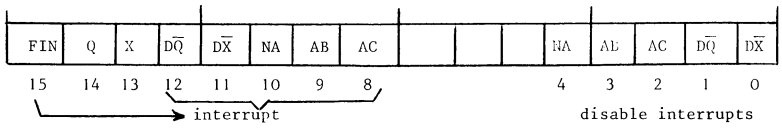
COMHI

command register high word

read : INA hex 9B
loaded: OTA hex DB

bit

0 - 4	F	function
5	IHI	inhibit write data high byte (saves to clear DATHI in 16bit transfers)
6	DX	demand X-response
7	DFIN	demand interrupt if CAMAC-cycle correctly finished
8	CAR	activate crate address register in branch coupler
9	STR	" stock register " " "
10 - 15	IDC	indirect data channel address (0: no indirect addressing)



COST

control - & status register

read : INA hex 9F
loaded: OTA hex DF

bit

0	dis DX̄	disable DX̄-interrupt
1	dis DQ̄	" DQ̄- "
2	dis AC	" AC- "
3	dis AB	" AB- "
4	dis NA	" NA- "
8	AC * +	attempt to access interface during running CAMAC-cycle
9	AB *	CAMAC cycle aborted (timeout: cycle started but no S2)
10	NA *	no access to CAMAC (timeout: cycle requested but not granted)
11	DX̄ *	no X-response although demanded
12	DQ̄ *	" Q- " " "
13	X *	X-response
14	Q *	Q-response
15	FIN *	CAMAC-cycle correctly finished

error-interrupt if not disabled

DQ̄-interrupt if not disabled

FIN-interrupt if demanded

all bits are cleared by init

* cleared by request for a new CAMAC-cycle

+ load registers is inhibited; read is allowed, but results may be unreliable

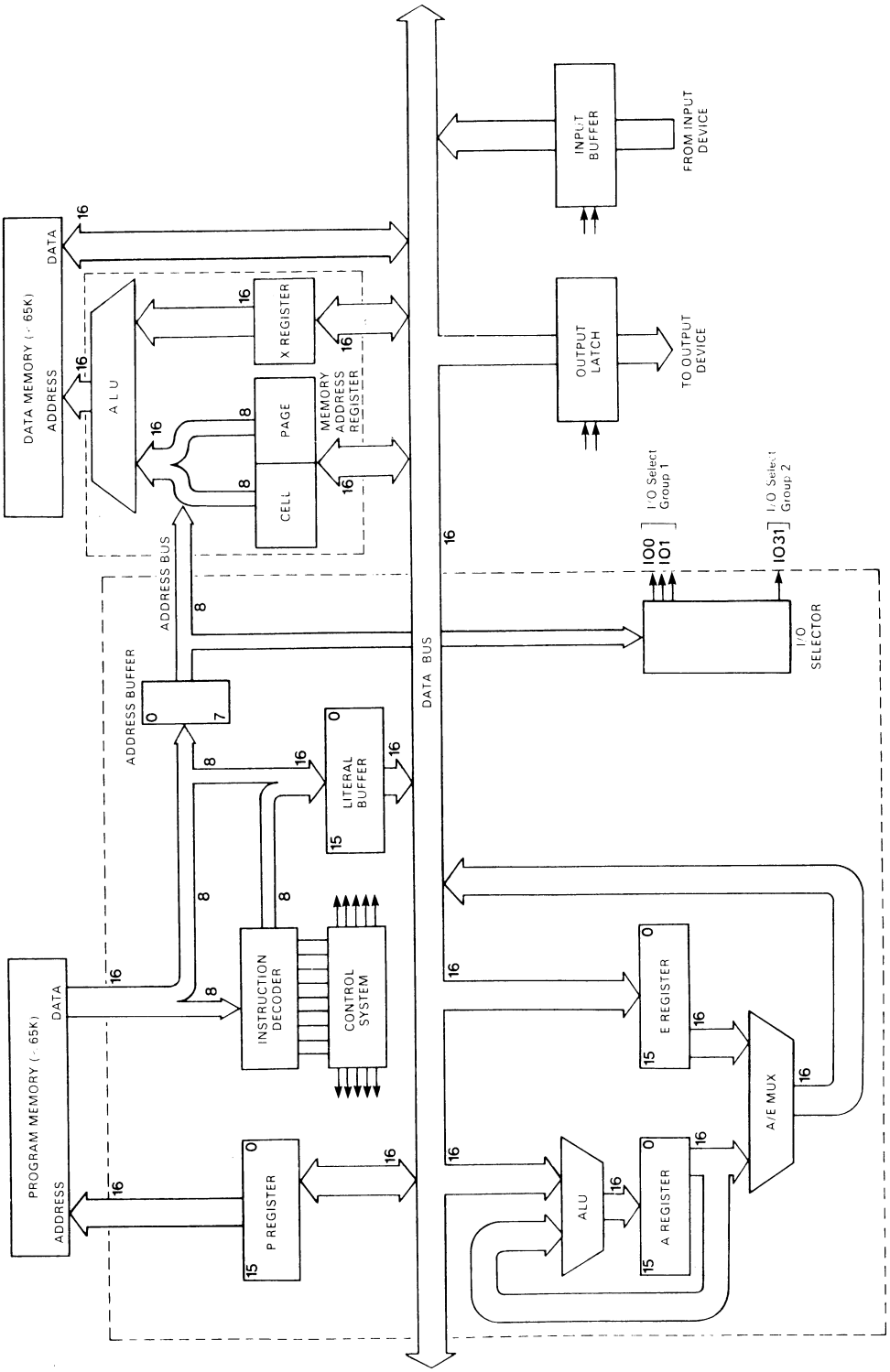


Fig. 1 MIPROC-16 system architecture

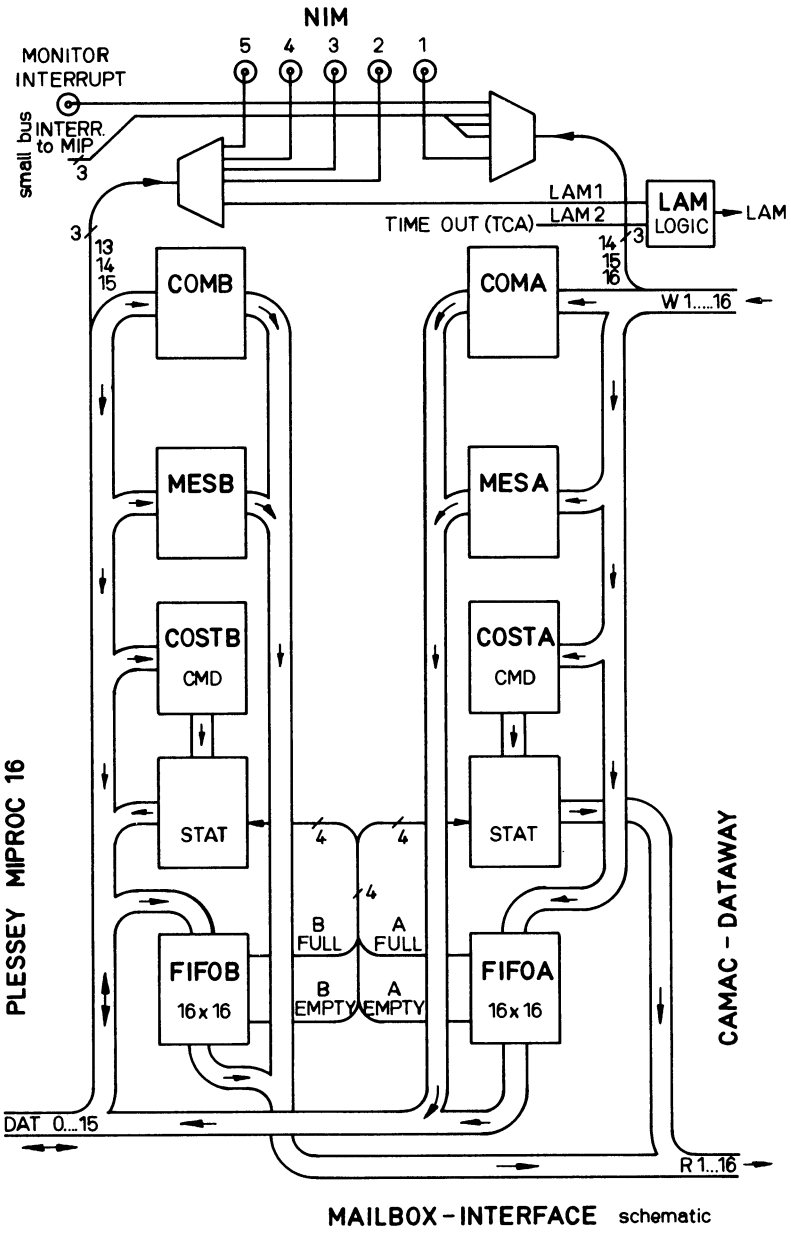


Fig. 2 MAIL BOX Interface schematic

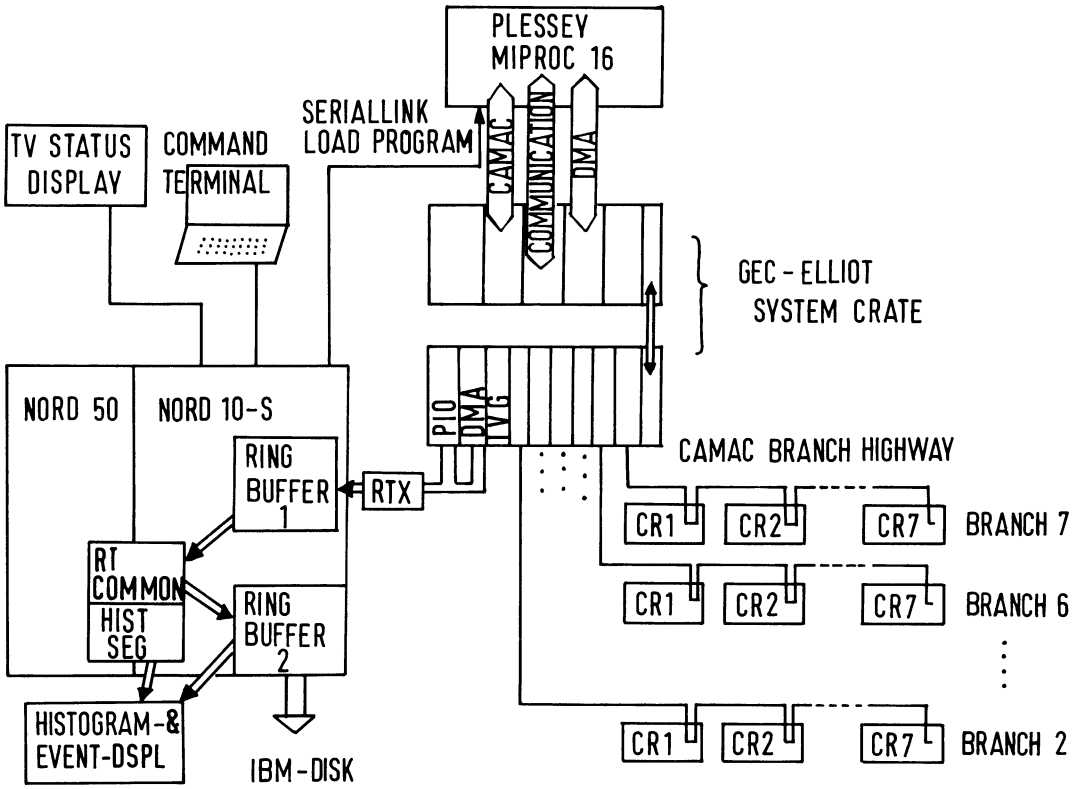


Fig. 3 System layout in the JADE - experiment

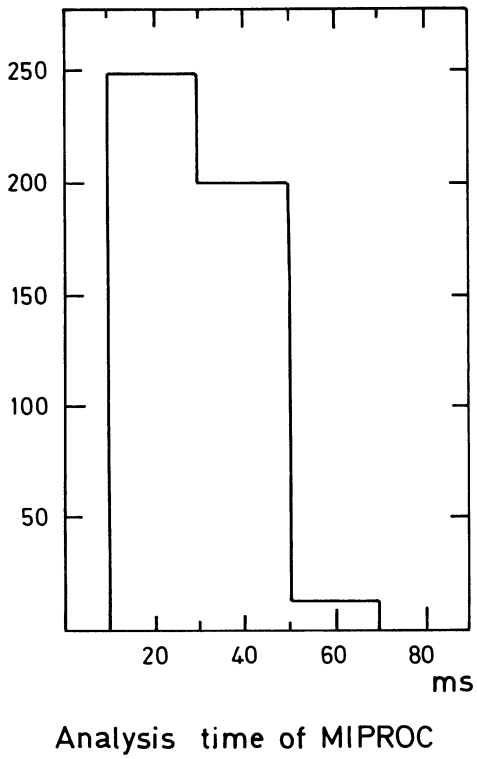


Fig. 4 Time of MIPROC-analysis. The readout starts at t = 0. At t = 10 ms the drift-chamber is being read.