Control System for the LHCb Muon Detector Front-end using SCADA PVSS

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Abstract

This document describes structure and operation, from both hardware and software viewpoints, of the LHCb Muon Control System. It utilizes a CANbus scheme based on two boards named Service Board and Pulse Distribution Module, and a Supervisory Control And Data Acquisition (SCADA) system called PVSS II. Its main task is to control and test the front-end circuitry of the LHCb muon detector.

I. INTRODUCTION

The LHCb Muon System will consist of 7440 front-end boards, capable of processing signals generated by the muon chambers and of reducing the number of physical channels. An effective control system is necessary to supervise, control and test the front-end circuitry functionalities. To accomplish this task a number of electronic boards, communication and control systems, using different protocols and standards (CAN, LVDS I^2C like, TCP/IP), are being developed and implemented. The system architecture and the hardware were entirely designed by INFN Rome1 group and the PVSS based control system in collaboration with CBPF, Brazil.

A. LHCb for the Muon Control System

Large Hadron Collider Beauty Experiment [1] (LHCb) is one of the four experiments of the Large Hadron Collider (LHC) accelerator at CERN, Geneva. It consists of a 20m long single-arm spectrometer which will be used mainly for precision measurements in CP violation and studies of rare decays in B hadrons. Its Muon System [2] is based on Multi-Wire Proportional Chambers (MWPC) and Gas Electron Multipliers (GEM) which will be located in accordance with the diagram shown in Figure 1. It is composed of five muon stations, M1 to M5, and each station is divided into four regions, R1 to R4. The M1 inner part (R1) will be made up of GEMs while the remaining regions will consist of MWPCs. There will be 1380 chambers in the Muon System, for a total in the vicinity of 120000 physical output channels.

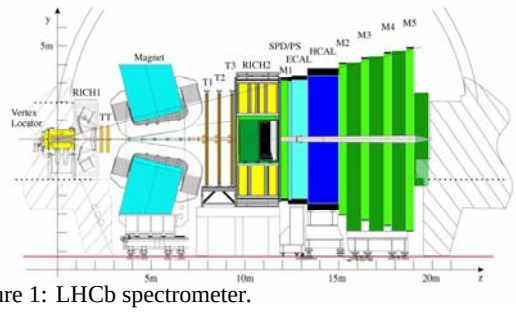

Figure 1: LHCb spectrometer.

B. Read-out Electronics

The LHCb Muon Group developed two ASICs for the read-out system using an IBM 0.25µm CMOS radiation tolerant technology: CARIOCA (Cern And RIO Current Amplifier) and DIALOG (Diagnostic, time Adjustment and LOGics), the last one designed by INFN Cagliari Group. The former is an 8-channel ASD (Amplifier Shaper Discriminator) capable of processing analog signals generated in the muon chambers, transforming them into LVDS (Low Voltage Differential Signaling). The latter ensures generation of logical channels from the ASD output channels, adjustment of ASD threshold levels, physical channels programmable timing and width adjustment as well as availability of testing tools. Some of those tools are: a 24-bit counter for each channel and auto-injection features for CARIOCA and DIALOG ASICs. Two CARIOCAs and one DIALOG will be hosted by a front-end board (FEB), called CARDIAC (CARioca DIAlog Connection).

The CARDIAC external communication is based on a I^2C-like protocol relying on LVDS as physical layer. The control system operates by means of this protocol to manage front-end electronics (FEE) access.

II. MUON CONTROL SYSTEM

The Muon Control System will control and monitor the entirety of FEBs, performing calibration and test routines for every channel. It can be divided into 3 parts, depending on their location (Figure 2). The first environment, the cavern, is located 100 meters underground; for safety reasons access will not be permitted during data acquisition, due to high radiation levels present in proximity of the beam pipe. Consequently, electronics equipment must be radiation hard (inside the detector) or radiation tolerant (in the vicinity of the detector), and must allow remote reset and re-programming of all devices covering single event upset (SEU) recovery and power cycling of selected sections of the Experiment Control System (ECS), thus avoiding data acquisition stoppages to perform on site maintenance. The control terminals will reside in the control room, on the ground level, where operators will be able to supervise the entire system. Terminals should be simple to utilize and their user interface should be intuitive to allow usage by non-specialist personnel. Local stations will be situated in the counting room, on the same level of the cavern; in the same way as in the control room, system control and monitoring will be carried out. In the counting room a C-based alternative tool will be available as well, for debugging purposes and as a fallback option in case of failure of the main control system.

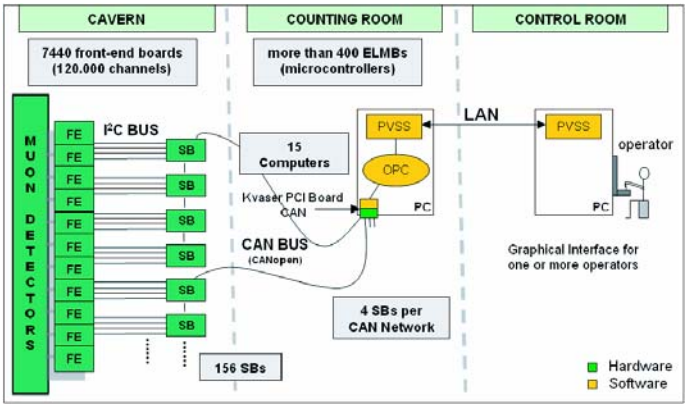

Figure 2: LHCb muon FEE control overview.

FEBs are directly connected to the detectors while FE control boards are connected in equipment crates and racks, in the cavern; both are exposed to radioactivity. For this reason the Muon Group developed the aforementioned radiation hard ASICs and the Rome1 group developed two CANbus based boards using radiation tolerant components. Those boards are the Service Board [3] (SB) and the Pulse Distribution Module (PDM), which will be described in the following. The control circuitry scheme will be based on a certain number of sub-units, using a combination of SBs and PDMs (it will result in a total of roughly 100 boards) and on crates with customized backplane interconnect.

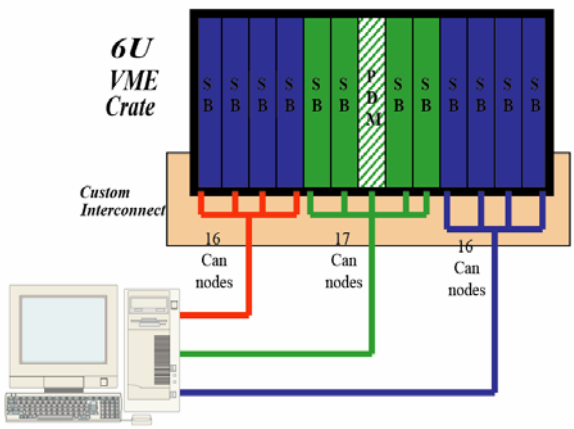

Figure 3: Crate scheme.

CANbus access via PC is made possible by a commercial PCI card manufactured by Kvaser AB (Sweden). Such a board has 4 CAN channels available; each channel can support up to 4 SBs (16 CAN nodes). The control system will make use of approximately 2000 I^2C-like links to access all the FEBs. A SB can handle up to 12 I^2C-like channels, each of those being able to manage up to 8 FEBs and to reach a maximum cable length of 10 meters. Considering that an I^2C channel must not connect more than one chamber and a chamber can use a couple of I^2C channels, the estimated total number of SBs required in the system is of 156.

Each FEB contains 93 registers: as a consequence in total there will be more than 690000 byte wide registers in the LHCb Muon System which will be accessed by the SCADA system. For this reason a server-client model communication system known as OPC [4] (OLE for Process Control) is being used. It provides data-transfer between CAN devices and high-level software. The SCADA system in use (PVSS II) has been chosen by CERN JCOP Group as a general solution for all LHC experiments. It is well adapted to large controlling systems, allowing manipulation of a high number of devices and registers by means of data acquisition, alarm handling, communication protocols, graphic user interfaces, etc.

A. *Service Board*

It consists of 4 Embedded Local Monitor Boards (ELMBs) [5] and a FPGA as well as other circuitry. Usage SRAM based FPGA in radiation environment has been evaluated [6] but a reprogrammable radiation tolerant Actel ProASIC^{PLUS} APA075 FPGA [7] (flash based) was chosen. The FPGA allows generation of strobe signals sent to the front-end auto-injection scheme, provides accurate timing signals to use FE scalers as rate meters and sends reset commands to ELMBs and FEBs. ELMBs can perform remote reset of the front-end digital section if necessary, manage the I^2C and CANopen [8] communication systems, and their firmware can be utilized also for test routines.

Figure 4: Service Board.

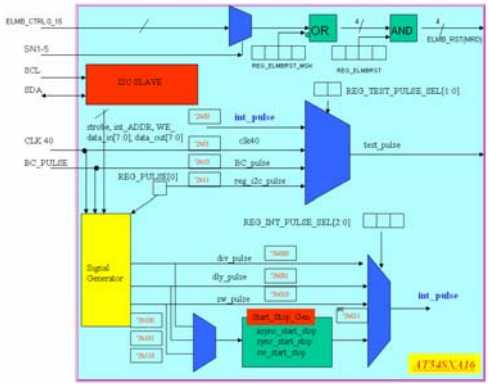

Figure 5: ProASIC^{PLUS} APA075 FPGA block diagram.

1) *ELMB for the LHCb muon system and test routines:*

ELMB is a general-purpose magnetic field and radiation tolerant plug-in board, developed by the ATLAS Control System Group, based on a microcontroller manufactured by ATMEL (ATmega128) and a CAN microcontroller SAE81C91 by INFINEON. An initial version of this board was built to control analog-to-digital converters by means of microcontroller firmware programming. To make it suitable

to the LHCb Muon System, its firmware has been modified as to provide access to FEB and SB FPGA registers via an I^2C-like protocol. Some heavier test, monitoring and calibration routines are also being implemented in firmware to speed up operation.

The main test routines implemented in the AtMega128 firmware are: check whether ELMB and FE boards are present, testing of all the FEB channels in parallel by using the CARIOCA auto-injection system, and channel-by-channel front-end calibration.

To check if FEBs are present a CANbus PDO (Process Data Object) Request, which can work also periodically, is implemented. Such a routine writes and reads different values into a specific FEB register; by checking its content, an ELMB sends a single PDO message containing the information about the presence of all FEBs connected to that chosen ELMB, with location information (I^2C channel and FEB number). In order to check if a certain ELMB is present, a node-guarding mechanism is in operation. PVSS manages those tests and allows visualization of the electronics set-up via user friendly panels (Figure 6).

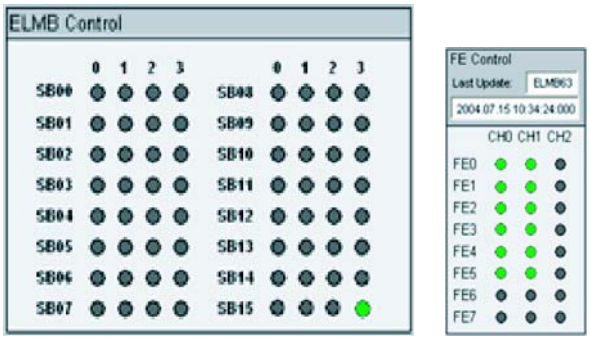

Figure 6: FEB and ELMB presence monitor shown by 'LED' colour in PVSS panels.

To test front-end operation channel-by-channel the CARIOCA auto-injection functionality is used to generate a fixed number of pulses; some scalers within the DIALOG are employed to verify the response of a chosen CARDIAC channels group. With a single SDO (Service Data Object) message it is possible to know if, on a given FEB, all channels are responding correctly or not.

A channel-by-channel calibration is required because of the CARIOCA offset non-uniformity. A procedure has been implemented in order to measure the offset of each LHCb muon FE channel and to create a database (by using PVSS), allowing a fine adjustment of the resulting threshold values (each FE channel has an independent related register). Its first implementation has been a C program and it is now being adapted to be part of the ELMB firmware. It finds the offset by means of threshold scan versus noise rate measurements; the offset values are then sent to the PVSS where they will be used to correct the offset non-uniformity. The threshold value with maximum noise rate is supposed to be the appropriate channel offset value. Graphs in Figure 7 were plotted with real data measured using CARDIAC boards, a MWPC and the GIF facilities at CERN.

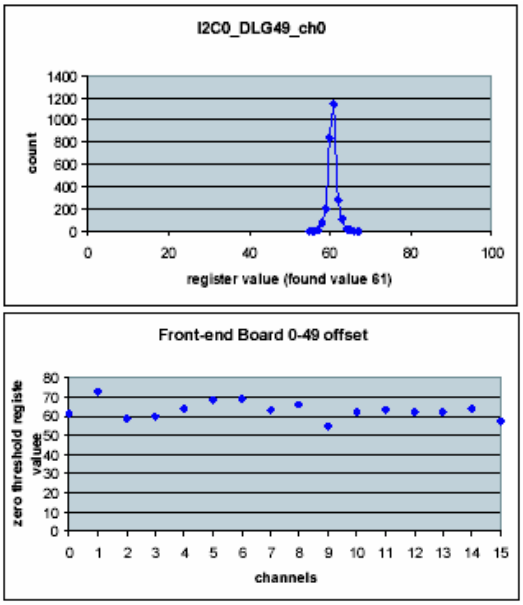

Figure 7: Plots relative to CARDIAC calibration procedure.

The top graph shows noise rate behavior when scanning threshold values; the bottom graph shows offset values found in the 16 channels of a specific CARDIAC board.

B. Pulse Distribution Module

The Pulse Distribution Module (PDM) has an ELMB, a TTCrq module [9] and an Actel ProASIC^{PLUS} APA075 FPGA as building blocks. Its main functionalities include distribution of the 4 CANbus channels from a Kvaser board to SBs through the crate backplane. A PDM also ensures recovery, re-phasing and distribution of the machine 40 MHz clock to all SBs using lvdsBUS standard signals. Finally, PDM can produce pulses derived from the TTCrq bunch crossing (BC) counter.

LvdsBUS timing signals are necessary for synchronous operation of logic contained in the SB FPGA. They are also used by DIALOG chips for calibration of their internal delays. Pulses obtained from the TTCrq BC signal are also used to test front-end electronics, through their pulse injection feature.

TTCrq modules receive the LHC clock signal via optical links and by means of an I^2C internal register permit to delay the 40 MHz clock. Delay adjustment of the main clock signal is necessary to synchronize the front-end system. The PDM FPGA also compares the TTCrq BC counter with an internal register to generate synchronization signals at given times. Every PDM can reset a specific SB and in turn any SB can reset a PDM in the same crate. Such a feature should be used in case of issues as communication failures and SEU errors.

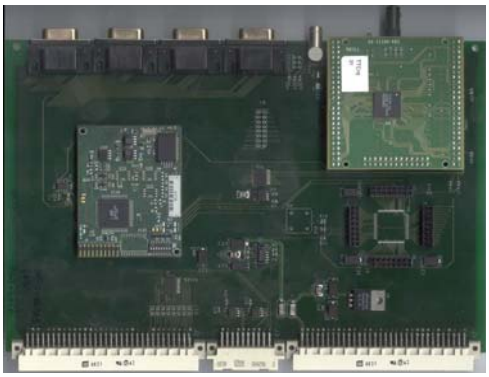

Figure 8: Pulse Distribution Module board.

C. *PVSS and OPC*

PVSS II [10] is the SCADA system chosen by CERN to supervise and control all LHC experiments. It is specially suited to assemble a distributed control system. Its main features are: compatibility with several communication protocols, alarm handling and database facilities.

OPC (OLE for Process Control) is based on a server-client communication scheme and it has been developed for several years by a foundation established by 150 companies specialized in the industrial control and automation field. The OPC server used by the LHCb Muon Control System [11] works as a transparent layer between PVSS and CAN devices (ELMBs). It allows management of CANopen features [8] as heartbeat/node-guarding, SDO, PDO and NMT messages.

The Muon Control System will need to handle all front-end channels using the DIALOG ASIC features. The PVSS system should access more than 690000 registers and their control devices for supervision, testing and calibration purposes. Data manipulation is carried out by means of PVSS data-point objects which represent individual system registers. Each entry requires implementation of a unique OPC item and PVSS data-point. A specific procedure has been developed in order to generate automatically every OPC item and data-point. Such a method performs, at experiment initialization time, detection of the ELMBs and FEBs connected to the system and creation of all the structures needed to manage them via PVSS.

The current control system makes possible to read and write all FE registers using PVSS (Figure 10). Each FE channel has its own threshold, scaler, mask, pattern and timing (delay and shaper) registers. PVSS is able to set all of them automatically when necessary and to monitor ELMBs and FEBs operation (Figure 9).

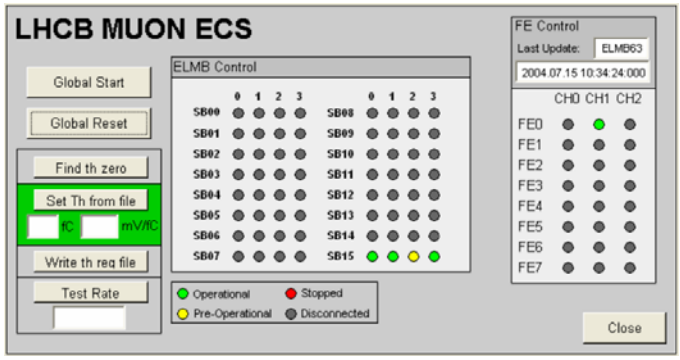

Figure 9: PVSS FE Control System main panel.

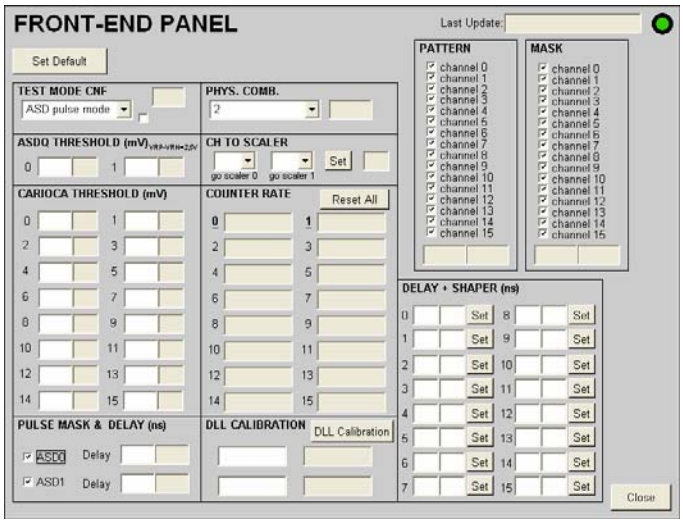

Figure 10: PVSS Front-end panel.

Features developed to control the FEE are summarized below:

- Automatic on site front-end calibration
- Front-end board presence monitoring
- Test of all FE channels using ASD chip auto-injection
- ELMB CANopen state and operation control
- All channels rate monitoring
- Masking out noisy and broken channels
- Automatic threshold adjustment in fC or mV for all channels
- Reset of control and front-end electronics
- Use of database with threshold values

III. CONTROL SYSTEM TEST USING GIF FACILITIES AT CERN

A system has already been utilized by the authors to test a MWPC assembled by the INFN LNF Group (Frascati). With such a test set up an evaluation of the current PVSS system and its features has been carried out. The MWPC under test contained 192 physical channels, which were read-out by means of 24 CARIOCAs and 12 DIALOGs.

The control system implementation consisted in a local computer running PVSS and OPC server, equipped with a Kvaser board, connected to a Service Board. Using control procedures calibration and threshold adjustment were performed on each ASD channel; some broken channels were singled out as well.

Threshold values were scanned on site to determine how ASD channels were offset (Figure 11 and Figure 12) and using the same procedure all thresholds values were set to be the same, resulting in an accurate measurement of the CARIOCA offset non uniformity (Figure 12).

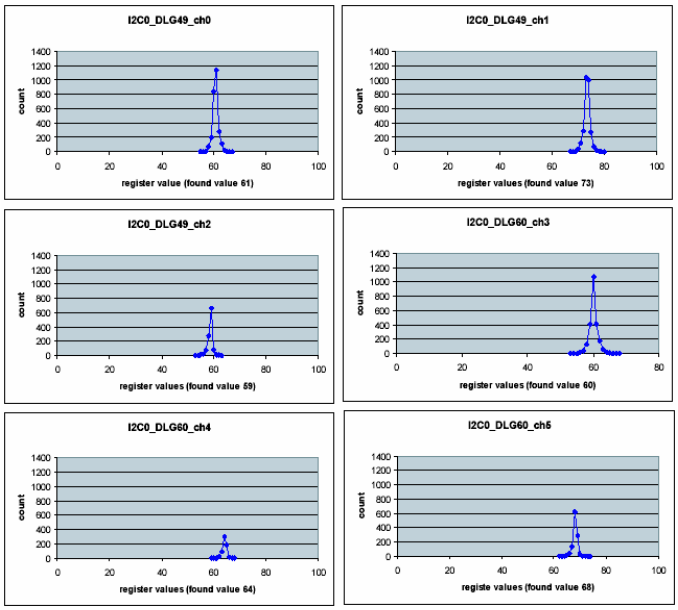

Figure 11: Noise behaviour on threshold scanning.

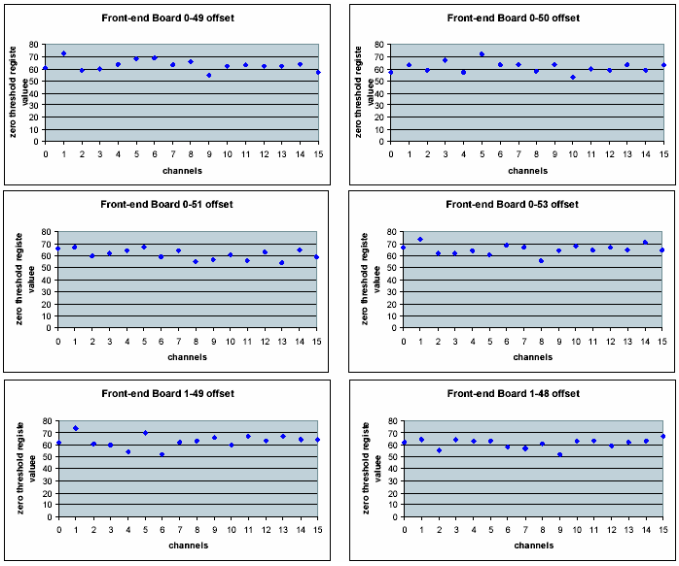

Figure 12: CARDIAC channels offset.

IV. Conclusion

The LHCb Muon FEB control system is currently being developed and implemented, and preliminary tests proved to be successful. A prototype with new ELMB firmware features and PVSS II program has given satisfying results. Development activities will continue focusing on new features implementation and system optimization.

V. Acknowledgments

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VI. References

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