The OTIS TDC Chip for LHCb Outer Tracker Readout

H. Deppe, A. Srowig*, U. Stange, M. Feuerstack-Raible†
U. Trunk, U. Uwer
(Physikalisches Institut der Universität Heidelberg, Philosophenweg 12, D-69120 Heidelberg, Germany)
deppe@kip.uni-heidelberg.de

I. The OTIS TDC Chip

OTIS[1] is a 32 channel TDC[2] chip developed at the University of Heidelberg. It will be used for the readout of the Outer Tracker detector in the LHCb Experiment. It features radiation hard layout techniques and is implemented in commercial CMOS 0.25μm technology. The latest version OTIS 1.2 has been submitted for manufacturing in May 2004. The TDC itself is based on a clock driven architecture and uses a DLL[3] for time reference. Each channel's drift time data is written to a ring buffer to cover the trigger latency, after which the data is either transferred to the derandomiser buffer or overwritten. The buffer management as well as the trigger handling, data formatting and transmission to the subsequent DAQ stages is accomplished by a control circuit. Measurement results for the OTIS 1.1 are presented together with the enhancements leading to OTIS 1.2.

II. LHCb Outer Tracker Front End Electronics

The outer tracker detector of the LHCb experiment consists of $\approx$ 54.000 straw tubes, whose anode wires are read out with the ASDblr chip [1]. Being amplified and discriminated by 4 ASDs, the signals of 32 channels connect to one OTIS chip for drift time measurement. The OTIS ASIC stores the drift times of all 32 channels relative to the 40 MHz LHC clock in an intermediate memory to cover the L0 trigger latency. Upon a trigger, the corresponding data is retrieved from the memory, formatted and transmitted to the next DAQ stage. Operating synchronous to the 40 MHz LHC clock, the 8bit parallel ports of 4 OTIS chips can connect to the 32bit wide input of the subsequent GOL chip [2]. The latter serializes the date and drives it off the detector via a gigabit optical link. The schema of the LHCb outer tracker DAQ in shown in Fig.1.

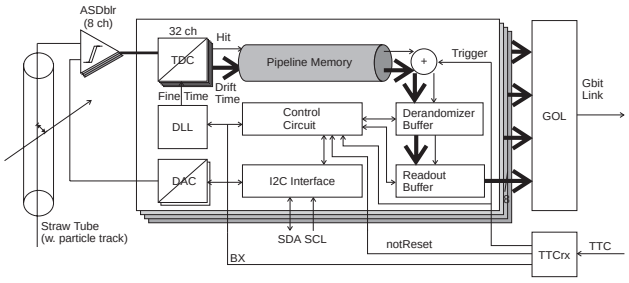

Figure 1: Schematic representation of the frontend electronics in the LHCb outer tracker.

III. Chip Architecture

The OTIS chips consists of four main components shown in Figure 2:

- The TDC core with pre-pipeline register
- The pipeline memory and derandomiser buffer
- The control algorithm
- The slow control circuit and DAC Block

A. The TDC Core

The TDC core, consisting of a 64 stages DLL used as a time reference, the hit register and the decoder circuit, performs the drift time measurement. Therefore the DLL is implemented as a chain of voltage controlled delay elements through which the LHC bunch crossing clock propagates. The phase detector of the DLL then compares the original LHC clock and propagated clock. Depending on the phase between these two clock signals, a charge pump adjusts the delay of the DLL to exactly 1 clock cycle such that the LHC clock and propagated clock are in phase. In this state, called lock state, the reference signals for the drift time measurement can be obtained from the 64 delay elements providing an intrinsic resolution of 390ps. These

*now at Max-Planck Institut für Kernphysik
†now at Fujitsu Mikroelektronik GmbH
[1]Outer Tracker Time Information System
[2]Time to Digital Converter
[3]Delay Locked Loop

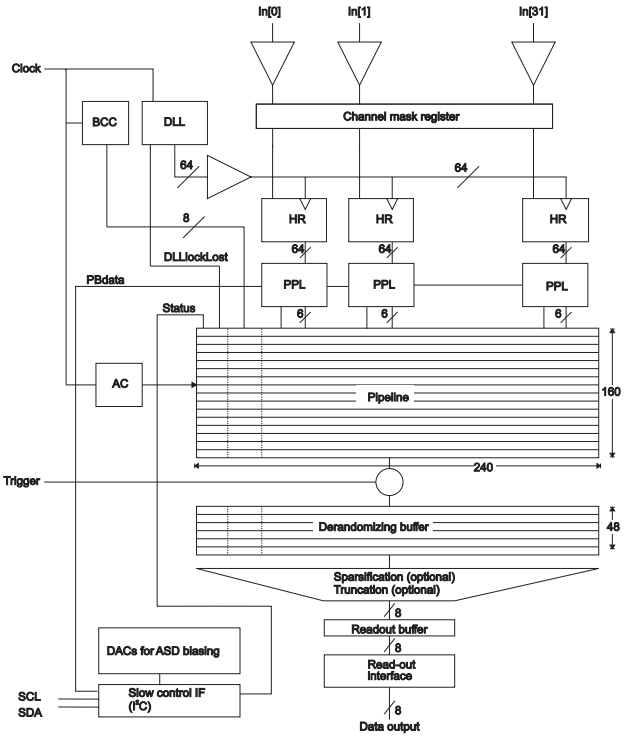

Figure 2: Block schematic showing the OTIS chip's basic building blocks.

reference signals are then used to latch the discriminated detector signals into the corresponding hit registers, thus forming the clock driven architecture of the TDC. The hit register holds an image of the detector signal and the subsequent decoder converts the hit position to a 6bit binary representation. The pre-pipeline register is the interface to the following pipeline memory. In addition to the drift time it stores some status information and is further used to feed the subsequent stages with programmable test data. It also provides the test patterns for the self-test of the pipeline memory.

B. *Pipeline memory and derandomiser buffer*

Pipeline and derandomizing buffer are realized as arrays of dual ported SRAM cells. Their dimensions are 164×240bit and 48×240bit respectively. Synchronous to the bunch crossing clock new data sets, consisting of drift time data from pre-pipeline register, bunch crossing number and status informations are stored into the pipeline. The pipeline is able to hold 164 data sets to cover the 4μs L0 trigger latency. Upon a trigger the corresponding data sets (1, 2 or 3 words) are copied to the derandomizing buffer, which compensates the trigger rate fluctuations. The size of 48×240bit is large enough to hold the data of 16 triggers (á 3 words) which is an LHCb requirement.

Table 2: 8 bit *Extended* drift time encoding of the OTIS 1.1 chip in *Encoded Hitmask* mode.

First Hit Position	Data
1^{st} BX	00xxxxxxxx
2^{nd} BX	01xxxxxxxx
3^{rd} BX	10xxxxxxxx
No Hit	11xxxxxxxx

C. *The control algorithm*

The control algorithm performs the memory access required for trigger handling and data retrieval for readout. In addition it provides the 50ns and 75ns measurement ranges by combining data from up to 3 consecutive bunch crossings. The transmission of the data frame on the OTIS' 8bit parallel output port is indicated by a *DataValid* signal. Furthermore for the OTIS 1.2 it implements two different formats of the readout data stream, described in the following.

Encoded Hitmask: The 4byte header information (containing e.g. BX- and EV counter, Chip ID and status information) is followed by 32byte representing drift times of the 32 channels. While the lower 6bits are the measured drift time within the clock cycle, the first two bits indicate the bunch crossing of the hit. Obviously only the first hit per trigger and channel is read out, allowing for a 100% occupancy. The fixed 900ns readout time required by LHCb is intrinsic to this mode. The data format for the Encoded Hitmask mode is shown in Table 1 and the extended drift time encoding in Table 2.

Plain Hitmask: In this readout mode the 4 header bytes are followed by 1, 2 or 3 32bit hit masks and a number of 6(8)bit drift times according to the total number of "1"s in the hit masks. In this case the data frame has to be cut after 900ns or filled with "0"s to meet the LHCb specifications. Depending on the number of hit masks, only a limited occupancy per trigger and bunch crossing can be transmitted by using the truncation: 1BX = 87%, 2BX = 37%, 3BX = 20%. The structure of the data frames for the Plain Hitmask mode is shown in the Table 3.

IV. The OTIS 1.1 Chip

The OTIS 1.1 (Fig.3) is the latest full scale prototype chip and is available since February 2004. On a die size of 5.1×7.7mm^2 it implements all key features except the *Plain Hitmask* readout mode.

Table 1: Data format of the OTIS chip in *Encoded Hitmask* mode.

Bit	0 . . . 31	32 . . . 39	. . .	280 . . . 287
Data	Header	Drift time (CH0)	. . .	Drift time (CH31)

Table 3: Data format of the OTIS chip in *Plain Hitmask* mode for 1, 2 and 3 BX (top to bottom) readout.

Bit	0 . . . 31	32 . . . 63	64 . . . 71	. . .	$58 + (8n) \ldots 63 + (8n)$
Data	Header	Hitmask (1 BX)	Drift time [1]	. . .	Drift Time $[n]$
Bit	0 . . . 31	32 . . . 95	96 . . . 103	. . .	$88 + (8n) \ldots 95 + (8n)$
Data	Header	Hitmasks (2 BX)	Drift time [1]	. . .	Drift Time $[n]$
Bit	0 . . . 31	32 . . . 127	128 . . . 138	. . .	$120 + (8n) \ldots 127 + (8n)$
Data	Header	Hitmasks (3 BX)	Drift time [1]	. . .	Drift Time $[n]$

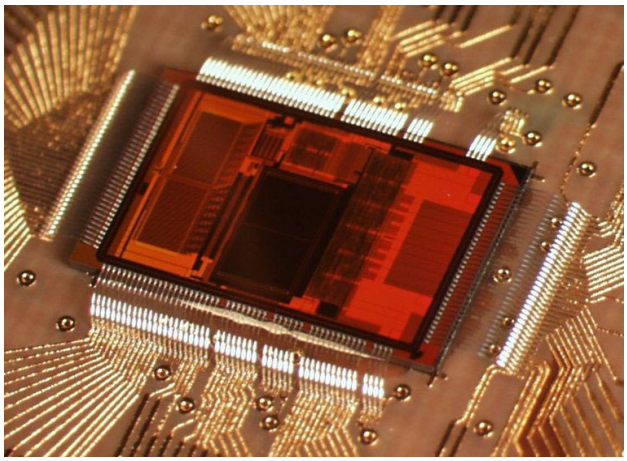

Figure 3: Bonded OTIS 1.1 chip on Test-PCB.

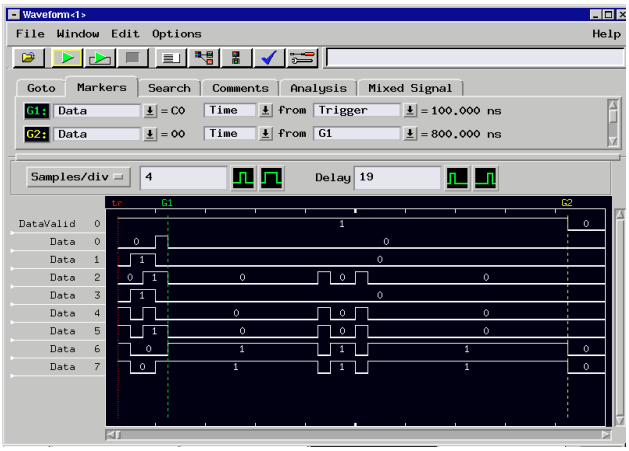

Figure 4: Readout Burst OTIS 1.1 in 3 BX Encoded Hitmask mode. For channel 12 and channel 15 an extended drift time is visible for the 1st BX.

V. Measurements performed on OTIS 1.1

A. *Power Consumption*

After powering the chip, it performs a power up reset. In this state power consumption is 480mW. The power consumption increases to 560mW when operating at the nominal clock frequency of 40MHz (17.5mW/Chan).

B. *Control Algorithm*

The control algorithm performed as expected from simulation. Readout of the data frame takes exactly 900ns, and while working in playback mode, which is also fully functional, the read data is exactly as programmed. Furtermore it was possible to verify the correct encoding of header data and drift times. Also trigger management shows the predicted behavior, e.g. a *FiFoFull* signal after 16 triggers in 3BX mode. All debug signals and internal test features included on the chip, such as the memory self -test, also show the expected behaviour. Furthermore a random trigger test performed at 40MHz clock speed with some 10^7 triggers did not reveal any problems.

Figure 4 shows a Readout Burst for the OTIS 1.1 running in Encoded Hitmask mode. The first 4bytes represents the header with information concerning TDC-ID, Readout mode, Error-Bit, Event- and Bunch Crossing number. The header is followed by the 32 extended drift times.

Figure 5 shows the Readout with an optional comma for nonconsecutive readout which is implemented for synchronization purposes.

C. *Drift Time Measurements*

The measured drift times are expected to follow the detector signals' position within a bunch crossing linearly. The measurements show this expected linear relation between hit position and drift time without missing codes or visible steps..

Figure 6 shows the measured drift times of two chan-

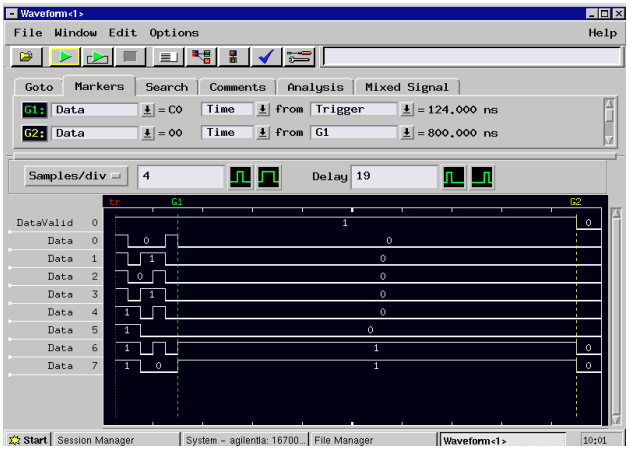

Figure 5: Readout Burst OTIS 1.1 in 3 BX Encoded Hitmask mode. The first byte exhibits the optional comma for nonconsecutive readout. For channel 12 and channel 15 an extended drift time is visible for the 3rd BX.

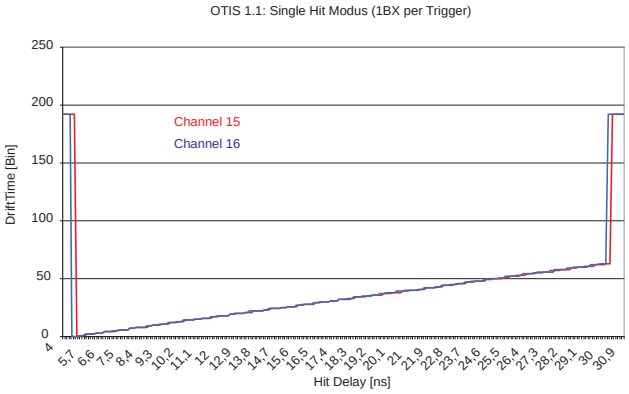

Figure 6: Delay scan (Drift Time vs. Hit Position) of the OTIS 1.1 for 1BX Encoded Hitmask mode.

nels as a function of the *hit*-signal position within the bunch crossing for 1BX Encoded Hitmask mode. For Figure 7 the OTIS 1.1 TDC is programmed to 3BX Encoded Hitmask mode.

VI. Conclusions

The OTIS 1.1 TDC already fulfills the LHCb basic requirements regarding timing and control signals e.g. the *DataValid* signal for the subsequent GOL serializer and an optional comma for the synchronization. The OTIS 1.2 will return at the end of September and finally comprises the additional 2nd readout mode for Plain Hitmasks as well as a reliable bunch crossing counter. Concurrently some minor improvements for the TDC core are done. The OTIS 1.2 features all planned readout modes and modifications to fit seamlessly into the LHCb outer tracker readout chain. In turn it is intended for production to equip the detector. Status reports and further test results will be available at [3].

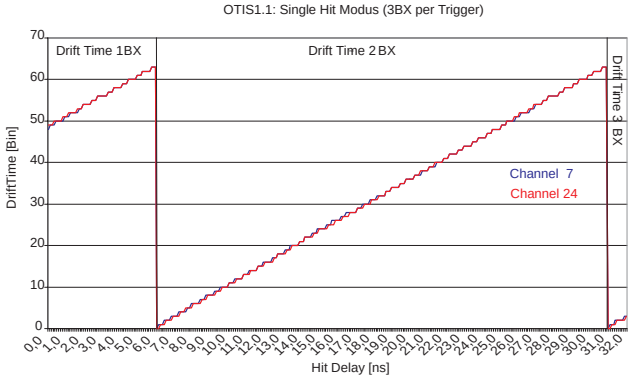

Figure 7: Delay scan (Drift Time vs. Hit Position) of the OTIS 1.1 for 3BX Encoded Hitmask mode.

VI. References

[1] ATLAS use of ASDblr:
`http://www.quark.lu.se/atlas/electronics/trt/chip_asdblr.html`
Measurements for LHCb:
`http://www.nikhef.nl/user/toms/lhcb/otfe/afe/deadtime/index.html`

[2] A 1.25 Gbit/s Serializer for LHC Data and Trigger Optical Links, P. Moreira et al., Proceedings of the 5th workshop on electronics for LHC experiments, September 20-24, 2000, CERN-LHC-2000/041

[3] `http://wwwasic.kip.uni-heidelberg.de/lhcbot/`