Radiation-hard ASICs for Optical Data Transmission in the ATLAS Pixel Detector

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Abstract

We have developed two radiation-hard ASICs for optical data transmission in the ATLAS pixel detector: the VDC, a driver chip for a Vertical Cavity Surface Emitting Laser (VCSEL) diode for 80 Mbit/s data transmission from the detector, and the DORIC, a Bi-Phase Mark decoder chip to recover the control data and 40 MHz clock received optically by a PIN diode. We have successfully implemented both ASICs in 0.25 μm CMOS technology using enclosed layout transistors and guard rings for increased radiation hardness. We present results from prototype circuits and from irradiation studies with 24 GeV protons up to ~60 Mrad (~2.0 x 10^{15} p/cm^2).

I. INTRODUCTION

The ATLAS pixel detector [1] consists of two barrel layers and two forward and backward disks which provide at least two space point measurements. It is the charged particle tracking detector nearest to the interaction region and as such must be able to function in a harsh radiation environment. The electronics used to readout and control the pixel detector therefore must be radiation hard. In this report we describe the progress in developing two radiation hard chips, the VCSEL Driver Chip (VDC) and the Digital Opto-Receiver Integrated Circuit (DORIC) chip as well as the tests used to measure their radiation hardness. First, we briefly describe the flow of data in the pixel detector (Fig. 1).

The pixel sensors are read out by front-end electronics controlled by the Module Control Chip (MCC). The output of the MCC is a low voltage differential signal (LVDS). This LVDS signal is converted by the VDC into a single-ended signal appropriate to drive a Vertical Cavity Surface Emitting Laser (VCSEL). The optical signal from the VCSEL is transmitted off detector to the Readout Device (ROD) via a fiber. The ROD transmits a 40 MHz beam crossing clock, bi-phase mark (BPM) encoded with the data (command) signal to control the pixel detector, via a fiber to a PIN diode. The BPM encoded signal is decoded by the DORIC. The clock and data signals recovered by the DORIC are in LVDS form for interfacing with the MCC chip.

In its entirety the ATLAS pixel optical readout system contains 448 VDC and 360 DORIC chips with each chip having four channels. The chips will be mounted on 180
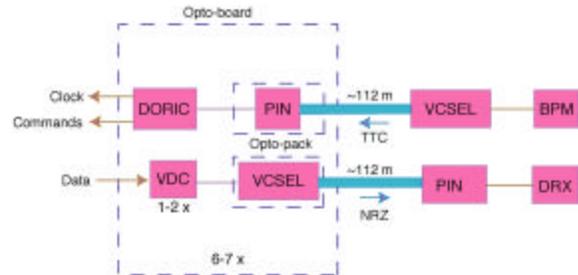

Figure 1: Schematic of the data flow for the pixel detector.

carrier boards (opto-boards). The optical link circuitry will be exposed to a maximum total fluence of 10^{15} 1-MeV n_{eq}/cm^2 during ten years of operation at the LHC. In this paper we describe the development of the radiation-hard VDC and DORIC circuits for use in the ATLAS pixel detector's optical link.

II. THE VDC CIRCUIT

The VDC is used to convert an LVDS input signal into a single-ended signal appropriate to drive a VCSEL in a common cathode array. The output current of the VDC is to be variable between 0 and 20 mA through an external control current, with a standing current (dim current) of ~1 mA to improve the switching speed of the VCSEL. The rise and fall times of the VCSEL driver current are required to be less than 1 ns and the duty cycle of the VDC output signal should be (50 ± 4)%. In order to minimize the power supply noise on the opto-board, the VDC should also have constant current consumption independent of whether the VCSEL is in the bright (on) or dim (off) state.

Figure 2 shows a block diagram of the VDC circuit. An LVDS receiver converts the differential input into a single-ended signal. The differential driver controls the current flow from the positive power supply into the anode of the VCSEL. The VDC circuit is therefore compatible with a common cathode VCSEL array. An externally controlled current, I_{set}, determines the amplitude of the VCSEL current (bright minus dim current), while an externally controlled voltage, tunepad, determines the dim current. The differential driver contains a dummy driver circuit that in the VCSEL dim state draws an identical amount of current from the positive power supply as is flowing through the VCSEL in the bright state. This enables the VDC to have constant current consumption.
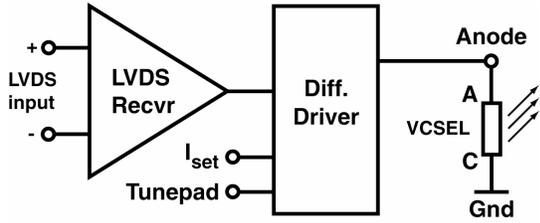
Figure 2: Block diagram of the VDC circuit.

III. THE DORIC CIRCUIT

The DORIC decodes the BPM encoded clock and data signals received by a PIN diode. Figure 3 shows an example of a BPM encoded signal. It is derived from the 40 MHz beam crossing clock by sending only transitions corresponding to clock leading edges. In the absence of data bits (logic level 1), this results simply in a 20 MHz clock. Any data bit in the data (command) stream is encoded as an extra transition at the clock trailing edge.

The amplitude of the current from the PIN diode is expected to be in the range of 40 to 1000 µA. The 40 MHz clock recovered by the DORIC is required to have a duty cycle of $(50 \pm 4)\%$ with a total timing error of less than 1 ns. The bit error rate of the DORIC circuit is required to be less than 10^{-11} at end of life.

Figure 4 shows a block diagram of the DORIC circuit. In order to keep the PIN bias voltage (up to 10 V) off the DORIC chip, we employ a single-ended preamp circuit to amplify the current produced by the PIN diode. Since single-ended preamp circuits are sensitive to power supply noise, we utilize two identical preamp channels: a signal channel and a noise cancellation channel. The signal channel receives and amplifies the input signal from the anode of the PIN diode, plus any noise picked up by the circuit. The noise cancellation channel amplifies noise similar to that picked up by the signal channel. This noise is then subtracted from the signal channel in the differential gain stage. To optimise the noise subtraction, the input load of the noise cancellation channel should be matched to the input load of the signal channel (PIN capacitance) via a dummy capacitance.
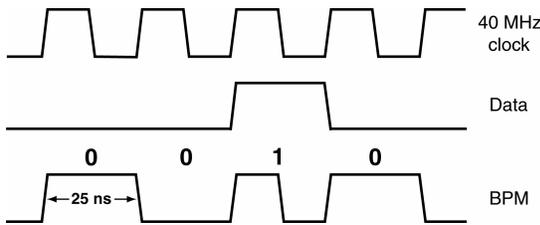

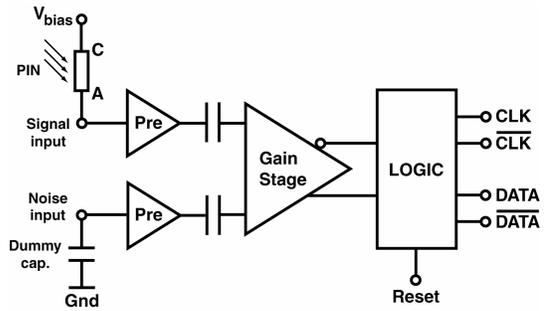Figure 3: Example of a Bi-Phase Mark (BPM) encoded signal.

Figure 4: Block diagram of the DORIC circuit.

To ensure that the DORIC logic locks onto the correct clock frequency it needs to be trained over a certain time period. The specifications currently allow for a 1 ms initialization period, during which a 20 MHz clock is sent to the DORIC chip. The 40 MHz recovered clock is the input to a delay locked loop that adjusts the internal delays until a 50% duty cycle is reached. After having locked into the correct duty cycle, the clock recovery circuit is blind to any extra transitions near the middle of the 25 ns intervals, and will continue to decode the clock correctly even in the presence of data bits.

The data recovery circuit uses each input transition to latch the state of the recovered clock just prior to the current transition into a flip-flop (Figure 5). For no data sent, the recovered clock is always in a low state prior to each input transition. When a data bit is present however, the recovered clock is in a high state just prior to the input transition. The thus decoded data bit is then stretched to make it more stable during full clock cycle (see dotted and solid data bit in Fig. 5).
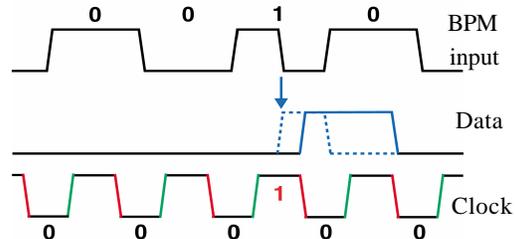

Figure 5: Data and clock recovery procedure of the DORIC.

IV. VDC AND DORIC DESIGN HISTORY

The pixel detector design of the VDC and DORIC takes advantage of the development work for similar circuits [2] used by the outer detector, the SemiConductor Tracker (SCT). Both SCT chips attain radiation-tolerance by using bipolar integrated circuits (AMS 0.8 µm BICMOS) and running with large currents in the transistors at 4 V nominal supply voltage. These chips are therefore not applicable for the higher radiation dosage and lower power budget requirements of the pixel detector.

We originally implemented the VDC and DORIC circuits in radiation-hard DMILL 0.8 µm technology with a nominal supply voltage of 3.2 V. We developed circuits in this technology that met the project's electrical specifications. However, an irradiation study of the DMILL circuits in April 2001 with 24 GeV protons at CERN showed severe degradation of circuit performance. We concluded that the DMILL technology did not meet the radiation hardness requirement of the ATLAS pixel detector.

We have therefore migrated the VDC and DORIC designs to standard deep submicron (0.25 µm) CMOS technology which has a nominal supply voltage of 2.5 V. Employing enclosed layout transistors and guard rings [3], this technology promises to be very radiation hard. Five deep submicron prototype runs of the VDC and DORIC circuits have been received between the summers of 2001 and 2003. Below we summarize the results achieved from the latest (I5e) of our submissions.

V. RESULTS FROM IBM 0.25 µM SUBMISSIONS

To date we have produced VDC and DORIC chips from submissions to IBM's 0.25 µm process. Our last submission used a 5-metal layout while previous submissions have used three metal layers. Both the VDC and DORIC are packaged four channels per chip. Below we briefly describe results from this latest submission. Details and results from previous submissions can be found in [4].

Over the course of the five submissions the VDC's total current consumption has been reduced and the current consumption between the bright and dim states of the VCSEL diode has been made more constant. Since the final VCSEL array will have a common cathode, this latest submission of the VDC circuit was made compatible with the array.

In Figure 6 we show the VCSEL current generated by the VDC as a function of the external control current I_{set}. The dim current is ~ 1mA as expected. The bright current saturates at high values of I_{set}. The saturation current is determined by the effective resistance of the VCSEL and maximum voltage provided by the VDC for a 2.5 V supply voltage. The saturation current is above 14 mA. We observe fairly balanced current consumption on the latest VDC circuits. In Fig. 7 the duty cycle of the output signal is shown for eight VDC chips. All chips have a duty cycle that falls within the required (50±4)%. The rise time of the output signal is typically ~1 ns. A few channels have rise times as large as 1.5 ns. The fall times of the output signals are all measured to be < 1.0 ns over the operating range of the circuit

The latest DORIC chips differ in function only slightly from the previous version. We have performed detailed measurements on samples from the latest version and verified that it satisfies all design specifications. The typical threshold for no bit errors is ~25 µA, well below the 40 µA spec. Channels with threshold above 40 µA can be brought into spec using the noise cancelling circuit. The threshold for no bit errors is independent of the activity in adjacent DORIC channels.

The electrical characteristics of VDCs and DORICs on opto-boards (Figure 8) have been studied in detail. We produce opto-boards of two flavours with each opto-board serving six or seven modules. To maximize the number of spare opto-boards, all opto-boards are fabricated to serve seven modules. For outer barrel layer and the disk system each module requires one link for transmitting data, therefore each opto-board contains two VDCs plus one VCSEL array opto-pack on the top side and two DORICs plus one PIN array opto-pack on the bottom side. The inner barrel (B) layer is expected to have a higher hit occupancy. Therefore each module requires two links for transmitting data to the ROD. The top side hence contains four VDCs plus two VCSEL array opto-packs with each pair of links serving a module connected to adjacent fibers in an 8-fiber ribbon.

We have verified that the DORIC thresholds are still low even after mounting on the opto-boards. For example, on fully populated opto-boards we routinely achieve PIN current thresholds for no bit errors of ~25 µA using the four-channel DORIC-I5e. The threshold for no bit errors is independent of the activity in adjacent DORIC channels.
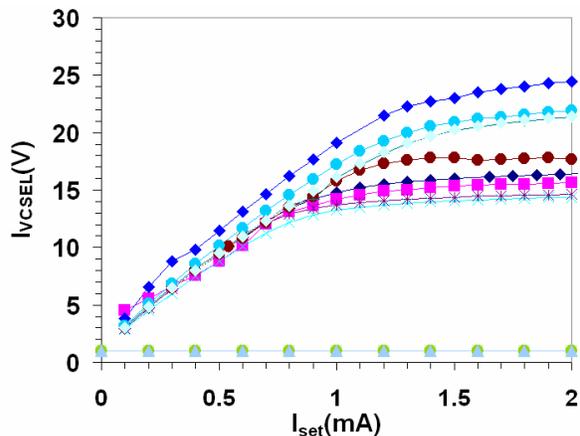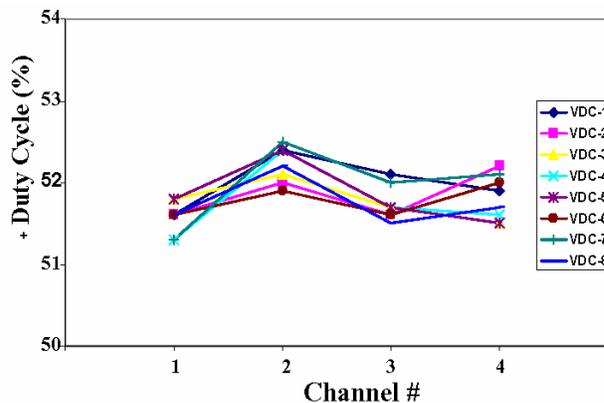

Figure 6: Measured VDC output current Vs Iset
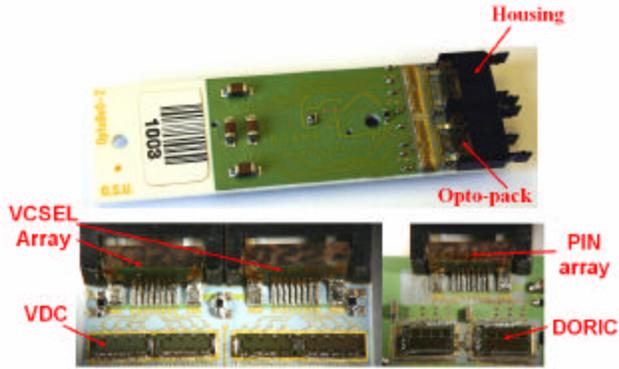

Figure 7: Measured duty cycle for eight VDC chips.

Figure 8:Example of a populated BeO opto-board.

VI. IRRADIATION STUDIES

Irradiation results from previous 0.25 µm submissions with 24 GeV protons at CERN have demonstrated that VDCs and DORICs from this process exceed the pixel detector's radiation hardness criteria. In September 2001 13 DORICs and 13 VDCs were irradiated up to a dosage of 50 Mrad (1.7 x 10^{15} p/cm^2). We observed no degradation in the amplitude and clock duty cycle of the output of the VDC. For the DORIC, the PIN current threshold for no bit errors remained constant. We received the irradiated chips one month after the irradiation and found that one chip had a much higher threshold. It was unclear whether the observed degradation of this chip was due to radiation or mishandling.

In August 2002, we irradiated VDC and DORIC circuits from the fourth deep submicron submission in the same proton beam at CERN. In a so-called cold box setup, we performed electrical testing of single channel VDC and DORIC circuits. For the 10 tested DORIC circuits we observed that the PIN current thresholds remained constant at ~12 µA up to the total dose of 57 Mrad. We found the bright and dim VCSEL currents for the eight tested VDC circuits to be constant throughout the irradiation. We have compared the performance of the VDC-I4 chips a month after irradiation to their performance before the irradiation. We observed no significant degradation of circuit performance on VCSEL drive current. There was also no significant change in the rise/fall time, clock duty cycle and current consumption.

In August 2003 we repeated the cold box tests, this time using VDCs and DORICs from the fifth submission. As expected, there was no degradation in their performance after exposure to a total dose of ~ 60 Mrad.

In addition to the cold box setup we also monitor, in real time, the optical power and threshold for no bit errors using a shuttle setup. Opto-boards are mounted on a shuttle that can be remotely moved in and out of the beamline. In this setup pseudo-random BPM signals are generated in the control room and sent via 25m of optical fibers to VDCs and DORICs on opto-boards located in the beam target area. The decoded clock and command data are then sent back to the control

room optically and are compared with the original BPM signals.

In our June 2004 irradiation four fully populated opto-boards were mounted in the shuttle setup, two at a time. We typically exposed the opto-boards to ~5Mrad (10 hours) before moving them out of the beamline in order to allow the VCSELs to anneal. In Figure 9 we show the PIN current thresholds for no bit errors, measured on one of the opto-boards during the irradiation study. We observe that the PIN current thresholds for no bit errors are all below 40 µA and remain constant up to the total dose of 32 Mrad. We also measured bit errors during spills and used it to calculate the SEU cross section. Using the Estimated particle flux at the location of the opto-board on the PIXEL detector, we calculate the bit error rate (BER). We find that BER decreases with PIN current as expected, as shown in Figure 10 for one of the opto-boards. The BER at 100 mA of PIN current is ~3 x 10^{10}. Considering that the DORIC spec. for BER is $< 10^{11}$, we find that the opto-link error rate is limited by SEU .The optical power returned from the opto-board to the control room over the course of the irradiation for one of the opto-boards is displayed in Figure 11. We observe a general trend in the data: during an irradiation period the returned optical power decreases; as the VCSEL anneals, the optical power increases, and some of the lost power is recovered as expected. We find that power is well above the minimum spec of 500 µW after 32 Mrad.
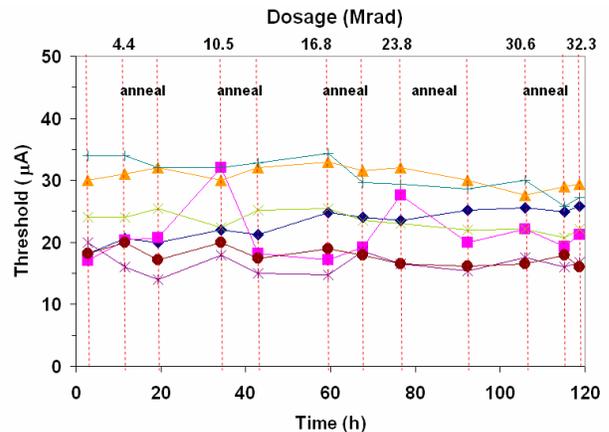

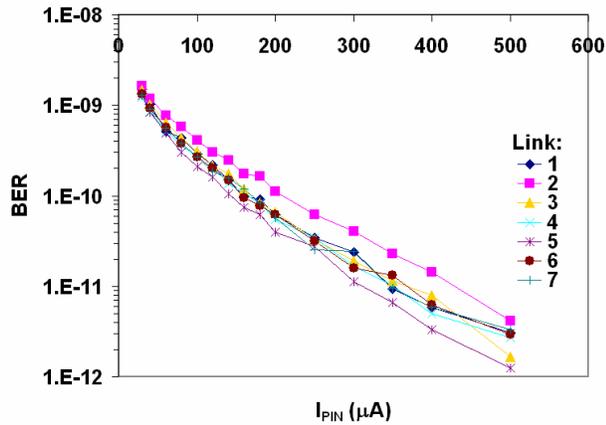Figure 9:Threshold for no bit errors Vs radiation dose for one of the four opto-boards in the shuttle setup.

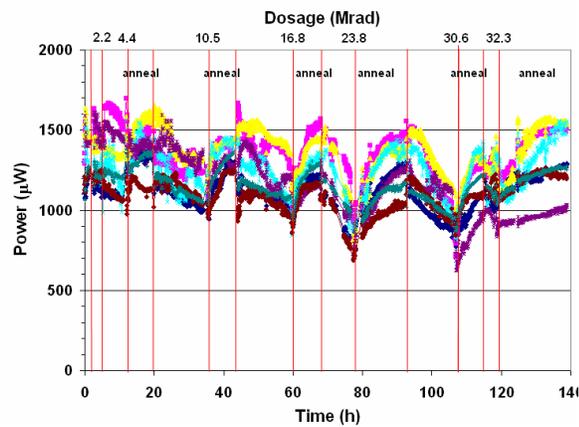Figure 10: Bit error rate (BER) Vs PIN current for one the opto-boards.

Figure 11:Optical power Vs time (dose) for one of the four opto-boards in the shuttle setup.

VII. SUMMARY

We have developed VDC and DORIC chips in deep submicron (0.25 µm) technology using enclosed layout transistors and guard rings for improved radiation hardness. The prototype circuits as well as their carrier, the opto-board, meet all the requirements for operation in the ATLAS pixel detector's optical readout system and further appear to be sufficiently radiation hard for ten years of operation at the LHC. We are now moving from the prototype stage of the project to the production phase.

IX. REFERENCES

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[3] G. Anelli et al, "Radiation Tolerant VLSI Circuits in Standard Deep Submicron CMOS Technologies for the LHC Experiments: Practical Design Aspects," IEEE Trans. on Nucl. Sci., Vol. 46, No. 6 (1999) 1690.

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